A High Power Handling Capability CMOS T/R Switch for X-Band Phased Array Antenna Systems

Tolga Dinc, Samet Zihir, Ferhat Tasdemir, and Yasar Gurbuz

Faculty of Engineering and Natural Sciences, Sabanci University
Orhanli, Tuzla, 34956 Istanbul, Turkey

***Abstract* — This paper presents a single-pole double-throw (SPDT) transmit/receive (T/R) switch fabricated in 0.25-µm SiGe BiCMOS process for X-Band (8 – 12 GHz) phased array radar applications. The switch is based on series-shunt topology with combination of techniques to improve insertion loss (IL), isolation and power handling capability (P_{1dB}). These techniques include optimization of transistor widths for lower insertion loss and parallel resonance technique to improve isolation. In addition, DC biasing of input and output ports, on-chip impedance transformation networks (ITN) and resistive body-floating are used to improve P_{1dB} of the switch. All these design techniques resulted in a measured IL of 3.6 dB, isolation of 30.8 dB and P_{1dB} of 28.2 dBm at 10 GHz. The return losses at both input and output ports are better than 16 dB from 8 to 12 GHz. To our knowledge, this work presents the *highest P_{1dB} at X-Band* compared to other reported single-ended CMOS T/R switches in the literature.**

***Index Terms* — T/R switch, SPDT switch, phased array radar, 0.25 µm CMOS, body-floating, DC biasing.**

I. Introduction

As a result of recent advances in Si-based IC technologies, next generation X-band Phased Array Radar systems aim to use low-cost, fully integrated transmit/receive (T/R) modules in order to decrease deployment and operational expenses [1]. In fully integrated T/R module design, one particular challenge is the design of CMOS T/R switch since it can directly affect the transmission efficiency and the noise figure of the receiver/system [2]. Therefore, in the recent years, CMOS T/R switch design has become an active area of research and several design techniques are reported to enhance IL, isolation and P_{1dB} compression point of T/R switches implemented in CMOS process [3]-[9]. In this work, we present a new CMOS SPDT T/R switch designed, based on design techniques for improving IL, isolation, and P_{1dB}.

As shown in Fig.1, SPDT T/R switch is a block in a TR module that routes antenna to either transmitter (TX) or receiver (RX). Hence, a typical SPDT T/R switch can operate either in transmit or receive mode at which low-loss paths are formed between ANT and TX or RX while isolating the other port, respectively.

In a typical transceiver system, primary aims are to direct high power RF signal from transmitter to antenna

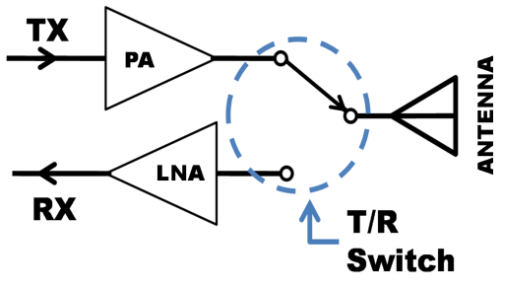

Fig. 1. A simple block diagram of T/R module.

while preventing leakage of that large signal into more sensitive front-end of receiver and to provide a low loss path between TX/ANT and particularly ANT/RX ports. Therefore, a T/R switch designed for a transceiver system should provide low loss and high isolation between TX-RX ports, as well as handling high power output signals of power amplifier during transmit mode of operation.

II. Circuit Design

In this work, an X-Band SPDT T/R switch whose schematic is shown in Fig. 2 is designed. It is mainly based on series-shunt topology reported in [3]. M1 and M2 transistors perform the main switching function of directing signal between TX/ANT or ANT/RX ports. M3

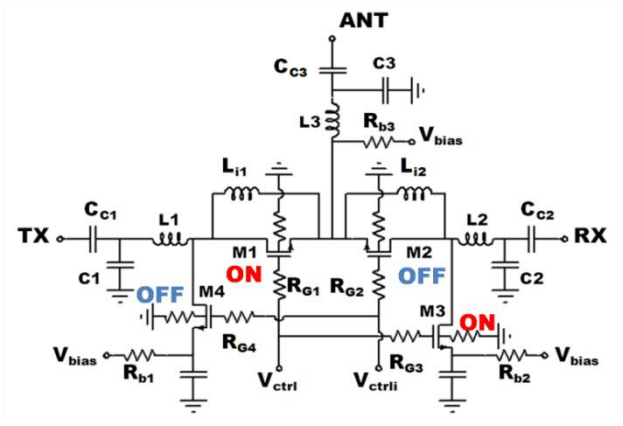

Fig. 2. Circuit schematic of the designed SPDT T/R switch. In TX mode, M1 and M3 operate in deep triode region (ON) while M2 and M4 operate in cut off region (OFF).

and M4 transistors improve isolation between TX and RX ports by grounding the leakage signal. Operation of the switch is as follow: when V_{ctrl} is high and V_{ctrli} is low, the switch operates in the transmit mode. In that mode, M1 and M3 operate in deep triode region (ON state) while M2 and M4 operate in cut off region (OFF state). Hence, channel resistance of M1 is very low and it forms a low loss connection between TX and ANT so that incoming signal from transmitter can be routed to antenna. Since M2 is operating in cut off region, channel resistance is very large and RX port is isolated from TX and ANT. Also, leakage signal due to parasitic coupling in M2 is directed to ground through low resistance path formed by M3 transistor before reaching receiver end. In receive mode, basic operation of the switch is similar to transmit mode and only difference is that roles of M1 and M3 are interchanged by M2 and M4, respectively.

Several techniques are incorporated into basic series/shunt topology to improve IL, isolation and power handling capability. Firstly, the sizes of the NMOS transistors in Fig. 2 are scaled for lower insertion loss, without degrading the isolation significantly. Insertion loss is mainly determined by resistances of M1 or M2 in the ON state. Resistance of the MOS transistor in the ON state should be as low as possible to decrease insertion loss of the switch. The resistance of a MOS transistor operating in the deep triode region (R_{on}) is defined by

$$R_{on} = \frac{1}{\mu_n C_{ox} (\frac{W}{L})(V_{GS} - V_{th})} \quad (1)$$

As can be seen in (1), as the width increases for fixed length of transistors, on resistance decreases and in return insertion loss decreases. However, there is a practical limit in increasing transistor width since as the width is increased, source/drain to body parasitic capacitances and, in return, coupling to substrate increases. In other words, there is a trade-off between R_{on} and parasitic capacitance which results in an optimum value for width of the transistor at a given operating frequency. The optimum width for minimum insertion loss at 10GHz has been found as 600-µm.

To improve the insertion loss and power handling capability, we have taken into account the effect of **DC** biasing. Based on the analysis of this effect, antenna node and sources of shunt transistors are biased at 2V through R_{b1} - R_{b3} resistors. This is to increase turn-on voltage of source/drain-to-body junctions and to decrease voltage dependent parasitic capacitances of NMOS transistors. The values of R_{b1} - R_{b3} should be high enough to prevent leakage into bias port. Otherwise, considerable amount of the input signal would be lost due to leakage and thus insertion loss would increase. Based on our analysis and confirmation by simulations, R_{b1} - R_{b3} resistors are chosen as 10-kΩ to prevent this phenomenon. Complete biasing method is shown in Fig. 2. A value of 8 pF for C_{B1} and C_{B2} by-pass capacitors are used to bias source terminals of M3/M4 while introducing RF ground to the sources of M3 and M4 [10].

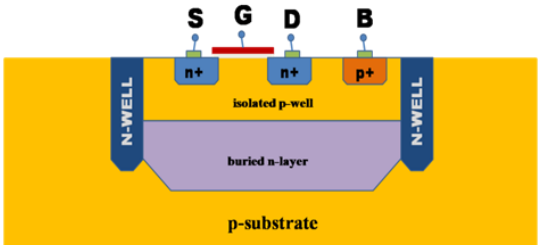

Fig. 3. Cross-sectional view of a typical isolated NMOS transistor.

As the frequency increases, parasitic capacitances' effect on the isolation becomes significant. Therefore, **to** improve the isolation of the switch at X-Band, shunt inductor resonance technique is used. To implement this technique, 680 pH inductors L_{i1} and L_{i2} are connected in parallel with M1 and M2 transistors. At resonance frequency in TX mode, inductor L_{i2} resonates with total parasitic capacitance of M2 to form a high impedance path to RX port. Hence, coupling through OFF switching transistor M2 to RX port reduces.

Power handling of the T/R switches is mainly limited by forward biasing of source/drain-to-body junctions during negative cycles of large RF signal. Body floating technique is used to improve power handling of the switch by reducing the signal loss through source/drain-to-body junctions. To implement this technique, body of the all transistors are connected to ground through 10-kΩ resistors. Isolated NMOS (iNMOS) transistors, shown in Fig. 3, offered by IHP 0.25 µm BiCMOS process is used to separate the body of each transistor from the p-substrate to be able to use transistors as four terminals device and apply body floating technique.

Besides DC biasing and body floating techniques, impedance transformation networks are employed to improve P_{1dB} of the switch. A 50 Ω source and load impedances at TX, RX and ANT port are transformed into lower impedances. Both series C - shunt L and shunt C-series L matching networks were tried in analysis and simulations. According to these results, a matching is achieved by shunt C- series L, in a broader frequency band and thus becoming our choice for matching network. 200fF metal-insulator-metal (MiM) capacitors and 540 pH octagonal integrated inductors are used to implement these networks.

III. Measurement

The switch was fabricated in IHP, 0.25-µm SiGe BiCMOS technology. This technology provides one-poly and five-metal layers, including thick metal layers to implement high-Q integrated inductors. The die photo of the switch is shown in Fig. 4. The chip area, including pads, is 0.44 mm^2. Inductors are custom designed with the thickest top metal layer in the process to take advantage of its lower resistivity and lower capacitance to ground.

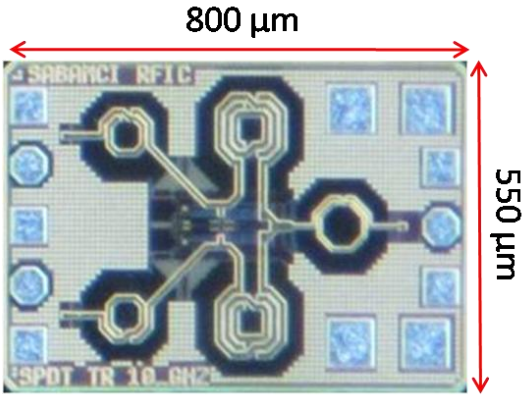

Fig. 4. Die photo of the SPDT T/R switch. The chip area including pads is 0.44 mm^2.

Measurements of T/R switch were performed under 4.5 V and 0 V control voltages. As shown in Fig. 5, the measured insertion loss and isolation is 3.6 dB and 30.8 dB, respectively, at 10 GHz. Insertion loss of the switch varies between 3.2 dB and 4.1 dB in the whole span of X-Band. The measured isolation is between ANT and RX ports. According to analysis and simulations, TX-RX isolation is almost same with ANT-RX isolation. Measured return losses are shown in Fig. 6. The return loss at TX port, S_{11}, is -18 dB at 10 GHz and ranges from -19 dB to -16 dB at X-Band. The return loss at ANT port, S_{22}, is -28 dB at 10 GHz and ranges between -18 dB and -28 dB at X-Band. Due to the symmetry of the switch, IL and RL in the receive mode are almost equal to transmit mode values. As shown in Fig. 7, the switch results in an input 1 dB compression point (IP_{1dB}) of 28.2 dBm at 10 GHz. By biasing sources and drains of the transistors to a higher potential, higher power handling can be achieved at the expense of reliability of the switch. In addition to operation in the X-Band, switch can also operate from 6 GHz to 8 GHz with adequate figures of merit.

TABLE I compares performance of our new switch with that of other single-ended CMOS T/R switches, in the literature, operating at X-Band. This work achieves the highest power handling capability among the single-ended CMOS X-Band switches to up to the date, to the best of our knowledge.

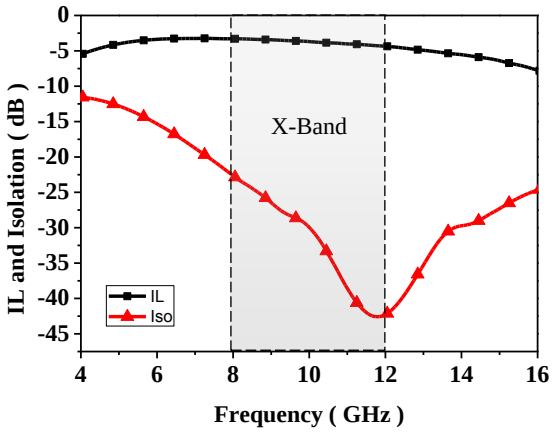

Fig. 5. Measured insertion loss and isolation of the T/R switch.

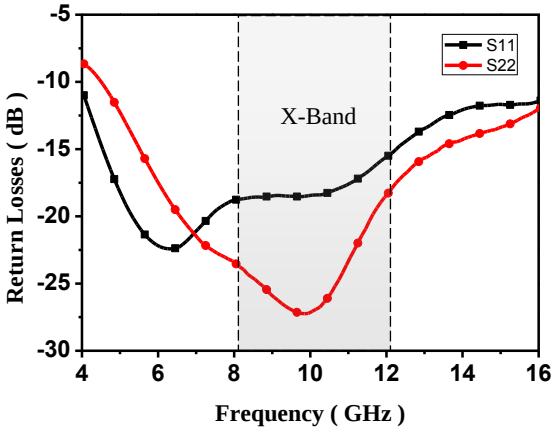

Fig. 6. Measured input return loss, S11, and output return loss, S22 of the T/R switch.

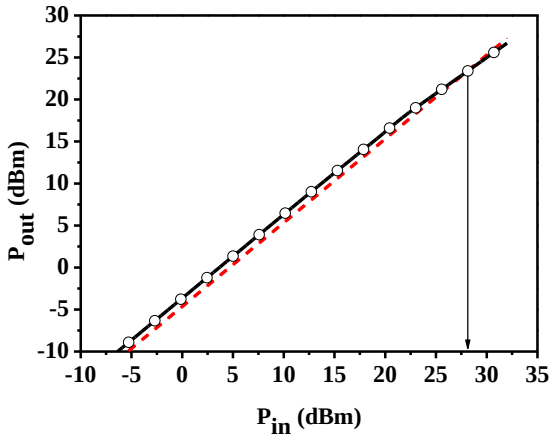

Fig. 7. Measured 1 dB compression point (P1dB) of the T/R switch at 10 GHz.

TABLE I
COMPARISON OF THE SWITCH WITH REPORTED WORKS

Frequency (GHz)	Figures of Merit			Chip Area (mm^2)	Technique	Technology	Ref.
	IL (dB)	Isolation (dB)	P_{1dB} (dBm)				
8-12	**3.2 – 4.1**	**23.2-42.5**	**28.2**	**0.44**	**Series-shunt, Body floating, ITN, Parallel Resonance, S/D Biasing**	**0.25 µm SiGe BiCMOS**	**This work**
3-10	3.1 ± 1.3	25–32	18-20	0.62	Distributed Topology	0.18 µm CMOS	[11]
3- 10.6	2.2 – 4.2	33–37	-	0.9	Synthetic Transmission Line	0.25 µm CMOS	[12]
10	1.81	21.9	10.1	0.67	Shunt	0.13 µm SiGe BiCMOS	[1]
	2.25	23.1	11.1	0.58	Series/Shunt		

IV. Conclusion

This paper presented an X-Band T/R switch fabricated in 0.25-µm SiGe BiCMOS technology. To authors' knowledge this paper presents the single-ended CMOS T/R switch with highest P1d at X-Band. The switch is based on series-shunt topology with combination of the different design techniques such as parallel resonance technique to improve isolation, DC biasing the input and output ports, using on-chip impedance transformation networks (ITN) and resistive body-floating to improve P_{1dB} and finally scaling of transistor sizes for lower insertion loss of the switch.

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