A New Resonant Circuit for 2.45 GHz LC VCO with Linear Frequency Tuning

Samet Zihir, Ferhat Tasdemir, Tolga Dinc, and Yasar Gurbuz

Faculty of Engineering and Natural Sciences - FENS, Sabanci University, Orhanli-Tuzla 34956, Istanbul, TURKEY

***Abstract* — A new MOS varactor bank is proposed to implement a 2.45 GHz SiGe BiCMOS LC-tank voltage controlled oscillator (VCO) with linear frequency tuning. Compared to a conventional VCO, the proposed technique improves the quality factor of the LC-tank while preserving the linearity of the circuit. Realized in 0.25-µm SiGe BiCMOS technology, VCO exhibits 35% VCO gain (K_{VCO}) variation from 2.29 to 2.66 GHz with a 16% tuning ratio. The VCO also exhibits a phase noise of -113 dBc/Hz at 1 MHz offset frequency and consumes 1.7 mA from 1.8 V supply.**

***Index Terms* — Voltage controlled oscillator, SiGe BiCMOS, linear frequency tuning, VCO gain (K_{VCO}).**

I. Introduction

The explosive growth of the wireless communication market is expected to continue in the future. The ISM (Industrial, Scientific and Medical) bands are open frequency bands and are the host for standardized and proprietary protocols such as Bluetooth, ZigBee and WiFi. The development of high performance applications has driven the demand for low power and low cost IC solutions for wireless transceiver RF front-ends. Fully integrated, including the tank circuit, voltage-controlled oscillator (VCO) is one of the most important and challenging building blocks in a RF transceiver.

The gain of VCO (K_{VCO}) determines the loop characteristics and overall performance of the Phase Locked Loop (PLL) -based frequency synthesizers. Using a VCO with linear f-V characteristics improves the performance of PLL blocks. Deficiency of linearity in tunable VCOs can complicate the PLL design and generates jitter in the system [1]. To achieve a VCO having constant K_{VCO} several techniques have been published, including varactor banks in LC tank [2], differently-biased varactor banks [3] or widely tunable varactors [4]. One drawback of these techniques, in general, is the degradation of quality factor of the LC tank. Even though inductor quality factor is the limiting factor in LC-tank VCOs, the quality factor of parallel-connected MOS varactors become comparable with inductor quality factor, resulting a potential improvement and degradation source of phase noise [5]. This problem becomes more severe if varactor banks are used to obtain more linearity and higher frequency sweep. Therefore, there is a demand for the improvement of quality factor of capacitor source of the LC tank.

In this work, we have developed a new technique to improve the quality factor of the MOS varactor-bank. Section II illustrates the design technique of the new LC-tank VCO. Experimental results of the new method and comparison with literature given in Section III and, finally, conclusion provided in Section IV.

II. VCO Design and Implementation

The schematic of the proposed LC VCO is shown in Fig. 1. PMOS current mirrors are used to improve phase noise of the VCO while reducing the generated noise from current source [6].

The proposed MOS varactor bank (linearization circuitry) is also shown in Fig.1. The linearization circuitry is much different from the conventional varactor banks that use varactors to improve the quality factor of the varactor bank.

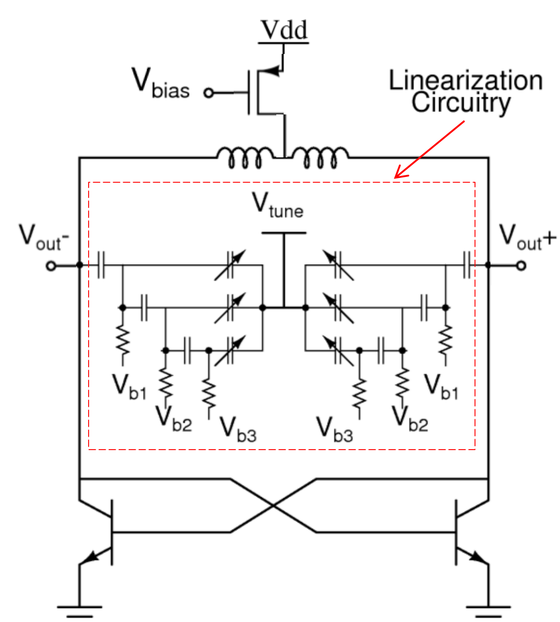

Fig. 1 Designed LC-tank VCO with linearization MOS varactor bank.

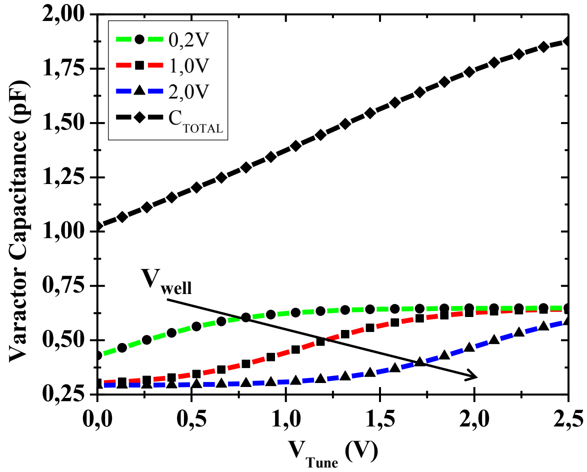

Fig. 2 Capacitance change of MOS varactor with different bias voltages.

Fig. 2 depicts the capacitance values for a frequency of 2.45 GHz and several tuning voltages V_W. Varactor stages are connected in parallel and biased at different voltages, as shown in Fig. 2, to obtain a linear K_{VCO} [2]. Although this method improves the linearity, the sensitivity of MOS varactors can degrade the phase noise performance of the VCO [7].

The quality factor of a varactor that used in the LC tank of the VCO can be given as [8],

$$Q_{var} = \frac{1}{2\pi f C_{var} R_{series}} \tag{1.1}$$

where R_{series} is the series resistance of the varactor. The quality factor and the capacitance of the varactor also depend on the bias voltage, V_{bias} as shown in Fig. 2. The simulated C-V curve and quality factor of the varactor used in the VCO is plotted in Fig. 3.

In conventional LC-tank VCOs, varactors are connected in parallel with different bias voltages as shown in Fig. 4

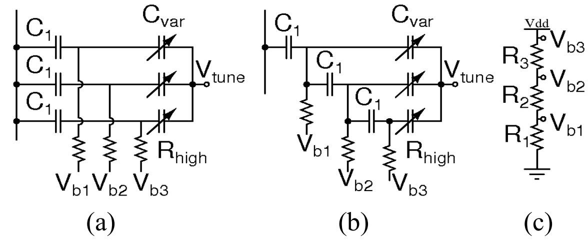

Fig. 4 (a) Conventional MOS varactor bank, (b) proposed MOS varactor, and (c) bank voltage divider.

(a). Because of biasing scheme provided in Fig. 2, the quality factor of each varactor is different, resulting a decrease in the overall quality factor of the LC-tank.

The same MOS varactors, with the same bias voltages, and C_1 capacitances are used in the proposed method, as shown in Fig. 4 (b). The quality factor of the varactor bank can be improved, at the expense of total capacitance tuning range. In this approach, the varactor, having a lower Q, is utilized in the innermost part of the bank and biased with V_{b3}, as shown in Fig. 4(b). The varactor, having a higher Q is kept at the outer part of the tank, and biased with Vb1, also shown in Fig. 4 (b). Hence the effect of lower Q varactor is suppressed without sacrificing its tuning range. .

The quality factor of both conventional, shown in Fig. 4 (a), and proposed, shown in Fig. 4(b), are calculated and compared in order to illustrate the effectiveness of the proposed varactor bank approach. The quality factor of the proposed MOS varactor bank is calculated as 33.1 whereas conventional varactor bank has a quality factor of 29.5, clearly presenting a 12.2 % improvement at 2.45 GHz. This improvement can directly improve the Phase Noise performance of the proposed VCO, according to the Leeson Eqn. [9] Phase Noise ~ log (1 / Q^2).

To highlight the linearity performance of the proposed new method, the proposed VCO and a non-linear

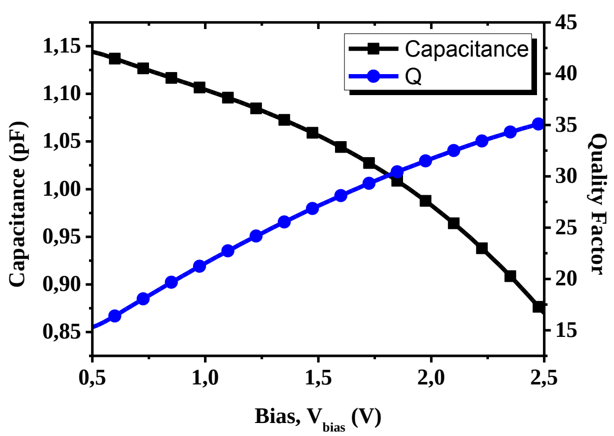

Fig. 3 Simulated C-V curve and Q for the varactor used in VCO.

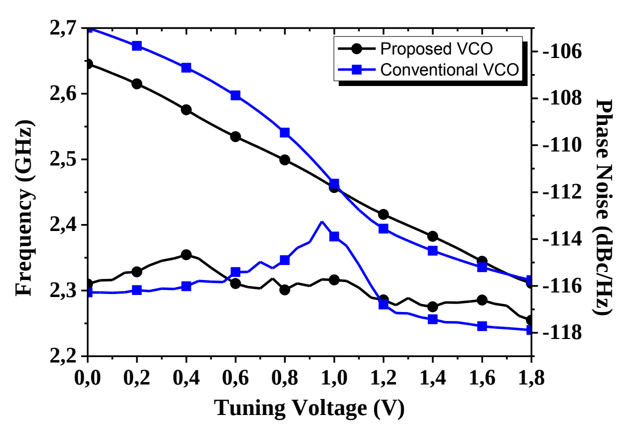

Fig. 5 Comparison of frequency and phase noise performance of conventional and proposed VCOs.

conventional VCO with $V_{b1}=V_{b2}=V_{b3}$ are compared and given in Fig. 5. The comparison of the simulation results, in Fig. 5, shows that proposed VCO achieves a higher linearity in the desired band with flat response in phase noise, compared to conventional VCOs.

III. Measurement Results

An ISM band LC-tank VCO with linear frequency tuning characteristic is implemented in 0.25 µm IHP SiGe BiCMOS process technology. Fig. 6 shows the microphotography of the designed LC-tank VCO with labeled pins.

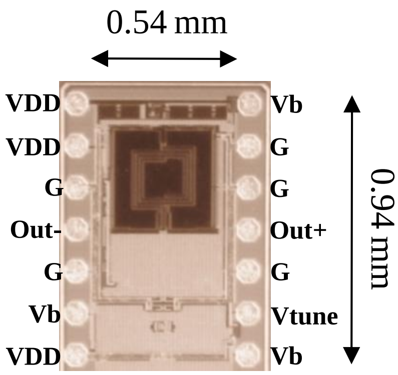

Fig. 6 The microphotography of the designed VCO.

The VCO chip core size is 0.54 mm x 0.94 mm which occupies 0.5 mm² and 0.7 mm² with pads include, shown in Fig. 6. Single-ended measurements are performed for one of the differential outputs using 50 Ω probes. The losses in the cables of the test setup, typically 1-1.5 dB, have not been calibrated out in the spectrum measurements. Agilent's E4407B Spectrum Analyzer is used to measure both output frequency-power and phase noise performance of the VCO.

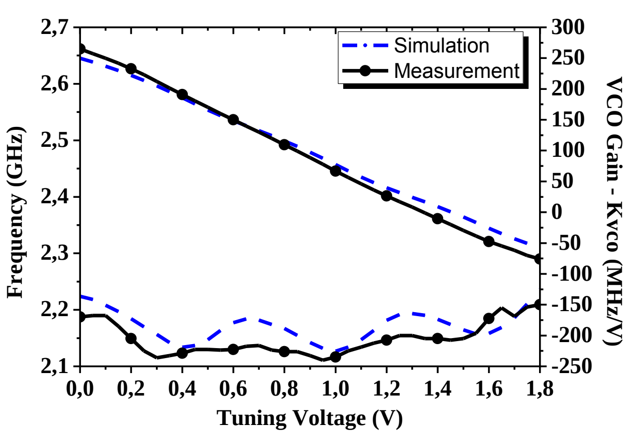

Fig. 7 Comparison of simulation and measurement results of frequency and VCO gain (Kvco) with respect to tuning voltage.

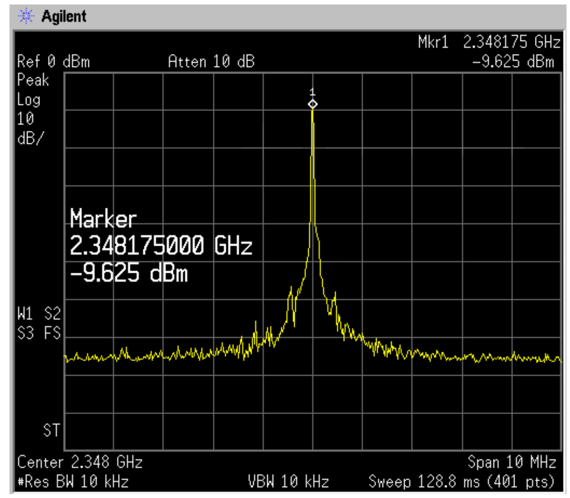

Fig. 8 Measured oscillation frequency.

The oscillation frequency and VCO gain of the proposed VCO are shown in Fig. 7. It is measured that VCO can be tuned from 2.29 GHz to 2.66 GHz, 370 MHz (16 %) with approximately 220 MHz/V VCO gain. Variations of the VCO gains (K_{VCO}) for simulation and measured results are within 32 % (simulation) and 35 % (measurement), as presented in Fig. 7 and also compared in Table I. These percentage variations in our study are better with respect to similar studies in the literature, as presented in Table I.

The core of the VCO consumes 1.7 mA whereas buffers consume 4.8 mA from a 1.8 V supply. The output power varied from -9.7 dBm to -8.5 dBm in the tuned frequency range. One of the measurement results showing the oscillation frequency at 2.34 GHz with 10 MHz span is shown in Fig. 8. The measured phase noise performance is given in Fig. 9 where -113.3 dBc/Hz is achieved at 1-MHz and -132 dBc/Hz at 10-MHz offset frequency. Relatively higher VCO gain (220 MHz/V) is assumed to be the source of a very small degradation of phase noise, down to -112 dBc/Hz .

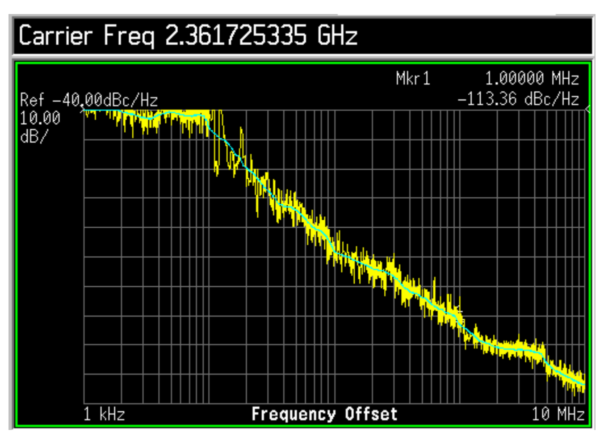

Fig. 9 Measured phase noise of the proposed VCO.

TABLE I
PERFORMANCE COMPARISON WITH OTHER PUBLISHED WORKS

Ref.	Tech [μm]	f_{osc} [GHz]	Tuning Range [%]	ΔKvco [%]	f_{step}/code [%]	Phase Noise [dBc/Hz]	Power Cons. [mW]
[2]	0.18	5.2	18.0	-	9.56	-113.7[#1]	9.7
[4]	0.35	5.6	8.8	41.4	-	-116.0[#1]	10.2
[10]	0.18	1.7	66.7	42.0	170	-127.1[#1]	10.8
[11]	0.13	3.6	22.5	28.0	-	-165.1[#2]	44.0
[12]	0.13	2.4	3.3	60.0	-	-126.0[#3]	3.4
This work	0.25	2.45	16	35.0	-	-113.3[#1]	3.1

[#1]Phase noise results is measured at 1 MHz offset from the carrier.
[#2]Phase noise result is measured at 20 MHz offset from the carrier.
[#3]Phase noise result is measured at 3 MHz offset from the carrier.

The comparison of the proposed VCO with previously published ones is given in Table I. As also seen in the Table I, our results of power consumption, tuning range and K_{VCO} variations in the proposed tank/VCO are better than others, especially when considered overall performance.

IV. CONLUSIONS

In this work, we have demonstrated a 2.45 GHz LC-tank VCO employing a new MOS varactor bank which increases the quality factor of the LC-tank and in turn improves the linearity and phase noise of the VCO. Implemented in 0.25-μm IHP SiGe BiCMOS process technology, the proposed VCO achieves 16 % ratio from 2.29 GHz to 2.66 GHz. The designed VCO shows a K_{VCO} 35 % with phase noise between -112 dBc/Hz to -114.3 dBc/Hz. The output power of the VCO varies from -9.4 dBm to -8.5 dBm with 3.1 mW core power consumption from 1.8 V power supply. Because the proposed VCO suppress the VCO-gain fluctuation, it is well suited for PLL-based frequency synthesizers at ISM band.

ACKNOWLEDGEMENT

The authors would like to thank IHP Microelectronics for providing IC fabrication and technical support.

REFERENCES

[1] R. J. Baker, *CMOS: circuit design, layout, and simulation*. IEEE Press, New York, 1998.

[2] Y.- J. Moon, Y. -S. Roh, C. -Y. Jeong, and C. Yoo, "4.39-5.26 GHZ LC-Tank CMOS Voltage-Controlled Oscillator With Small VCO-Gain Variation," in *IEEE Microw. and Wireless Comp. Letters*, vol. 19, no. 8, Aug. 2009.

[3] B. Hanafi, and E. Hegazi, "A Technique for Truly Linear LC VCO Tuning, A Proof of Concept," in *Proc. IEEE Int. Conf. on Microelect.*, ICM, Dec. 2007, pp. 93-96.

[4] S. Kurachi, T. Yoshimasu, N. Itoh, and K. Yonemura, "5-GHz Band Highly Linear VCO IC with a Novel Resonant Circuit," in *Proc. Silic. Mono. Integr. Cir. in RF Syst.*, Jan. 2007, pp. 285-288.

[5] J. Maget, M. Tiebout, and R. Kraus, "MOS Varactors With n- and p-Type Gates and Their Influence on an LC-VCO in Digital CMOS," *IEEE J. Solid-State Circuits,* vol. 38, no. 7, pp. 1139-1147, July 2003.

[6] G. D. Astis, D. Cardeau, J.-M. Paillot, and L. Cascalescu, "A 5-GHz Fully Integrated Full PMOS LOW-Phase-Noise LC VCO," *IEEE J. Solid-State Circuits,* vol. 40, no. 10, pp. 2087-2091, 2005.

[7] J. Rogers, J. Macedo and C. Plett, "The effect of varactor nonlinearity on phase noise of completely integrated VCOs," *IEEE J. Solid-State Circuit*, vol. 35, no. 9, Sep. 2001.

[8] C. Cao, and K. O. Kenneth, "Millimeter-Wave Voltage-Controlled Oscillators in 0.13-μm CMOS Technology," *IEEE J. Solid-State Circuits,* vol. 41, no. 6, pp. 1297-1304, June 2006.

[9] J.-C. Nallatamby, M. Prignet, M. Camiade, and J. J. Obregon, "Extension of the Leeson formula to phase noise calculation in transistor oscillators with complex tanks," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, no. 3, pp. 690-696, Mar. 2003.

[10] J. Kim, J. Shin, S. Kim, and H. Shin, "A Wide-Band CMOS LC VCO With Linearized Coarse Tuning Charactertics," in *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 55, no.5, pp. 399-403, May. 2008.

[11] S. Samadian, "A Low Phase Noise Quad-Band CMOS VCO with Minimized Gain Variation for GSM/GPRS/EDGE," in *IEEE Circuits and Syst. Symp.*, ISCAS, May 2007, pp. 3287-3290.

[12] J. Mira, T. Divel, S. Ramet, J.-B Bedueret, and Y. Deval, "Distributed MOS Varactor Biasing for VCO Gain Equalization in 0.13μm CMOS Technology," in *IEEE RFIC. Symp.*, 2004, pp. 131-134.