Abstract—Deposited instead of thermally grown oxides were studied to form very high-quality inter-polysilicon dielectric layers for embedded nonvolatile memory application. It was found that by optimizing the microstructure, i.e., texture and morphology of the polysilicon layers, and by optimizing the post dielectric deposition anneal, very high-quality dielectric layers can be obtained. In this paper it is shown on simple capacitor structure level and full EEPROM device level that the electrical properties of interpoly dielectric layers can be improved tremendously by using deposited dielectric layers with additional rapid thermal anneal. Typical results are: a high charge-to-breakdown ($Q_{BD} \approx 25 \text{ C/cm}^2$), low leakage currents and decreased charge trapping during constant current stress. An additional advantage is the low thermal budget, which is very attractive for embedded applications. However, results depend on the polysilicon preparation, dielectric type and RTP anneal environment.

From electrical evaluation it appeared that even for deposited dielectric layers the influence of polysilicon surface roughness and corners is considerable.

The optimized combination of flat polysilicon layers, deposited inter-polysilicon dielectric and additional optimized rapid thermal anneal have been applied in full EEPROM devices. Cycling over one million cycles was possible, which indicates an endurance improvement by a factor of 10.

Index Terms—Charge-to-breakdown ($Q_{BD}$), interpoly tunneling, low-pressure-chemical-vapor-deposited (LPCVD) dielectrics, nonvolatile memories, RTP-annealing, silicon micro-structure, surface roughness.

I. INTRODUCTION

In order to obtain good data retention and endurance characteristics for nonvolatile memories, interpoly dielectrics with low conductivity and high breakdown fields have been topic of research for a long time [1]–[3]. Besides, developing dielectric layers with proper electrical qualities becomes even more complex when, in addition to good isolating properties for low and moderate applied voltages, good conduction properties at high voltages are required. This concerns the vertical injection punchthrough based MOS (VIPMOS) EEPROM [4], [5]. During reading and programming (low and moderate voltages) charge leakage is unacceptable, while high voltages are needed for achieving interpoly tunneling as erasing mechanism [4], [5]. Because thermal oxidation of polycrystalline silicon leads to roughening of the silicon [6]–[16], thermally grown polyoxides exhibit a higher conductance and lower electric breakdown field than oxides on monocrystalline silicon, when the top electrode is positively biased. Several authors have searched for techniques to control the surface roughening of silicon layers. Mori et al. [17], [18] found that the dielectric strength depends on polysilicon roughness as well as polysilicon dope. Jun et al. [19] proposed a new oxidation scheme, using an intermediate oxide layer preventing polysilicon consumption. Different oxidation temperatures and ambient have been proposed [20], [21] to control silicon roughness, which, however, only moderately improved the dielectric strength.

Recently, chemical mechanical polishing (CMP) has been introduced prior to polyoxide growth from N$_2$O directly in order to smoothen the polysilicon surface [22]. Silicon surface roughness typically decreased from 9 nm to 0.9 nm and an improved polyoxide quality was achieved. Combining CMP with deposited oxide layers yielded even better dielectric strength [23], but $Q_{BD}$ values are still susceptible for improvement.

Stacks of oxide/nitride/oxide (ONO) layers have been widely proposed for improving inter-polysilicon dielectric quality [18], [24]–[32]. However, since nitride layers have very poor tunneling properties, they are not applicable in devices using poly–poly tunneling (e.g., VIPMOS) and therefore they are beyond the scope of this paper.

In the last decade deposited dielectric layers have been investigated as a very promising alternative, since these dielectric layers are deposited on the polysilicon layer without silicon surface consumption, contrary to thermal oxidation. Low-temperature oxides (LTO) [33] deposited in a rapid thermal processing (RTP) system [34] or in a conventional low pressure chemical vapor deposition (LPCVD) system [35] have resulted in useful layers for thin film transistors [36]. Although post deposition treatments have been applied (see for instance [37]–[45]), the electrical properties are too poor for EEPROM application.

Deposition at higher temperatures, like TEOS [33], [46] or high temperature oxides (HTO) [33], [47] has lead to superior electrical properties (see for instance [1], [20]). Post deposition treatment in a rapid thermal processor (e.g., densification, reoxidation, and/or nitridation) is needed to obtain the desired electrical properties [45], [48]–[52]. Although using deposited oxides, the underlying polysilicon layer still plays a dominant roles.
role in the dielectric strength [53]. Therefore the microstructure, i.e., the texture and morphology, of LPCVD silicon layers has been investigated intensively as a function of different process parameters. In particular the roughness of the silicon surface has been examined.

This paper reports on the development of a combination of flat polysilicon and deposited interpoly dielectric layers with an additional post deposition anneal which are applied in nonvolatile memories (e.g., VIPMOS). By optimizing the deposition conditions of the polysilicon layers, the surface roughness of the As-deposited layers is considerably reduced. Roughness typically decreases from RMS = 7.4 to 0.7 nm. The roughest and flattest layers have subsequently been applied in simple capacitor structures for interpoly dielectric development and electrical evaluation. A combination of ultra flat polysilicon layer, deposited dielectrics and an optimized post deposition treatment appears to be a very attractive alternative for replacing thermal oxide layers. In order to investigate the functionality of these layers they have been applied in full EEPROM devices, on which retention and endurance tests have been applied.

II. EXPERIMENTS

P-type wafers were thermally oxidized to a thickness of 100 nm. Then a 300 nm silicon film (poly 1) was deposited by LPCVD at different temperatures (500, 550, or 625 °C), total pressures (0.1 and 1 mbar) and partial pressures of silane (SiH4) (0.1, 0.5, or 1 mbar). This layer was either annealed in N2 ambient at 600 or 800 °C or it was implanted with Phosphorus up to a dose of $8 \times 10^{15}$ cm$^{-2}$ at 50 keV and additionally annealed at 600 or 800 °C in N2 ambient. These layers were then ready for microstructure investigation [53] (see Fig. 1).

Subsequently some samples were used for realizing capacitor structures. After implantation and annealing of the first polysilicon layer the roughest and flattest variant were used to complete capacitor structures [53]. On top of the first polysilicon layer a 25 nm dielectric layer was deposited, which consisted of HTO from SiH2Cl2 and N2O at 800 °C. It was annealed in a rapid thermal processor at 950 °C for 20 min in different ambients: N2, O2, or N2O. For comparison, also dielectric layers without annealing were processed [referred to as control oxides see (Fig. 1)]. Then a second silicon layer (poly 2) of 300 nm was deposited by LPCVD at 625 °C. It was implanted with Arsenic up to a dose of $6 \times 10^{15}$ cm$^{-2}$ at 100 keV. After activating the dopant at 950 °C in N2 ambient and defining poly 2, all samples were covered with a 200 nm CVD oxide as a passivation layer. Contact holes were opened and Al was deposited and patterned to form capacitor structures. Finally, all devices were sintered at 400 °C for 30 min in wet N2 ambient.
III. RESULTS AND DISCUSSION

For the sake of clarity, this section is divided into three parts. Section III-A describes the results of the polysilicon microstructure investigation. The electrical measurements on capacitor structures are described in Section III-B and finally Section III-C discusses the electrical measurements performed on EEPROM devices.

A. Polysilicon Microstructure (Texture and Morphology)

In Fig. 2, the quantitative results of the AFM (atomic force microscope) measurements are shown. In particular the root mean square value (RMS) and the average roughness (Ra) will be concerned. Some samples will be discussed in more detail. Deposition of silicon films (LPCVD) at a temperature of 625 °C at a pressure of 0.1 mbar leads to a polycrystalline silicon layer with a (110) texture. This layer has a very rough surface (RMS = 7.4 nm and Ra = 5.8 nm) and small grains (θ = 100–150 nm). Implantation and additional annealing leads to polycrystalline silicon layers with a (111) texture and a slightly reduced surface roughness (RMS = 5.2 nm and Ra = 4 nm), hardly dependent on the anneal temperature.

When the deposition temperature is lowered to 550 °C, deposition at a pressure of 1 mbar (P_{partial} = P_{total}) results in amorphous silicon films, in which no texture (no preferential crystalline structure) is observed. Annealing at 600 or 800 °C results in polycrystalline silicon films with a (111) texture, smooth surface (RMS = 1.2 and Ra = 0.90 nm), again hardly dependent on the anneal temperature. Implantation and additional annealing leads to silicon films with a (111) texture and a slightly reduced surface roughness (RMS = 0.9 nm, Ra = 0.8 nm). Even smoother surfaces, approximating those of monocrystalline silicon, are obtained, when the pressure during deposition is decreased to 0.1 mbar (RMS = 0.6 nm, Ra = 0.5 nm). However, lower pressures are accompanied by longer deposition times, which may not be useful in practical applications. Implantation and additional annealing further decreases the surface roughness. In all cases a (111) texture develops, with a very flat surface and large crystals (θ = 250 nm). Concluding, decreasing the deposition temperature from 625 to 550 °C yields smoother surfaces.

Lowering the deposition temperature even further to 500 °C remarkably results in only a slightly increased surface rough-
ness (RMS = 1.2 nm, Ra = 1.1 nm). Because lowering the deposition temperature to 500 °C is accompanied by decreasing growth rates, these layers are not discussed in more detail. In Fig. 3 typical AFM surface scans are shown: One of the roughest surface and one of the flattest surface. Fig. 4 shows a typical cross section and a typical planar view TEM (transmission electron microscope) photograph of the flattest sample of Fig. 3. It appeared that the large structures from Fig. 3 are relatively large crystals/grains with different orientations.

From this point on the roughest and flattest polysilicon layers have been applied in capacitor structures for electrical evaluation of the dielectric layers. Depositing silicon at 550 °C at higher pressures (P = 1 mbar) leads to a slightly increased surface roughness (RMS = 0.9 nm; Ra = 0.8 nm). However, it yields a deposition time reduction (deposition rate = 4 nm/min) and will therefore be used when flat polysilicon layers are needed for the electrical measurements.

B. Electrical Measurements on Capacitor Structures

In this section, the improvements of interpoly dielectric layers are discussed, using electrical evaluation by charge-to-breakdown and current–voltage (I–V) measurements on simple capacitor structures.

Fig. 5(a) shows a schematic view of these structures. Structure A is a flat capacitor; structure B is a capacitor with corners/edges, referred to as single corner and structure C is a capacitor with many corners/edges, referred to as multi corner. Capacitors B and C are merely used to investigate the influence of poly1–poly2 edges later. The area of all capacitors is 1 x 10^{-4} cm².

In [50], it was shown that annealing could tremendously improve the electrical properties of deposited dielectric layers. Annealing in a rapid thermal processor in N₂O ambient yielded high Q_{BD} values (Q_{BD} ≈ 20 C/cm²) and low electron-trapping rates. In order to investigate what mechanism mainly
causes this improvement, annealings in N$_2$, O$_2$, and N$_2$O ambient have been compared.

Typical $J$–$E$ curves of the dielectrics are shown in Fig. 6. The electric field has been calculated with the dielectric-thickness as measured by ellipsometry on monitor wafers (i.e., monocrystalline wafers on which the dielectric layers were deposited directly). This thickness increased upon annealing, depending on the anneal environment.

In all ambients used, RTP annealing yields higher breakdown fields. The layers annealed in N$_2$O ambient conduct a lower leakage current and start conducting at higher voltages than the other dielectrics, when the top electrode (poly 2) is positively biased (i.e., electrons are injected from the bottom electrode).

Annealing in N$_2$ or O$_2$ ambient results in higher breakdown fields in comparison with the control oxide, but shows a $J$–$E$ curve that behaves irregularly for moderate applied electric fields, for which the reason is not yet understood.

In Fig. 7, typical $Q_{BD}$ plots of the samples are shown, from which also the trapping behavior can be determined. The stress condition was 2.5 mA/cm$^2$ constant current injection for positive bias. It can be seen that the annealed dielectrics in N$_2$ and N$_2$O ambient have a much higher $Q_{BD}$ and a much smaller voltage shift ($\Delta V$) than the control dielectric layer. However, annealing in O$_2$ ambient results in a lower $Q_{BD}$ value. During annealing in O$_2$ ambient a small thermal dielectric layer is grown ("thermal oxidation") [7], thereby roughening the underlying silicon layer, which affects the dielectric layer negatively. This has been confirmed by AFM measurements (after removing the oxide layer), where the roughening could be clearly observed. Roughness typically increased from RMS = 0.9–1.7 nm during annealing in O$_2$ ambient, while the roughness remained constant by annealing in N$_2$ or N$_2$O ambient.

Annealing in an inert N$_2$ ambient, which mainly aims for a densification of the dielectric layer, results in a higher
Fig. 10. Typical Weibull plots of the \( Q_{BD} \) for the N\(_2\) and O\(_2\) annealed dielectric layers under positive and negative stress. A constant current density of 2.5 mA/cm\(^2\) was applied to capacitors with an area of \( 1 \times 10^{-4} \) cm\(^2\). 

\( Q_{BD} \) and smaller voltage shift than the control oxide, which implies that the N\(_2\) annealed dielectric trapped fewer electrons. However, it still results in a too large \( \Delta V \), which can be explained by the unreduced amount of interface states.

Annealing in N\(_2\)O ambient is thought to achieve three effects, namely oxidation of the bulk non stoichiometric SiO\(_2\), a nitridation at the Si–SiO\(_2\) interface without roughening and a densification. It results in a very high \( Q_{BD} \) and very small voltage shift (\( \Delta V \)), implying that the N\(_2\)O annealed dielectric trapped very few electrons. This is mainly ascribed to the nitrogen peak (observed by means of Auger measurements) at the Si–SiO\(_2\) interface. The actual anneal mechanism is thought to be the replacement of weak Si–H, strained Si–O bonds or dangling bonds by Si–N bonds, leading to a relaxation of the interface stress. The interface state generation and neutral trap creation caused by hot electron injection should thereby be suppressed. Therefore, improved dielectric strength resulting in higher \( Q_{BD} \) values can be expected. By incorporating more nitrogen, which can be achieved by varying the anneal conditions or even using NO\(_2\) gas [15], the interface state generation can be decreased further. However, when too much nitrogen is incorporated the trapping in the bulk of the layer increases leading to inferior dielectric strength.

Compared to layers directly grown in N\(_2\)O ambient [21], [54], which first of all leads to silicon consumption and nitrogen present throughout the whole dielectric layer, even As-deposited layers have high \( Q_{BD} \) values and are attractive as inter-poly silicon dielectrics.

Plotting the \( J–E \) characteristics in the form of a Fowler–Nordheim (F–N) plot (\( J/E^2 \) versus \( 1/E \)) [55] straight lines were obtained for all dielectric layers, indicating F–N tunneling to be the major conducting mechanism. Moreover, according to the F-N model, from the corresponding slopes of these straight lines the apparent barrier heights for the electron tunneling from the bottom polycrystalline silicon layer to the SiO\(_2\) conduction band were determined. An electron effective mass of \( 0.5m_0 \) was used for these calculations [55]. The calculated barrier heights were 2.8 eV for the O\(_2\) annealing, 3.1 eV for N\(_2\) annealing and 3.2 eV for the N\(_2\)O annealing (the estimated measurement error was approximately 0.25 eV). In comparison with the control oxide (2.6 eV) the barrier heights increased upon annealing, with annealing in N\(_2\)O ambient resulting in the highest barrier. The roughening due to O\(_2\) annealing reveals itself as a smaller barrier height as compared to the other variants.

When multilevel storage or analog applications are concerned, the trapping behavior of dielectric layers becomes even more important, since voltage shifts might lead to a decreasing bit resolution. To make a reasonable comparison, we have related the voltage shift to the amount of charge that is forced through the dielectric layer. Therefore in Fig. 8, the voltage shift per \( Q_{BD} \) is shown as a function of the anneal ambient. All RTP annealings of the deposited dielectric layer improve the quality, but the N\(_2\)O annealed dielectric shows superior results in comparison with the other dielectric layers.

In Fig. 9, the Weibull distributions of charge-to-breakdown for 100 capacitors under 2.5 mA/cm\(^2\) constant current stress are shown for positive bias. Again, it is seen that the O\(^2\)
anneal affects the dielectric layer negatively, while the other annealings yield improved dielectric quality.

So far only the electron injection from the bottom electrode (positive top electrode bias) was considered. For negative top electrode bias, i.e., electron injection from the top electrode, a remarkable change in polarity preference was observed in $J-E$ characteristics, when a post-deposition anneal in N$_2$O environment was performed [50]. The annealed dielectric layers conducted a higher current than the As-deposited oxides, which is in contrast to positive top bias. This polarity preference was also observed for inter-polysilicon oxide layers, which were directly grown from N$_2$O [21], [54]. This is mainly ascribed to the nitrogen peak at the lower Si–SiO$_2$ interface. Concerning the N$_2$ and O$_2$ anneal ambients additional measurement results are shown in Fig. 10, where typical Weibull plots are depicted. As can be seen, annealing in O$_2$ ambient results in high $Q_{BD}$ values when negative top bias is applied, indicating that the electrical properties of the oxide layer are improved. However, while applying positive top electrode biasing remarkable low $Q_{BD}$ values are observed, indicating that an additional parameter, namely the surface roughness, deteriorates the electrical characteristics. So when the annealing is performed in O$_2$ ambient the improvement of the dielectric strength is surpassed by the consumption of the underlying polysilicon layer. Since erasure in the VIPMOS is carried out by applying a high voltage to the top electrode (erase gate), this result is unacceptable.

When annealing is performed in N$_2$ ambient the difference between positive and negative applied bias is much smaller. This indicates that the bulk of the oxide is mainly affected by this anneal, resulting in moderately improved $Q_{BD}$ data, but irregular $J-E$ curves.

Annealing in N$_2$O ambient gives superior results. Optimizing the N$_2$O anneal conditions with regard to the temperature, time and pressure during annealing, yielded even better dielectric layers [51]. In [51], it has been shown that annealing in N$_2$O ambient for 5 min at 925 °C and a pressure of 25 torr achieves the best electrical properties. A high charge-to-breakdown ($Q_{BD} \approx 25$ C/cm$^2$), low charge trapping and low leakage currents are obtained.

Next, the influence of the poly1–poly2 edge on the electrical properties has been verified electrically and the influence of surface roughness was evaluated. When a capacitor structure contains more corners, i.e., longer edges, a current is expected to flow at lower applied voltages. In Fig. 11, in which typical $I-V$ curves are shown for the three capacitor structures (structure A, B and C from Fig. 5, respectively), this is clearly observed. A measurable current flows at a voltage as low as 8 V (structure B and C), while in case of a flat capacitor current starts flowing at 15 V. An increasing amount of edges

**Fig. 12.** Typical Weibull plots of the three capacitor structures of Fig. 5, under both positive and negative bias. A constant current density of 2.5 mA/cm$^2$ was applied to capacitors with an area of $1 \times 10^{-3}$ cm$^2$. The influence of edges is clearly observed.

**Fig. 13.** Typical Weibull plots of the $Q_{BD}$ for (optimized) 25 and (un-optimized) 15 nm N$_2$O annealed dielectric layers on different polysilicon layers under positive stress, i.e., electrons are being injected from the bottom electrode. A constant current density of 2.5 mA/cm$^2$ was applied to capacitors with an area of $1 \times 10^{-3}$ cm$^2$. 
slightly moves the $I-V$ characteristic to the lower voltage regime. The electrical breakdown field, $E_{BD}$, also decreases with increasing amount of edges.

Statistical measurements of 100 capacitors result in the Weibull distributions of Fig. 12, in which typical plots are shown for the three capacitor structures under both positive and negative bias. In case of positive applied top bias, i.e., electron injection from the bottom electrode, the influence of the poly1–poly2 edge is clearly observed. When longer edges appear, i.e., when the edge of the overlap of the polysilicon layers increases, $Q_{BD}$ values decrease. Flat capacitors yield the highest $Q_{BD}$ values. It is notable that a negative applied bias results in curves that just differ slightly, indicating very good oxide quality. From the results it is clear that edges on the injecting electrode must be avoided as much as possible.

Summarizing it can be concluded that edges appearing in capacitor structures yield lower $Q_{BD}$ values, higher charge trapping and lower voltages to conduct a certain current density. This leads to poor retention properties as a consequence of locally enhanced current densities when electrons are injected from the bottom electrode.

In order to find out whether the surface roughness of polysilicon layers still is an important parameter when the electrical properties of the dielectric layers have been optimized, the influence of the surface roughness is verified again.

Fig. 13 shows the charge-to-breakdown Weibull distributions for 100 capacitors under 2.5 mA/cm$^2$ constant current stress. The largest $Q_{BD}$ is obtained for the 25 nm dielectric on flat polysilicon, which has a very narrow distribution. When the same dielectric layer is deposited on a rough polysilicon layer, suffering from locally enhanced electric fields and therefore locally higher current densities, the $Q_{BD}$ values are decreased by two orders of magnitude. When thinner dielectric layers (15 nm) are concerned, the same tendency is observed. Note that the anneal recipe has been optimized for 25 nm dielectrics only and therefore results of 15 nm dielectrics are likely to be susceptible for improvement. However, the difference between flat and rough polysilicon layers is less, which has also been observed in accompanying $I-V$ curves. The better step coverage and therefore lower thickness variation of thinner dielectric layers explain this.

Summarizing, the above-mentioned results show that deposited oxides with additional RTP N$_2$O anneal are very attractive for replacing polyoxides as interpoly dielectric, providing that the surface of the underlying polysilicon layers has an optimized flatness.

### C. Electrical Measurements EEPROMs

In order to confirm the functionality of the previously discussed interpoly dielectrics, complete EEPROM cells [Fig. 14(a)] have been realized, which have been derived form the optimized VIPMOS EEPROM [Fig. 14(b)] [4], [5], [56]. Programming is based on channel hot electron injection, while erasing is performed by F–N tunneling from the floating gate to the erase gate. An additional oxide layer has been added covering the sharp corners of the floating gate [Fig. 14(a)]. During erasure, the current is consequently forced through the flat part of the overlap between the polysilicon layers. Devices without this additional oxide layer suffered from undesirable high leakage currents at the corners of the floating gate and early breakdown during operating the memory cell. Voltages necessary for operating the memory cell are listed in Table I.

In Fig. 15, a typical endurance curve is depicted, which consists of two curves: one for the sample with an N$_2$O annealed interpoly dielectric (optimized process) and one for a control sample (As-deposited). The threshold voltage window of the N$_2$O annealed sample starts closing from approximately

<table>
<thead>
<tr>
<th>Terminal Voltages for Operating the Memory Cell of Fig. 14. The Source/Injector and Substrate Terminal Were Always at Ground Potential. The Cell Is Read by Applying a Step Voltage ($V_{read}$) on the Control Gate and Determining the Threshold Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{drain}$ [V]</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>Read</td>
</tr>
<tr>
<td>Program</td>
</tr>
<tr>
<td>Erase</td>
</tr>
</tbody>
</table>
106 cycles, while the threshold voltage window of the control sample starts already closing after 105 program/erase cycles. Therefore, the threshold voltage window remains constant for a larger number of cycles when the amount of trapped electrons is reduced by annealing in N\textsubscript{2}O.

In order to investigate the retention behavior, accelerated bake tests at $T = 250\,^\circ\text{C}$ under no applied voltage ($V_{\text{applied}} = 0\,\text{V}$) have been performed. In the VIPMOS cell, composed of 50 cells in parallel, no charge loss was observed, indicating no intrinsic charge loss problems. No difference was observed between the control oxide and N\textsubscript{2}O annealed oxide, indicating that the As-deposited oxide layer already has good isolating properties when no voltage is applied.

IV. CONCLUSION

In conclusion, the above results show that deposited oxides with additional N\textsubscript{2}O anneal are a very attractive alternative for conventional polyoxides. By optimizing the deposition conditions of the LPCVD polysilicon layers very smooth silicon layers can be obtained, which reduces the electric field enhancement and therefore improves the isolating properties of the dielectric layer upon it. The electrical characteristics of the deposited HTO dielectric layer can be largely improved by optimizing the post dielectric deposition rapid thermal anneal. From measurements on simple capacitor structures it has become clear, that annealing in N\textsubscript{2}O ambient yields the best results. It has desirable polarity asymmetry of $J$-$E$ characteristics, i.e., lower leakage current and higher EBD and $Q_{BD}$ when the top electrode is positively biased. Charge trapping characteristics of the N\textsubscript{2}O annealed dielectrics are greatly improved, including a much lower electron trapping rate and a desirable polarity asymmetry of trappings. It is believed that, similar to the N\textsubscript{2}O oxide on monocrystalline silicon, it is the incorporation of nitrogen at the polyoxide/poly-1 interface to result in the suppressed electron trapping and the improvement on $Q_{BD}$. The centroids of trapped charges of N\textsubscript{2}O annealed dielectrics are more away from the polyoxide/poly-1 interface than conventional polyoxides.

The optimized recipe of flat polysilicon and deposited oxide layer has been applied in complete EEPROM devices. It has been shown that the endurance is extended by at least a factor of 10 with respect to the control oxide and previously processed batches. Retention measurement showed no intrinsic charge loss problems.

So the trends, as have been presented on device level indicate, together with the results on capacitor structures, show that the dielectric strength of the developed inter-polysilicon dielectric layer is adequate for EEPROM application, provided that the polysilicon has an optimized flatness and poly1–poly2 edges are avoided as much as possible.

ACKNOWLEDGMENT

The authors wish to thank Dr. C. Cobianu for valuable discussions. The MESA cleanroom staff is kindly acknowledged for their support. Dr. R. Woltjer is kindly acknowledged for reading the final manuscript.

REFERENCES


Johan H. Klootwijk (S’95–M’98) was born in Hengelo, The Netherlands, in 1969. He received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1993 and 1997, respectively. His Ph.D. dissertation dealt with the development, characterization and application of deposited interpoly dielectrics for nonvolatile memories.

In October 1997, he joined the Philips Research Laboratories, Eindhoven, The Netherlands. His present research interests include BiCMOS technologies, SOI/SOA technologies and reliability of thin dielectrics.

Dr. Klootwijk is a member of the IEEE Electron Devices Society.

Herma van Kranenburg was born in Buren, the Netherlands, in 1964. She received the M.Sc. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1988, and the Ph.D. degree, also from the University of Twente, in 1992 for work on materials science of ferromagnetic thin films.

In 1993, she joined the Integrated Circuits Technology, Devices and Reliability Group, MESA Research Institute, University of Twente, as Assistant Professor. Her present research interests include chemical mechanical polishing, advanced metallization, deposition and breakdown behaviour of thin dielectrics, dielectrics for non-volatile memories and reliability aspects of thin film transistors for liquid crystal displays. She also lectures on IC technology.

Hans Wallinga received the M.Sc. degree in physics from the State University of Utrecht, The Netherlands, and the Ph.D. degree in technical sciences from the University of Twente, Enschede, The Netherlands.

At the University of Twente, he was involved in device physics and device characterisation of MOST devices and CCD’s. His research activities gradually also included the design and testing of sampled data, adaptive signal processing. He was appointed Full Professor of semiconductor devices in 1987 and is heading the laboratory on Semiconductor Components with research and education in the areas of IC-process technology, reliability of semiconductor components, and testable design and test of microsystems. He authored and co-authored several papers on diverse microelectronics subjects. An the MESA Research Institute, University of Twente, he is responsible for the research theme: IC-technology, Devices and Reliability. Presently, he is the Dean of the Faculty of Electrical Engineering, University of Twente.

Pierre H. Woerlee received the Ph.D degree in atomic physics from the University of Amsterdam, Amsterdam, The Netherlands, in 1979.

In 1980, he joined Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on electrical transport in ultra small devices. In 1985, he joined the MOS process integration group. He has worked on device physics, modeling and MOS front-end process integration. Since 1992, he is a part-time Professor at the University Twente, where he is teaching IC technology. His research interests are material research, metal CMP, barrier layers and reliability of thin dielectric layers.

Dr. Woerlee received the Paul Rappaport award in 1996. He was general chair of the 1998 IEEE IEDM conference.