Fast Switched Current analog memory

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ABSTRACT

In this paper is presented the structure of a fast Switched Current (SI) analog memory and its integration with a high energy nuclear physics experiment equipment. A special emphasis is focused on the structure of the elementary memory cell, the SI flash A/D converter, and the sampling commands generation. There can be found also a short comparation of the SI and SC techniques for analog memories.

1 INTRODUCTION

The presented analog SI memory is designed to be used as a very fast buffer memory. It will store in parallel, at a high sampling rate the 32 outputs of a silicon drift detector (SDD) used in nuclear high energy physics experiments. The SDD output information sampled at a constant rate and stored in the analog memory is later read and converted to digital form by a SI flash A/D converter and after that processed to recover the time, the intensity, and the space coordinates of particle collision on the SDD.

The main advantage of using a SI analog memory instead of using a more conventional switched-capacitor (SC) one is that the former is cheaper as it is fully CMOS technology compatible. Similar to the operation of dynamic logic circuits, a voltage is sampled on the gate of a MOSFET and held on its non-critical gate capacitance. The held voltage signal on the gate causes a corresponding held current signal in the drain. Another important advantage of the SI over SC approach is that in SI is stored a voltage and is read a current, while in SC is stored and read the same voltage, thus being likely to alter the stored value while reading.
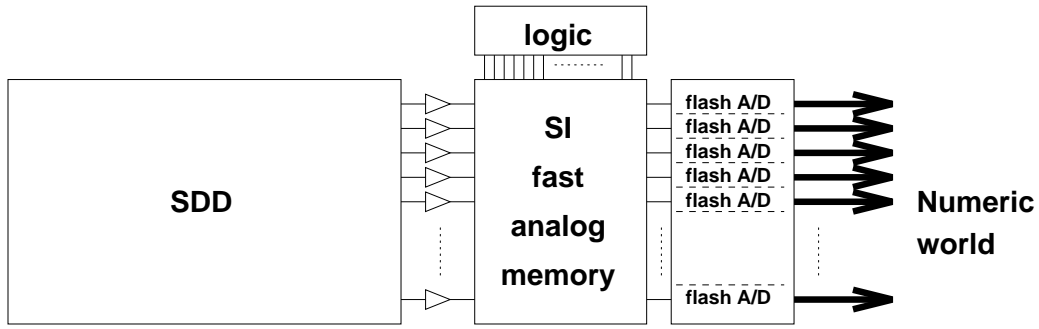
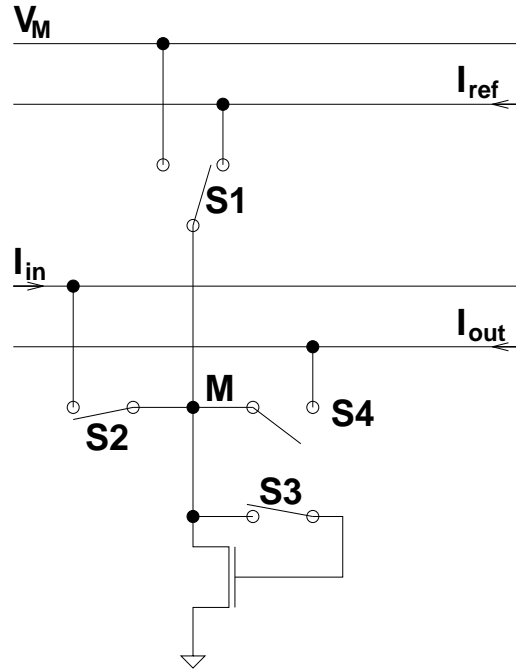Figure 1: Block schematic of the analog part of the detector

Figure 2: Principle schematic of a single memory cell

2 THE STRUCTURE

As reported in figure 1, the structure of the analog part of the data processing for the experiment is composed by four main parts: the SDD, the analog low-noise amplifiers, the analog SI memory (256×32), and the final A/D converter. The SI memory uses an auxiliary digital block which generates the control signals it needs for a proper operation. Next we will focus only on the single memory cell and on the A/D converter principle schematic.

The principle schematic of the memory cell is presented in figure 2. Aiming to be kept as simple as possible, it is composed of a NMOS transistor acting as storage element, four lines carrying different signals, and four switches.

The line I_{ref} is connected to an unique per row current source. This allows to reduce both the power dissipation and the size of the elementary memory cell.

The line V_M has a constant voltage set below the minimum value of the voltage swing of M node
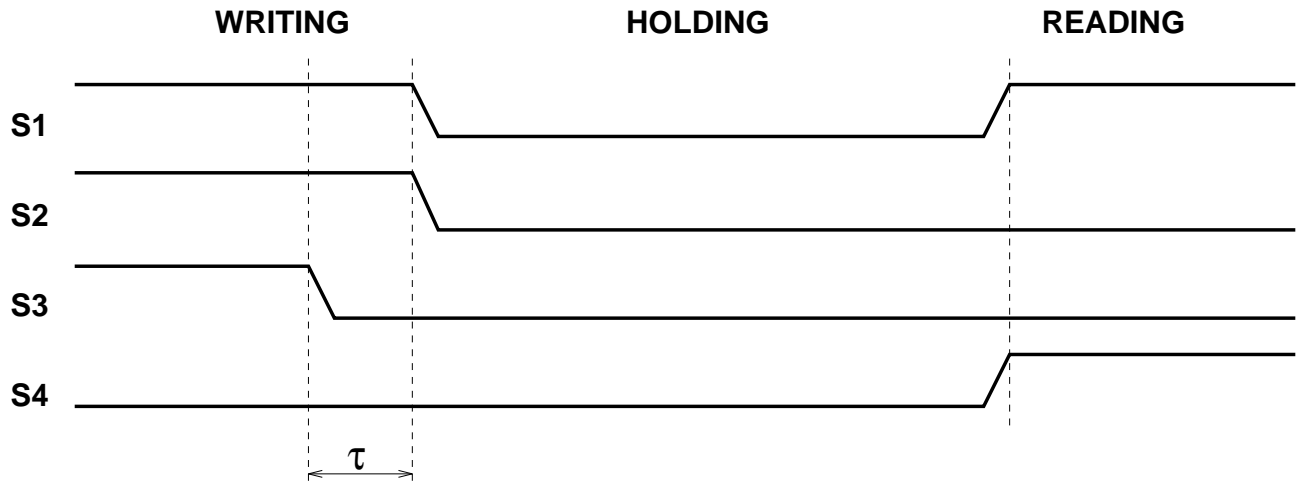
Figure 3: Time diagram for the operation modes of the elementary memory cell
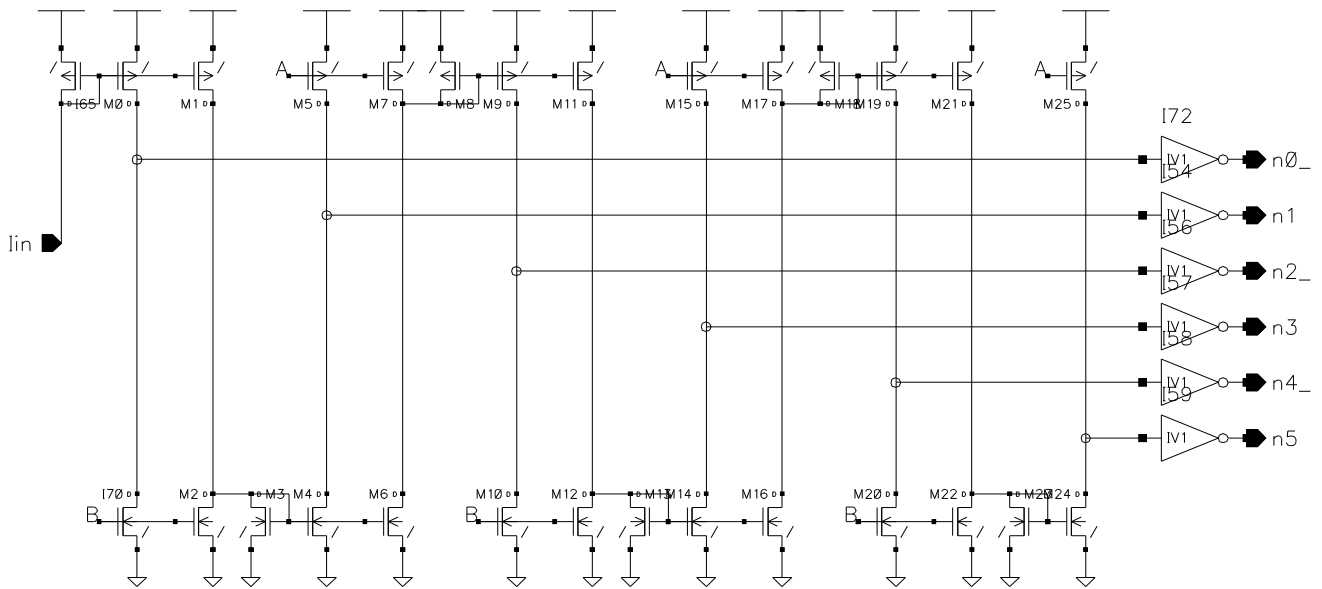

Figure 4: Principle schematic of the flash A/D converter

for normal cell operation. This is one of the precautions taken to avoid storage errors by charge injection on the gate capacitance of the NMOS storage transistor when commuting the cell from one state to another. It was chosen la lower value than the minimum value of the M voltage for V_M line to have no DC current consumption on the memory cell when not selected.

In figure 3 are presented the command signals for the four switches of the memory cell for writing, holding, and reading modes.

A principle schematic of a cost and power consumption effective flash A/D converter is given in figure 4. It is composed of an alternate cascade of complementary stages built of only 5 even-size transistors each (without counting the output inverter). Each stage decodes a digital number unit and that means that the converter size increases linearly with the maximum decoded number. Moreover, it features a very regular structure simplifying the design and compaction of the layout.
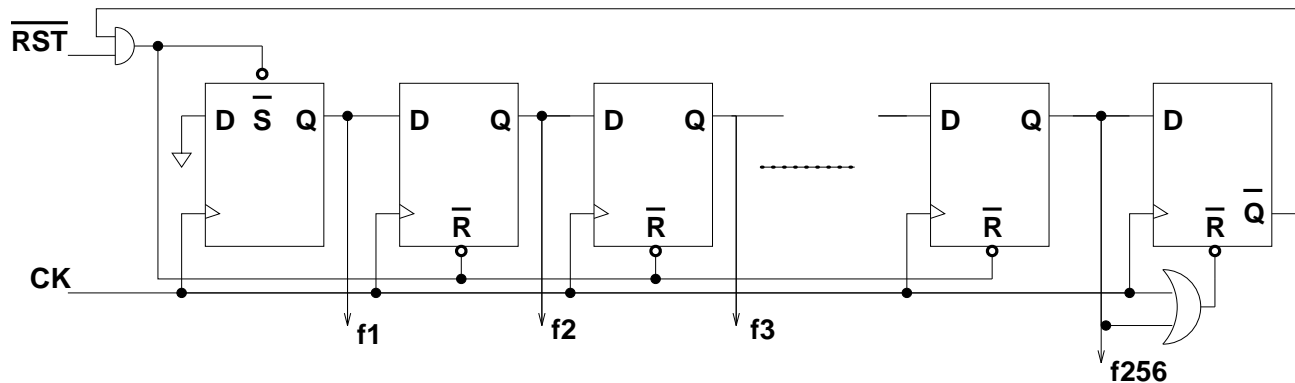
Figure 5: Command signals generator

The transistor M_1 (M_6, M_{11}, M_{16}, etc.) provides the current to be measured to the first (second, third, etc.) stage of the converter. The transistor M_2 (M_7, M_{12}, M_{17}, etc.) subtracts a constant current (corresponding to one unit of the output digital number) from the current to be measured. The subtracted current is imposed by the gate voltage B (A) provided by a common bias block. The resulting current after the subtraction is mirrored by the transistors M_3 and M_4 (M_8 and M_9, M_{13} and M_{14}, etc.) and then compared with the unity current (I_{70}, M_5, M_{10}, M_{15}, etc.). The result is converted to digital level by an inverter. It is to be noted that even number output signals are inverted with respect to the odd number signals. This aspect is to be taken into account when designing the output decoder.

To generate the command signals for the memory cells it is proposed the shift register presented in figure 5. In order to avoid as much as possible the prohibited states with a minimum expense in extra gates we used one additional flip-flop which resets for a half clock period the whole shift register at the end of the shift. This way any but one (i.e. all zeros) prohibited state do not propagate longer than a counting period.

3 CONCLUSIONS

The main problem that is expected when designing an analog memory of this structure is related to the alteration of the hold voltage on the elementary memory cell due to parasitic influence. While charge feedthrough and leakage current of drain and source junction of switches MOS transistors can be compensated in a certain degree, it seems to be very difficult to avoid the errors introduced by the voltage swing of the node M (see figure 2). The swing of node M is due to the different conditions the memory cell is written than read. There has been already provided the V_M voltage to connect the N node while the cell is in hold state to reduce the voltage swing. Another way to improve the holding capacity of the MOS transistor is to use large size transistors.

The command signals generator has the advantage of simplicity while having an implicit built-in

test every new cycle. Unfortunately, there is no way to realize an error state signalization for this block without using a large amount of combinatory logic.

In the design of this structure of SI analog memory it should be made the best trade-off between the memory size, accuracy, power dissipation, and failure signalization.

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