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A Low-cost Emulation System for Fast Co-verification and Debug

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Abstract— A flexible system for SoC co-verification is proposed, built around an Infrastructure Microprocessor (IM), providing improved controllability and observability in a fast self-contained FPGA-based emulation environment. In addition, software debug is supported by enabling observation of critical signals, breakpoint setting and step-by-step execution with total memory accessibility. Experimental results in an industrial case study confirm the effectiveness of the approach for validating and debugging hardware and software.

SUMMARY

Guaranteeing the implementation correctness of today's integrated systems, which may include microprocessor and logic cores as well as several software layers, is becoming a daunting task. Finding design or implementation bugs requires the activation of the devices in functional mode while feeding them with input data and control signals, replicating complex and possible long operating sequences, and observing critical signals. Single hardware modules and small low-level code segments can be efficiently reproduced and analyzed in simulation, employing testbenches, or verified through formal techniques. For larger and more complex systems, simulators can hardly be employed, due to the huge requirements in terms of computational power and time. Emulation represents a viable improvement, enabling faster system behavior replication, but often with reduced system observability [1-6]. Commercial platforms are available for several architectures, based on simulators, emulators and/or programmable hardware, each one offering a specific set of features and possibly introducing a significant setup cost in the design flow.

A co-verification and debug system is here proposed (Fig.1), based on full FPGA emulation of the circuit design and on a dedicated microprocessor-based interface. The emulation environment is self-contained and runs at high speed. Complete controllability on the inspected device is achieved, including I/O signals, clocks and memories, so as to perform hardware validation/verification and supporting software debug, while the development of tests relies on writing high-level code routines. In addition, the adaption to different circuits takes minimal redesign effort, making the system particularly suitable to follow the different development steps of a new complex device. To enable effective use, a supporting software environment was developed, ranging from HDL simulators, ad-hoc flow management tools, up to high-level system models. The platform presented herein extends the capabilities of our previous work [7] by providing additional control and observation features in order to interact more deeply with the emulated system. Also, we demonstrate the possibility of adding purpose-specific verification support modules to the emulation system in order to perform specific tasks, such as bus protocol conversions or noise injection.

The proposed platform has been implemented on a Xilinx Virtex-5 LX development board, using the Xilinx MicroBlaze soft core as IM. It is currently being employed for co-verification and debug of an innovative automotive system under development by Pirelli Tyres [8]. The main integrated device, located inside a car's tire, is intended to acquire accelerometric data from the inner liner and transmit them to the main car body. Such data will then be elaborated and employed for improving braking and stability control systems. The proposed platform enabled performing noise immunity characterization of the implemented DBB radio modules and general system debugging, granting up to a 100x speed-up with respect to RTL simulation.

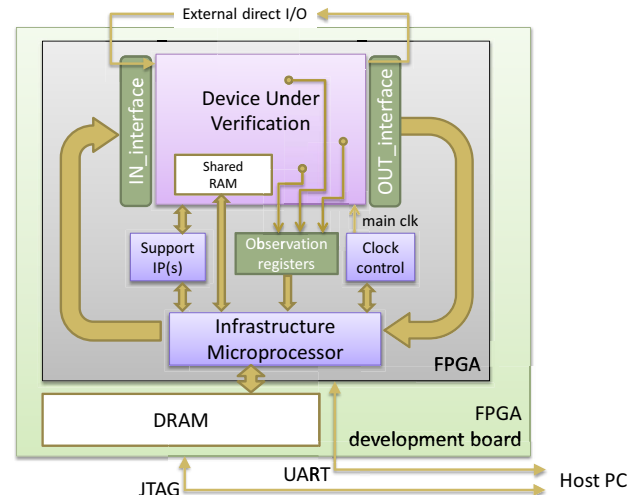


Figure 1. The proposed FPGA-based co-verification and debug platform.

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