# Single and Multi-Piece Behavioral Models of IC Output Buffers

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***Abstract***

*This paper discusses the switching properties of the behavioral models of integrated circuit output buffers. Present behavioral models are based on a two-piece structure defined by a linear combination of two submodels for the two logic states. These models are very accurate in the two logic states, but their state switching is sensitive to the driven loads. The analysis carried out in this paper shows that this load sensitivity stems from the linear combination defining the two-piece model. A new single-piece behavioral model is proposed, that solves this problem and has efficiency and complexity levels comparable to those of two-piece models.*

## Introduction

The modeling of digital Integrated Circuits (IC) input and output buffers is of paramount importance for the assessment of Signal Integrity (SI) and ElectroMagnetic Compatibility (EMC) effects in high-end digital systems. The most effective modeling solution for this problem is based on the development of behavioral macromodels. Two main macromodeling approaches are generally used. The simplest one exploits simplified equivalent circuits derived from the internal structure of the modeled devices, leading to the widely used Input/Output Buffer Information Specification (IBIS) [1]. The second approach, in contrast, is based on the use of parametric relations to approximate the device port equations and on the estimation of the parameters from the device responses [2]. It offers improved accuracy and enhanced modeling capabilities.

These two approaches rely on different modeling concepts, nevertheless, for output buffers, they use the same two-piece model structure based on a linear combination of models for the High and Low logic states. With this structure, the behavior in the two logic states is correctly represented and state switching between voltage levels close to zero and to the power supply voltage are well reproduced. When the switching takes place between two voltage levels that are not close enough to the power supply rails, however, accuracy penalties may arise. A well known example of this effect is a device operating in Stub Series Terminated Logic (SSTL) signaling systems, where switching takes place between voltage levels $V_d/2-\Delta_L$ and $V_d/2+\Delta_H$, $V_d$ being the power supply voltage and $\Delta_L < V_d/2$, $\Delta_H < V_d/2$. Similarly, problems arise in devices performing incomplete state switching, *e.g.*, in overclocked operation. In order to overcome these difficulties, two-piece models with multiple switching rules have already been proposed [3].

In this paper, the state switching process of a two-piece model is thoroughly analyzed, with the aim of pointing out the source of possible errors. A complete numerical example is developed to demonstrate why two-piece models may fail to describe switching between voltage levels not close enough to the power supply rails. Finally, a new single-piece model is proposed, which can overcome the limitations of two-piece models for a moderate increase of the model complexity.

## Two-Piece Models

IC Output buffers (simply drivers in the following) are circuits composed of cascaded inverter stages interfacing IC internal logic with external interconnects. The typical driver structure is sketched in Fig. 1 along with the relevant electrical variables.

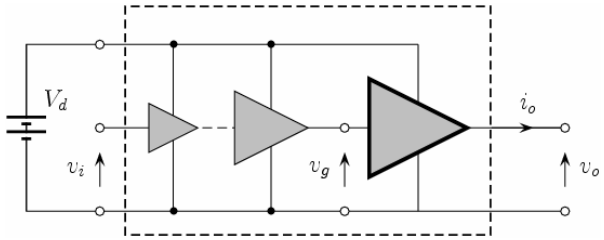


Figure 1: Typical IC output buffer (dashed box) and its main electrical variables. Voltage $v_i$ is the control voltage applied by the IC logic core, $v_o$ and $i_o$ are the circuit output voltage and currents, respectively. The bold triangle symbol indicates the last inverter stage and $v_g$ its input voltage.

A behavioral driver model is a relation between the driver output variables $v_o$ and $i_o$. This relation must also change according to the value of a control variable, in order to describe the operation in the two logic states and the switching between them. Both the circuit based and the parametric modeling approaches solve this problem by a two-piece model representation defined by:

$$i_0 = w_H(t)\, i_H(v_0, dv_0/dt) \quad + \quad w_L(t)\, i_L(v_0, dv_0/dt) \tag{1}$$

where $i_H$ and $i_L$ are submodels accounting for the device behavior in the logic High and Low state, respectively. The switching between the logic states is controlled by the weighting functions $w_H(t)$ and $w_L(t)$ that vary in time, causing transitions between the two submodels. In the two modeling approaches, submodels $i_H$ and $i_L$ are obtained from either equivalent circuit representations or parametric relations and identification methods. The physical meaning of the two-piece assumption and the easy estimation of the model parameters from the port waveforms are the main strengths of this model representation.

The two-piece model representation (1) yields models that are inherently accurate for operation in fixed logic states, because in that condition only one of the two submodels is active. In particular, the use of parametric nonlinear submodels allows to reproduce also complicated device behaviors [2]. Possible inaccuracies arise during state transitions, where (1) must mimic the behavior of the modeled device by using $i_H$ and $i_L$, that contain information on fixed logic state operation only. An example of inaccurate description of state switching is shown in Fig. 2. This example involves the four-inverter-stage CMOS driver defined in [4, pag. 492], for which a Device Level (DL) model is available. This driver is used in all the examples presented in this paper and the response of its DL model is used as the reference against which checking the accuracy of behavioral models. The voltage responses of switching experiments with different loads are shown in Fig. 2. The solid line curves are the driver responses, whereas the dashed line curves are the responses of a two-piece model made by state-of-the-art nonlinear dynamic submodels $i_H$ and $i_L$ [2]. The responses for the two load with the 100Ω resistor are used to estimate the switching coefficients of the two-piece model (see next Section). Model responses are accurate for the loads with the 100Ω resistor and in poor agreement for the other cases. This is a typical situation: two-piece models predict accurate state transitions for loads close to those used in switching coefficient estimation and may be inaccurate for other loads. It is ought to remark that the load with the 2.5V voltage source is typical of SSTL applications and that the error of two-piece models for these loads is a known effect [3].

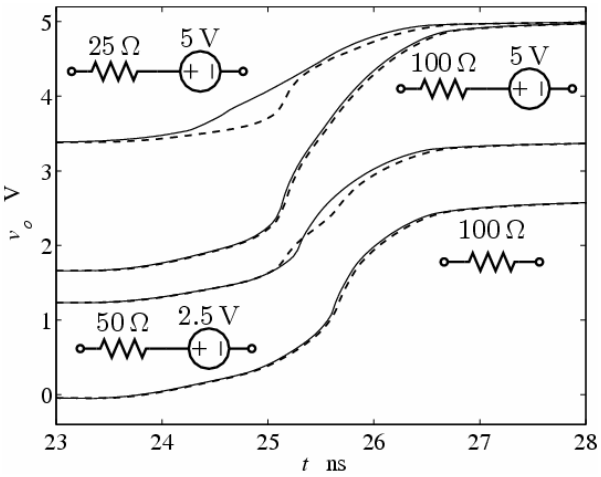


Figure 2: Output voltage waveforms for the example driver (See text) driving different loads. Solid lines: reference responses; dashed lines: responses of a state-of-the-art two-piece model.

**Analysis of State Switching**

In order to address the modeling of buffers during state switching, in this Section we analyze the switching process of the example driver. Figure 3 shows the output voltage waveform produced by the example driver when it applies a logic High pulse to a 100Ω resistor. The solid and dashed lines indicate the driver reference response and the last driver stage DC response, respectively. The DC response is computed by assuming $v_g = v_{gs}(t)$, where $v_{gs}(t)$ is the same $v_g$ waveform that gives rise to the reference response. In other words, the dashed curve is the driver response that would be observed if any dynamical effect were removed from its DL model. Figure 3 highlights that the static response of the last driver stage gives a dominant contribution to shape the edges of the driver responses.

The switching process of our two-piece model is then considered, in order to verify how it reproduces the static behavior of the modeled device during state switching. For such a model, as for most state-of-the-art two-piece models, the coefficients $w_H(t)$ and $w_L(t)$ are estimated by means of the two-waveforms method [5].

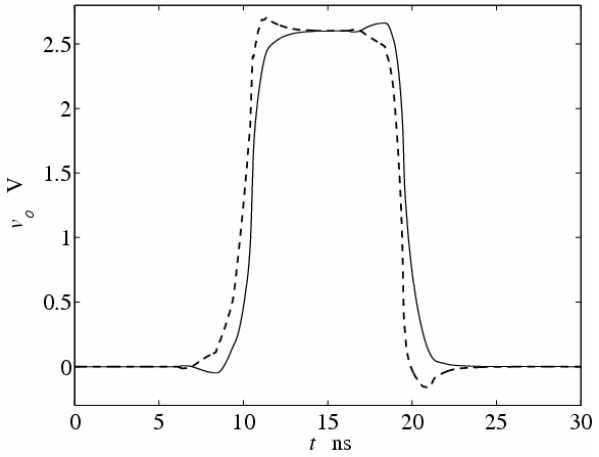


Figure 3: Static contribution to the output voltage for a switching process with a 100Ω load resistor. Solid line: reference; dashed line: static contribution (see text).

In this method, the switching coefficient are the solution of the following linear problem:

$$\begin{cases} i_{0a}(t) = w_H(t)\, i_H(v_{0a}(t)) + w_L(t)\, i_L(v_{0a}(t)) \\ i_{0b}(t) = w_H(t)\, i_H(v_{0b}(t)) + w_L(t)\, i_L(v_{0b}(t)) \end{cases} \quad (2)$$

where $v_{oa}(t)$, $i_{oa}(t)$ and $v_{ob}(t)$, $i_{ob}(t)$ are the driver output waveforms recorded on two different loads during a state switching. The two loads are named *reference loads* and are usually made of a simple resistor (with resistance R) connected to ground or to $V_d$. For our model, the reference load is defined by R=100Ω, as indicated in Fig. 2. The rationale for this method is that it should allow accurate modeling also for $(v_o,i_o)$ values in the region delimited by the two load lines $i_o = v_o/R$ and $i_o = (v_o - V_d)/R$.

The static contribution of the two-piece model during state switchig can be studied by plotting the curves $i_o = w_H(t_k)\, i_{Hs}(v_o) + w_L(t_k)\, i_{Ls}(v_o)$ for some $t_k$ values in the switching time interval. In the above equation, $i_{Hs}$ and $i_{Ls}$ are the static parts of submodels $i_H$ and $i_L$, and they coincide with the v-i curves of the driver in the Low and High states, respectively. The intersection of these curves with the load lines $i_o=v_o/R$ and $i_o=(v_o-V_d)/R$ yield the static contributions of the two-piece model at the selected time instants. The actual static contribution at times $\{t_k\}$ are the intersections of the driver last stage DC characteristics for $v_g=v_{gs}(t_k)$ with the load lines. (It has been verified that the dependence of $v_g(t)$ on the driven load is negligible). The two sets of DC curves, along with the load lines of the reference loads, are shown in Fig. 4. The DC curves of the driver and of the two-piece model intersect along the load lines that are used to compute $w_H(t)$ and $w_L(t)$. However, large differences can be observed in the other regions of the $(v_o,i_o)$ plane. In particular such differences hold in the region between the two load lines, too. This is the region crossed by the load lines of SSTL loads and those differences explain the errors shown in Fig. 2.

The discrepancy between the DC curves of the model and of the driver stems from the structure of the model. In fact, for two-piece models, the DC curves during state switching are a linear combination of the driver v-i curves of the two logic states. However, the DC curves of the driver are more complicated and arise from the nonlinear dependence of the pullup and pulldown currents on the value of $v_g$. In conclusion, the error of two-piece models during state switching arises from the linear nature of their switching mechanism, that cannot reproduce the device DC curves in intermediate states.

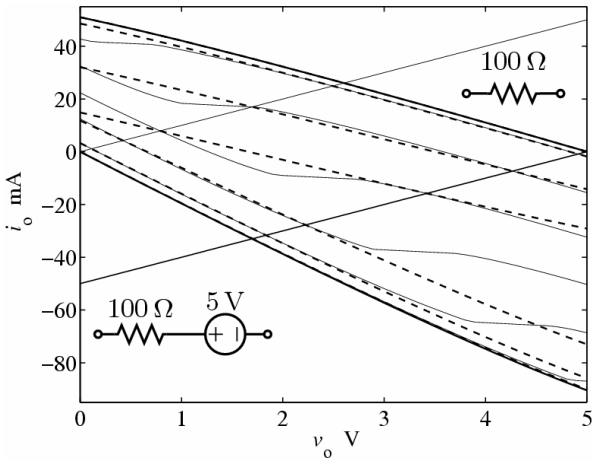


Figure 4: Reference load lines, driver (solid lines) and two-piece model DC output curves (dashed lines, see text for details). The driver and model curves intersect along the reference load lines only.

The assesment of accuracy penalty caused by the error on DC curves is particularly difficult, because it depends on the shape of the curves and on the region of the $(v_o,i_o)$ plane explored by responses. A good pratice would be to provide two-piece models (including those developed from IBIS data via the two-waveform method) with a $(v_o,i_o)$ domain of guaranteed accuracy. In any case, the accurate simulation of state switching is of paramount importance for the timing analysis of digital designs. As an example, Fig. 5 shows the edges of the driver and the two-piece model responses for a load composed of a 100Ω resistor and a 10pF shunt capacitor. The timing error of the model is significant with respect to the switching time, and therefore important for the timing analysis. Again

this error can be explained by the model error on the DC curves in intermediate states, because the trajectory of this responses crosses regions of the plot of Fig. 4 where the DC error is large.

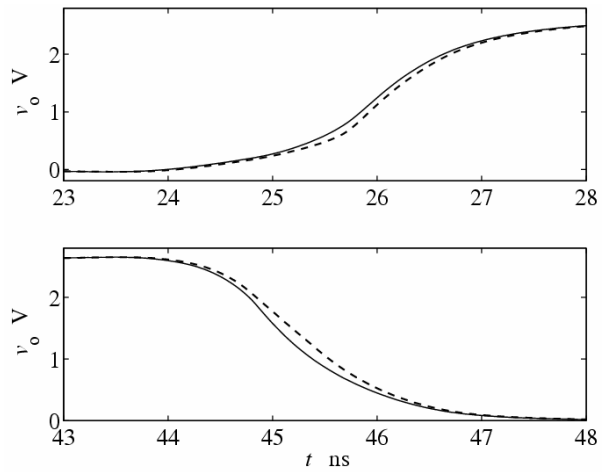


Figure 5: Edges of the driver voltage responses for an RC load. Solid line: reference; dashed line: two-piece model.

**Single-Piece Model**

In this Section, the development of a single-piece model is addressed. The discussion developed is aimed at assessing the feasibility of the model, and assumes that all the driver internal variables are accessible.

Different single-piece models can be devised to relate the output variables of drivers. Here we concentrare on the simplest one, *i.e.*, a model defined by a representation composed of a static and a dynamic part:

$$i_0 = i_{os}(v_0, v_g) + i_d(v_0, v_g) \qquad (3)$$

where $i_{os}$ is the DC output characteristic of the driver and $i_d$ is a dynamic model accounting for the difference between the actual response and the static one. The dynamic part is defined null for constant $v_o$ and $v_g$ waveforms, so that any DC contribution to $i_o$ is included in $i_{os}$. Representations with splitted static and dynamic parts have been already exploited in two-piece models [2]. Their main advantage is a facilitated estimation of the dynamic part parameters, as the information on the static behavior is completely contained in the static part. In (3), $i_{os}(v_o,v_g)$ reproduce the DC curves of Fig. 4 completely, thereby eliminating the error of the two-piece model on the DC contribution in intermediate states.

In order to obtain a driver output model, a control variable defining the logic state of the model and driving the switching process must be also defined. The most natural control variable for model (3) is the driver last stage input voltage $v_g$. For $v_g=V_d$ and $v_g=0$ the DC characteristic of the Low and High logic states are selected, respectively, whereas intermediate $v_g$ values lead to intermediate states. In our model, therefore, the role of coefficients $w_H$ and $w_L$ of the two-piece models is played by a suitable $v_g(t)$ waveform. In actual operation, $v_g(t)$ is decided by the circuits preceding the last stage and by the backward transmission properties of the last stage. However, the backward transmission of inverter stages is weak, and is neglected in this approach. For the problem at hand, it has been verified that $v_g(t)$ weakly depends on the driven loads. In conclusion, the proposed model is defined by (3) and by function $v_{gs}(t)$ (see previous Section), controlling the logic state and state switching.

The generation of a model based on (3) mainly amounts to generating the dynamic part $i_d$, *i.e.*, to selecting a suitable representation of $i_d$ and to estimating its parameters. The dynamic part id would be well represented by a nonlinear dynamic relation. However, in order to verify the feasibility of this approach, we try a simple linear dynamic representation, *i.e.*, an ARX model. We build the estimation data set for this model by applying $v_{gs}(t)$ to the last driver stage while it drives a transmission line load. The transmission line reflections excite the output port dynamic behavior. This allows to estimate $i_d$ parameters via a standard algorithm by using $v_{gs}$, $v_{oe}$ and the difference current:

$$i_{de}(t) = i_{oe}(t) - i_{os}(v_{oe}(t), v_{gs}(t)) \qquad (4)$$

where $v_{oe}(t)$ and $i_{oe}(t)$ are the output driver waveforms recorded in the switching experiment with the transmission line load.

In our example, the transmission line load is composed an ideal transmission line with 50Ω characteristic impedance and 3ns time delay terminated by a 10pF capacitor. The estimated ARX model has dynamic order equal two, *i.e.*, it is composed of six terms. The voltage signals used to estimate the parameters of this model are shown in Fig. 6.

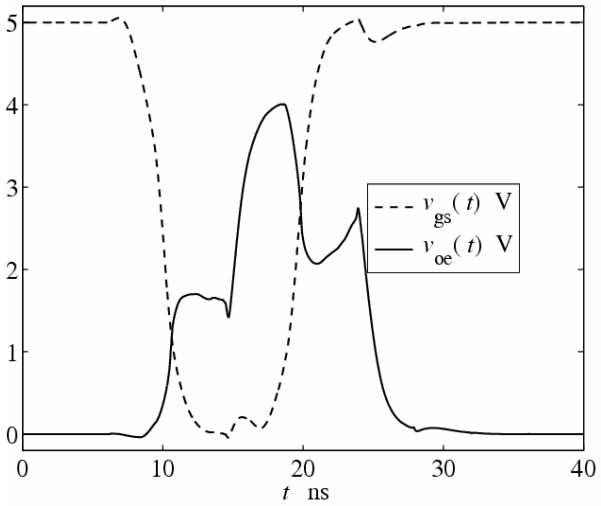


Figure 6: Voltage signal involved in the estimation of the parameter of the dynamic part of (3), *i.e.*, the last driver stage input voltage and the output voltage recorded for a transmission line load (see text).

The single-piece model obtained in this way has been extensively tested to verify its properties and performance. Figure 7 shows the results of a cumulative test, obtained by driving a load composed of the series connection of a 100Ω resistor and of a noisy voltage source. The voltage source also applies large pulses while the driver is in the two logic states. The voltage responses of this test circuit for the driver and its single-piece and two-piece models are shown. The responses predicted for the large pulses demonstrate the ability of the single-piece model to perform as the two-piece model in describing driver operation in fixed logic state. In this test, the large pulse response of the two-piece model is slightly more accurate than the response of the single-piece model. This is consistent, because submodels $i_H$ and $i_L$ are of nonlinear dynamic type, whereas we use a simple ARX model for $i_d$ of (3). Nonetheless the wide pulse response of the single-piece model is good and can be improved by using a nonlinear dynamic model for $i_d$ as well.

The edge part of the responses of Fig. 7 demonstrates the key feature expected from a single-piece model, *i.e.*, its ability to describe state transitions for arbitrary loads. The edge predicted by the single-piece model, in fact, is in good agreement with the driver response, whereas the edge predicted by the two-piece model is in poor agreement. This confirms that the proposed model overcomes the limitations of two-piece models.

Single-piece models have the potential to describe incomplete state transition as well. This feature would allow to simulate designs for operating condition exceeding nominal values and it is highly desired. In principle, approximations of the $v_g$ waveforms occurring in incomplete state transitions can be built from $v_{gs}(t)$ and $v_i(t)$. These approximations automatically give rise to the responses for incomplete state transition.

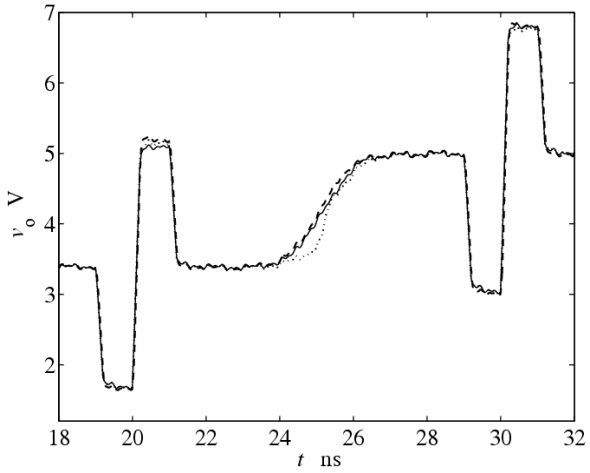


Figure 7: Voltage responses for a load composed of the series connection of a 100Ω resistor and of a noisy voltage source. Solid line: reference; dashed line: single-piece model; dotted line: two-piece model.

A final comment on implementation and efficiency issues is in order. Two-piece models require the implementation of two dynamic submodels, two v-i curves and two switching functions of time. The proposed single-piece model requires the implementation of a dynamic part (whose complexity is comparable to the one of the submodels composing two-piece models), one set of v-i curves and one switching function of time. The most costly part is the implementation of the set of v-i curves, that, however can be efficiently done via sigmoidal functions. In conclusion, the execution time of the single-piece model is expected to be comparable to the one of two-piece models.

**Conclusions**

The switching process of two-piece models of drivers is analyzed. It is pointed out that the main source of errors of the two-piece model is the linear combination of the defining submodels. In fact, such a combination hardly accounts for the nonlinear nature of the driver output characteristic during state switchings and may fail to predict the switching behaviors. The feasibility of a single-piece model is addressed by developing a model composed of the output DC characteristic of the last driver stage and of a dynamic linear model. The logic state of this model is controlled by a variable that mimics the input voltage of the last driver stage. The obtained model turns out to be accurate also during state transitions and has a complexity comparable to the one of two-piece models.

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