

Macromodeling of IC output buffers from in-place measurements

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Abstract – This paper addresses the development of accurate and efficient macromodels of the output ports of digital integrated circuits. The proposed approach is based on the estimation of mathematical parametric relations reproducing the external behavior of devices from transient port voltage and current responses recorded during the normal activity of the IC. The efficiency of the approach is demonstrated on a real device via numerical simulation, also for model estimation based on noisy measurements.

Keywords – Digital IC ports, Macromodels, Behavioral models, Identification.

I. INTRODUCTION

Nowadays, the design of high-speed digital systems along with the time-to-market constraints require the assessment of SI/EMC effects at the early stage of the design process. Such an assessment, achieved by the simulation of signals propagating on critical nets, relies on the availability of accurate and efficient models of the ports of digital integrated circuits (ICs) that act as the nonlinear terminations of interconnects.

As an example, Figure 1 shows the typical structure of a digital output buffer with the main IC blocks and the relevant electrical variables. For the structure shown in Fig. 1, a macromodel for the output buffer is represented by a suitable nonlinear dynamic relation between voltage v and current i of the device port.

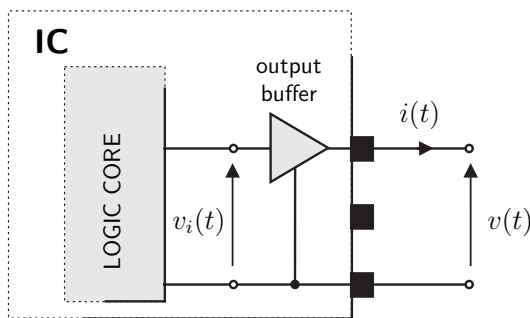


Fig. 1. Typical structure of a digital IC with the main blocks and the relevant electrical variables.

Different approaches are in use to obtain macromodels.

The most common approach is based on simplified equivalent circuits derived from the internal structure of the modeled devices. This approach leads to the I/O Buffer Information Specification [1], that is widely supported by EDA tools and dominates modeling applications. More recent approaches are based on the use of parametric relations to approximate the device port equations and on the identification of their parameters from device responses [2], [4], [5]. These approaches offer enhanced modeling capabilities, that facilitate and improve the modeling of recent devices, like preemphasis drivers [6].

For both approaches, however, the generation of macromodels requires the availability of transistor-level models of the device, or the capability to control the device operation, *i.e.*, the use of dedicated test fixtures to stimulate and measure specific device behaviors. As an example, the estimation of parametric models exploits port responses recorded while the buffer is forced (*e.g.*, through the internal logic signal v_i in Fig. 1) in a fixed logic state or is forced to perform complete state switchings [2]. In real devices with complex logic cores, output buffer states can be hardly controlled and model generation from measured data becomes unpractical.

In this paper, we propose a new modeling technique for the generation of parametric models from responses recorded during regular operation of the device. The advocated procedure is aimed at allowing the modeling of devices from actual measurements, avoiding the need of dedicated test fixtures and device control. The final goal of the proposed approach is the generation of macromodels from responses measured on devices mounted directly on the board, while they operate in normal conditions. The feasibility of the approach is thoroughly discussed and its sensitivity to measurement noise is also assessed.

II. MODEL STRUCTURE AND ESTIMATION PROCEDURE

Parametric macromodels of the output ports of digital ICs like the one shown in Fig. 1, exploit the following two-piece parametric relation

$$i(t) = w_H(t)i_H(v, d/dt) + w_L(t)i_L(v, d/dt) \quad (1)$$

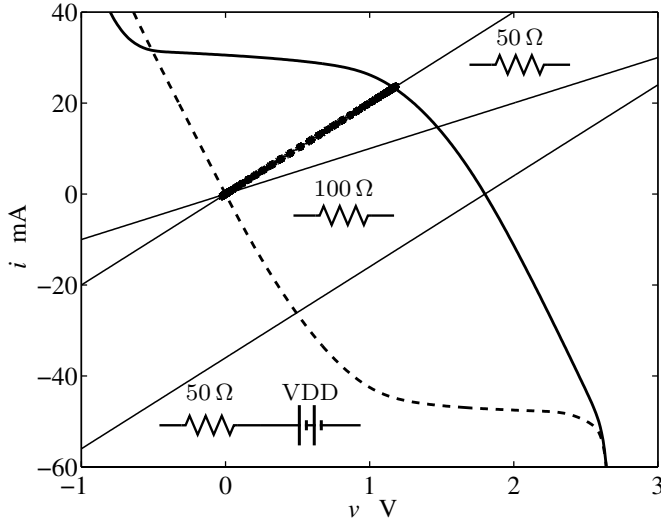


Fig. 2. Static characteristics of the example driver in fixed high state (solid thick line) and low state (dashed thick line) superimposed to the characteristics of three lumped resistive loads and to the samples $\{v(t), i(t)\}$ of the port transient response in Fig. 3 (star line).

where w_H and w_L are switching signals accounting for the device state transitions and playing the same role of the internal voltage v_i in Fig. 1, and i_H and i_L are nonlinear parametric relations expressed in terms of sigmoidal expansion and accounting for the device behavior in fixed logic high and low states, respectively. More details on the model representation (1) and on the use of parametric relations for the modeling of IC ports can be found in [2] and references therein, where a detailed discussion on the derivation of model equations and on the estimation of model parameters are presented.

The estimation of model (1) amounts to computing the parameters of submodels i_H and i_L and the weighting signals w_H and w_L from suitable port voltage $v(t)$ and current $i(t)$ responses. Model parameters are computed by minimizing suitable error functions between the model responses and the measured port responses, that are used as references to be fitted. The objective of this work is to obtain port responses suitable to parameter estimation from devices responses during normal logic operation. To this end, the device responses that can be obtained by driving different loads are studied. For the sake of simplicity, the discussion is based on the output port of a commercial Texas Instruments transceiver, whose HSPICE transistor-level description is available from the official website of the vendor. The example device is a 8-bit bus transceiver with four independent buffers (model name SN74ALVCH16973, power supply voltage $V_{DD} = 1.8\text{ V}$). The example device operates at 167 Mbps, *i.e.*, the bit time is 6 ns, and is driven to produce a 2048 long pseudo-random bit stream. The HSPICE simulations of the transistor-level model of the driver are assumed as the reference curves hereafter.

As an example, Fig. 2 shows the static characteristics of the example device superimposed to the characteristics of three simple lumped resistive loads. Fig. 2 also shows the points

$\{v(t), i(t)\}$ explored by the transient voltage and current signals recorded while the example device drives a $50\ \Omega$ load as shown in Fig. 3. The above figure highlights that simple lumped loads confine the response to a very limited region of the voltage-current plane, that is close to the static characteristic. Responses of this kind have limited information on the device behavior and can hardly be used for the estimation of submodels in (1).

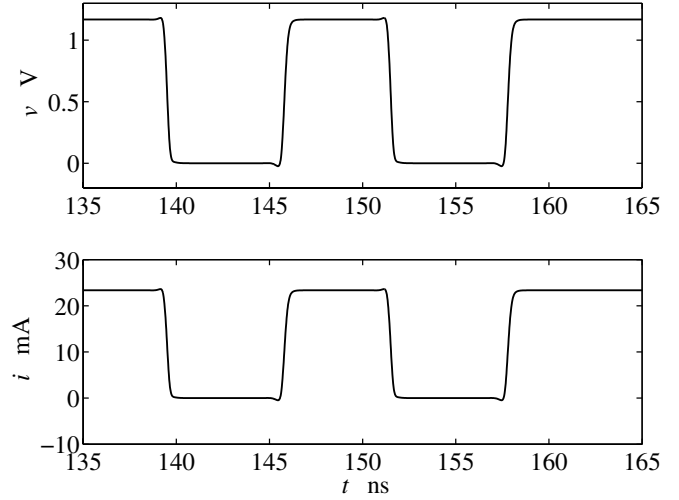


Fig. 3. Port voltage $v(t)$ and current $i(t)$ responses computed for the example driver connected to a $50\ \Omega$ resistor.

In order to generate port responses carrying more information on both the static and dynamic behavior of the port, a distributed load must be considered. Figure 4 shows the port static characteristics superimposed to the points $\{v(t), i(t)\}$ explored by the transient voltage and current signals recorded while the example device is connected to an ideal transmission line load (characteristic impedance $Z_0 = 50\ \Omega$, time delay $T_d = 2\text{ ns}$) loaded by a 10 pF capacitor, as shown in Fig. 5. From Fig. 4 it is clear that port responses of this class are good candidates to be used for the estimation of model parameters, since they explore a wide region of the solution space.

These observations suggest the following two-steps procedure for the estimation of model (1) from port responses during normal logic activity:

(i) *Estimation of submodels.* As already done in [2], the parametric models used for i_H and i_L in (1) are discrete-time parametric representations based on sigmoidal expansions [8] (standard algorithms like [9] are used for parameter estimation). The port responses used to feed the estimation algorithm are parts of the transient curves shown in Fig. 5. In particular, the responses for the estimation of submodel i_H , *i.e.*, the submodel accounting for the information of the port behavior in fixed High logic state, are the solid thick parts of the signals $v(t)$ and $i(t)$ in Fig. 5. These signals are obtained by considering the slice of the port responses recorded while the device is kept through the internal (non-accessible) input signal v_i in the fixed High state for the larger number of consecutive logic

ones. In a similar way, the responses for the estimation of submodel i_L are the dashed thick parts in Fig. 5, recorded while the device is kept in the fixed Low state by means of consecutive logic zeros of the input signal v_i . As an additional remark, it is worth noting that the estimation procedure is facilitated by using the auxiliary input/output variables (x_1, x_2) defined by the following linear transformation of the (v, i) variables.

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 1 & -50 \\ 1 & 50 \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} \quad (2)$$

Such a choice arises from the symmetry of the state transitions of the $\{v(t), i(t)\}$ points in Fig. 4 along directions parallel to the characteristic (not shown in the Figure) defined by the characteristic impedance of the line $i = v/Z_0$. In contrast to the classical port electrical variables, transformation (2) leads to nearly the same range of the new input variable x_1 for both submodels, thus allowing the complete model equation (1) to be always defined. As an additional strength, the above transformation reduces the nonlinearity of the static characteristics of clamps and benefits the quality of estimated models.

(ii) *Computation of weighting signals.* Once the submodels i_H and i_L are completely defined, the weighting signals w_H and w_L are estimated by simple linear inversion of equation (1) from port voltage and current responses recorded while the device is connected to simple lumped loads like the $50\ \Omega$, as in the signal set of Fig. 3. The computation of the weighting signals is a well established procedure and all the details can be found in [2].

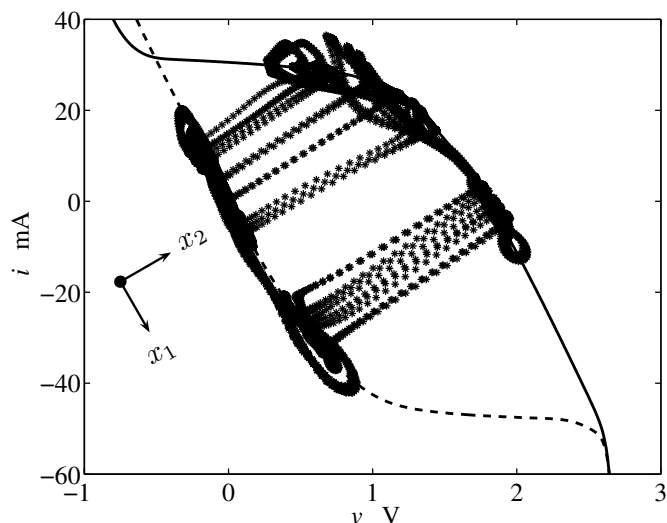


Fig. 4. Static characteristics of the example driver in fixed high state (solid thick line) and low state (dashed thick line) superimposed to the samples $\{v(t), i(t)\}$ of the port transient response recorded while the driver is loaded by transmission-line load (star line).

It is ought to remark that, in order to generate macromodels from in-place measurements, estimation signals for both submodels and switching functions must be obtained from device responses while they drive normal interconnects. This is rather

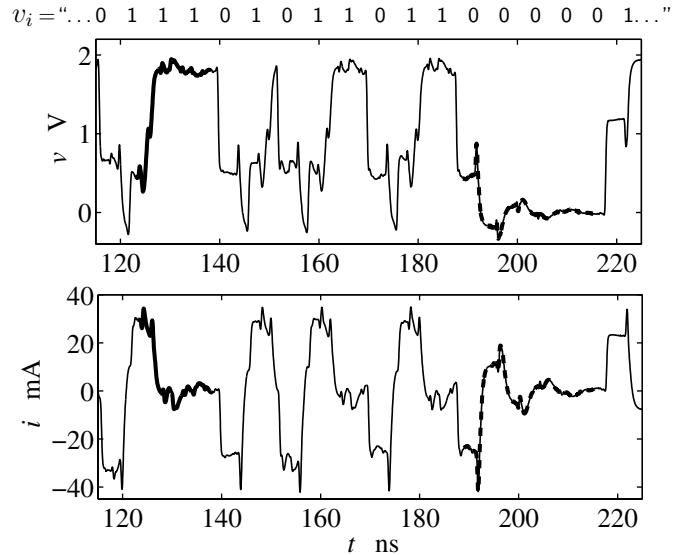


Fig. 5. Output port voltage $v(t)$ and current $i(t)$ responses computed for the example driver connected to an ideal transmission line load (characteristic impedance $Z_0 = 50\ \Omega$, time delay $T_d = 2\ ns$) loaded by a $10\ pF$ capacitor. The thick parts of the $v(t)$ and $i(t)$ signals are the waveforms used for the estimation of the submodels i_H and i_L in (1) (see text for details).

easy for the responses devoted to submodel estimation, as any stub added on board can give rise to signals similar to those used in this study. In contrast, the estimation of the switching functions from state transition responses measured in-place are presently under study.

Finally, the last step of the modeling process amounts to converting the macromodel equation (1) into a form that can be plugged into commercial simulation environments like Analog Mixed-Signal tools or standard circuit simulators like SPICE for the assessment of SI/EMC effects. For the first class of tools, such a conversion is simply based on the direct equation description via metalanguages like VHDL-AMS or Verilog AMS. Instead, for the latter class of circuit simulators, the conversion is carried out by means of a standard procedure by converting the equation into an equivalent circuit and by implementing the equivalent as a SPICE-like netlist as detailed in [2].

III. RESULTS

In this Section, the macromodel estimated for the example device of this study is validated by comparing its static characteristics and transient responses to suitable test loads with those obtained from the reference transistor-level model of the example driver. All the responses of the reference model and of the SPICE-type implementation of the macromodel are computed by means of HSPICE.

As a first test, Fig. 6 shows the comparison of the actual static characteristics of the device compared to the static characteristics of submodels i_H and i_L estimated by the proposed

procedure. This comparison confirms the accuracy of estimated models to capture the static information of the device. Besides, Fig. 7 shows part of the port voltage waveform $v(t)$ computed by the reference transistor-level model and by the macromodel and recorded while the driver is connected to a distributed load different from the one used in the estimation process. The validation load is an ideal transmission line (characteristic impedance $Z_0 = 50\Omega$, time delay $T_d = 1\text{ ns}$) loaded by the connection of a 100Ω resistor and a 5 pF capacitor. The comparison in Fig. 7 highlights the high accuracy of the complete macromodel running in normal operation conditions.

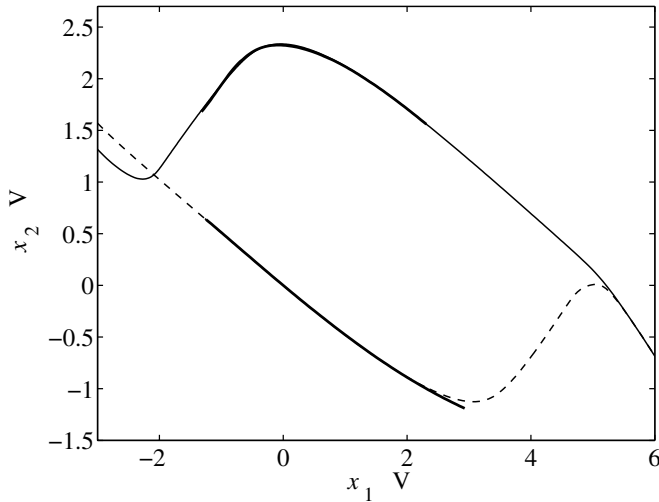


Fig. 6. Static characteristics of submodels i_H and i_L in (1) (solid thick curves) superimposed to the actual characteristics of the example driver in fixed high state (solid line) and low state (dashed line).

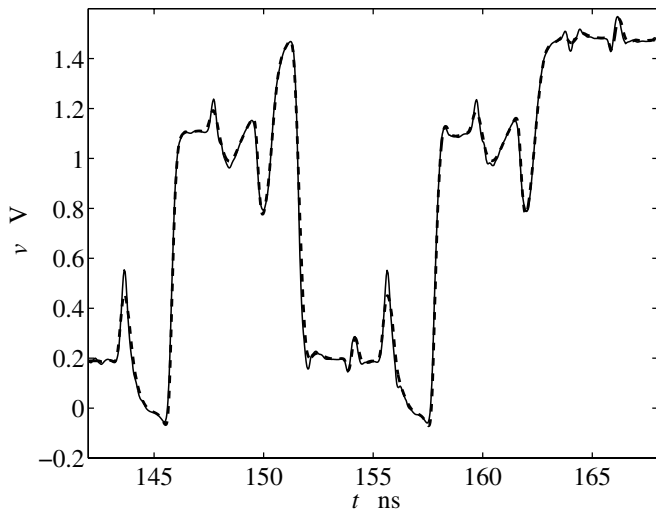


Fig. 7. Port voltage $v(t)$ response computed for the example driver connected to an ideal transmission line load (characteristic impedance $Z_0 = 50\Omega$, time delay $T_d = 1\text{ ns}$) loaded by the shunt connection of a 100Ω resistor and a 5 pF capacitor.

As a second and more realistic test, aimed at verifying the

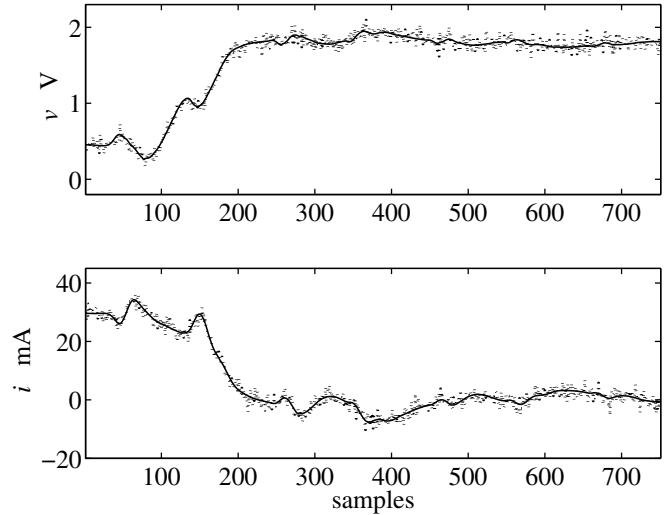


Fig. 8. Port voltage $v(t)$ and current $i(t)$ signals used for the estimation of submodel i_H , i.e., the solid thick signals in Fig. 5, with a superimposed gaussian white noise with standard deviation $\sigma = 4\%$ of the voltage and current swing.

feasibility of proposed approach for the generation of macromodels from actual measurements, the estimation of submodels i_H and i_L has been carried out from noisy measurements. For this second test case, the estimation of submodel parameters is carried out by means of the algorithm [10]. The above algorithm is a modification of the basic version [9] used for the noiseless case in which a suitable penalty function is introduced in the minimization scheme to average the effects of noise and thus to avoid problems of spurious dynamics of estimated models. As an example, Fig. 8 shows the transient responses used for the estimation of submodel i_H that is corrupted by a superimposed gaussian white noise with standard deviation $\sigma = 4\%$ of the voltage and current swing. Figure 9 shows the comparison of the actual static characteristics of the device compared to the static characteristics of submodels i_H and i_L and Fig. 10 shows part of the port voltage waveform $v(t)$ computed by the reference transistor-level model and by the macromodel and recorded while the driver is connected to the same validation load of the previous test. The comparison carried out in this second test highlights the robustness of the proposed estimation procedure and the good accuracy of the complete macromodel estimated from on-line measured data.

IV. CONCLUSIONS

In this paper, a methodology for the development of accurate and efficient macromodels of the output ports of digital integrated circuits is presented. The proposed approach is based on the estimation of mathematical parametric relations reproducing the external behavior of devices from transient port voltage and current responses recorded during the normal activity of the ICs. The advocated procedure is aimed

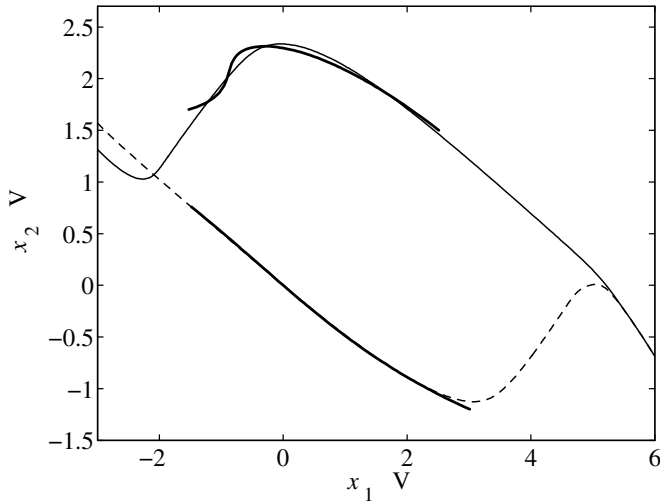


Fig. 9. Static characteristics of the submodels i_H and i_L in (1) estimated from noisy signals (solid thick curves) superimposed to the actual characteristics of the example driver in fixed high state (solid line) and low state (dashed line).

at allowing the modeling of devices from actual measurements, avoiding the need of dedicated test fixtures and device control. The efficiency of the approach is demonstrated on a real device via numerical simulation, also for model estimation based on noisy measurements.

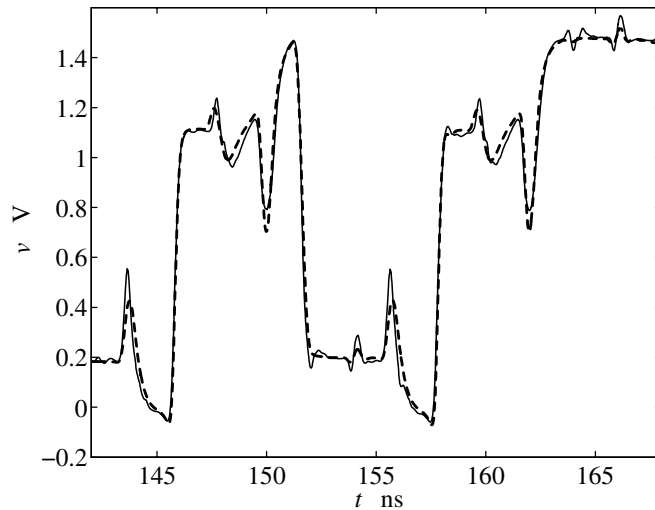


Fig. 10. Port voltage $v(t)$ response computed for the example driver connected to an ideal transmission line load (characteristic impedance $Z_0 = 50\Omega$, time delay $T_d = 1 ns$) loaded by the shunt connection of a 100Ω resistor and a $5 pF$ capacitor. Solid line: reference, dashed line: macromodel estimated from noisy signals.

Acknowledgements This work was supported in part by the Italian Ministry of University (MIUR) under a Program for the Development of Research of National Interest (PRIN grant #2004093025).

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