BEHAVIORAL MODELING OF IC OUTPUT BUFFERS: A CASE STUDY

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ABSTRACT

This paper addresses the behavioral modeling of IC output ports by means of nonlinear parametric relations and system identification methods. The approach is applied to a commercial device and a systematic discussion of the impact of the modeling setup on the model performance is presented.

1. INTRODUCTION

Behavioral models of IC buffers are of paramount importance for the simulation of Signal Integrity (SI) and electromagnetic compatibility effects in fast digital circuits. Recently, behavioral models based on parametric relations and system identification methods have been proposed and successfully exploited in practical applications [1, 2]. These models have inherent accuracy advantages over traditional behavioral models based on simplified equivalent circuits, whereas they maintain a very good numerical efficiency.

The generation of a model based on parametric relations amounts to estimating its parameters so that an error function between the model output and the output of the buffer being modeled (*i.e.,* the estimation waveform) is minimum. The major difficulty of this process is that, due to the nonlinear nature of the problem, there are no general rules for the choice of the estimation waveform and of the modeling setup (*e.g.,* number of samples, sampling time, estimation algorithm, model representation etc.). Usually these choices are carried out via empirical guidelines [4] and the model estimation is rather easy. However a systematic study of the effects of the modeling setup can help to improve the model quality and can facilitate the model generation for those devices that exhibit nonlinear or dynamic behaviors difficult to reproduce. This paper focuses on the modeling of a commercial device with a pronounced nonlinear dynamic behavior and uses the results of this study to address the effects of the modeling setup on the final model.

2. MODEL STRUCTURE

Behavioral models of output buffers are two-pieces representation, where two separate parts account for the device behavior in fixed logic state, and time varying linear coefficients provide the information on state switching. For a single-ended output buffer this writes

$$i(t) = w_H(t) i_H(v, v_{dd}, t) + w_L(t) i_L(v, v_{dd}, t) \qquad (1)$$

where i is the buffer output current, v the output voltage, i_H and i_L the two parts (submodels) describing the behavior in the two logic states, and w_H and w_L the two switching coefficients. Symbol v_{dd} indicates the power supply voltage, included in the model as an example of supplemental input. It is worth noting that, for a given device, the above model can be estimated from port voltage and current responses only, without involving any device internal signal. More details on model structure (1) and on the estimation of its parameters are in [1, 2].

In order to build a model like (1), submodels i_H and i_L must be properly represented, their parameter estimated by fitting the estimation waveforms and, finally, the weighting coefficients w_H and w_L computed. This paper focuses on submodels i_H and i_L by considering different possible representations and parameter estimation methods.

In this work, submodels i_H and i_L are sought for as discrete-time input/output nonlinear parametric relations

$$y(k) = f(\Theta\,;\,\mathbf{x}(k)) \qquad (2)$$

where k is the discrete-time variable ($t = kT$, being T the sampling period), y is the model output variable, vector Θ collects the unknown model parameters, $\mathbf{x}$ collects samples of the model input and output variables and $f(\cdot)$ is expressed as sum of suitable basis functions. Vector $\mathbf{x}$ is named regression vector and has the general form

$$\begin{aligned}\mathbf{x}(k) = [\, & y(k-1), ..., y(k-r), \\ & \mathbf{u}^T(k), ..., \mathbf{u}^T(k-r)\,]^T\end{aligned} \qquad (3)$$

where $\mathbf{u}$ is the vector of the input variables and index r is referred to as the dynamic order of the model. Different sets of basis functions can be exploited to define $f(\cdot)$, like expansions in linear and nonlinear basis functions [2]. Among representation defined by nonlinear basis functions, those involving sigmoidal function (Sigmoidal Basis Functions SBF) [6] turned out to be particular effective for the modeling of IC output ports.

Submodels i_H and i_L can be also represented as a sum of a nonlinear static part and a nonlinear dynamic part with null

static contribution [5], *e.g.,*

$$i_H(t) = f_{sH}(v, v_{dd}) + f_{dH}(v, v_{dd}, t) \qquad (4)$$

where f_{sH} and f_{dH} are the possible static and dynamic parts of the submodel, respectively [4]. The static part can be easily obtained from measurements, whereas representation (2) can be used for f_{dH}. In this case, the output variable is $y(k) = i_H(k) - f_{sH}\left(v(k)\right)$ and the vector of input variables is $\mathbf{u}(k) = [\, v(k), v_{dd}(k) \,]^T$. This splitted representation of submodels turns out to have practical advantages, as it facilitates the estimation of f_{dH} and leads to better models.

3. MODELING SETUP

In this Section, we discuss the effects of the modeling setup on the estimation of submodels i_H and i_L defined by (2) and (4). The following elements of the estimation process are addressed.

a. Model representation
Representation of (2) defined by linear Auto Regression with eXtra input (ARX) parametric models, and by sums of sigmoidal basis functions (SBF) are considered [4]. These representation writes

$$y(k) = \Theta^T \mathbf{x}(k) \qquad (5)$$

and

$$y(k) = \sum_{n=1}^{p} \alpha_n \tanh\left(\mathbf{v}_n^T \mathbf{x}(k) + b_n\right) \qquad (6)$$

respectively. In the above equations, p is the number of basis functions (size of the model), α_n is a linear coefficients and $\mathbf{v}_n$ and b_n are the nonlinear parameters of the sigmoidal function. Besides, these representation are exploited either for the entire submodels or for their dynamic parts only, as in (4).

b. Estimation algorithms
Different estimation algorithms are available for the different model representations. The estimation of linear ARX models (5) relies on simple and efficient algorithms based on the solution of a standard least mean squares problem [7]. On the other hand, the estimation of nonlinear SBF models (6) requires the solution of a fully nonlinear problem. Among possible methods, we found good results by Levenberg-Marquardt based methods [6]. Two versions of the above method are considered: one classic version that solves a nonlinear static problem [8], and another one that solves a nonlinear recurrent problem [10]. Besides, variants of these methods including a suitable linear constraint forcing the static parts of f_{dH} and f_{dL} of (4) to be null are also considered.

c. Initialization
Fully nonlinear algorithms are iterative methods and they need a *random* initialization of parameters. Different initializations lead to different solutions, so the initial guess of parameters becomes an extra element affecting the quality of the estimated model.

d. Estimation waveforms
The estimation waveforms are the port voltage stimuli applied to the output (or supply) port of the buffer under modeling (in fixed logic state) and its output current responses. Estimation waveforms must contain as much information on the buffer behavior as possible. Only qualitative guidelines are available for the design of voltage stimuli [4], leading to noisy multilevel signal like those shown in Figure 1. In this study, we consider multilevel signals like those of Fig. 1 with different number of levels and duration of the constant parts. The duration of level transitions is on the order of the device port switching time.

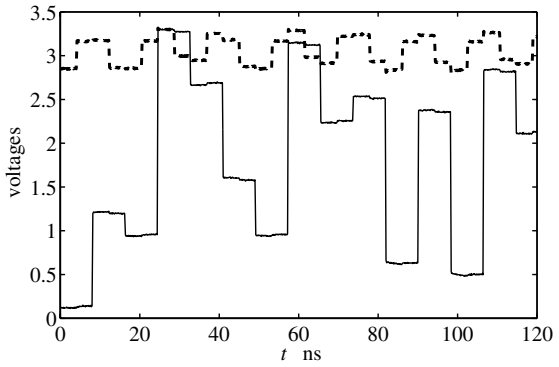

Figure 1: Port voltage stimuli $v(t)$ (solid line) and $v_{dd}(t)$ (dashed line) applied to the output and supply ports of the example driver forced in fixed high logic state.

4. NUMERICAL RESULTS

This Section describes the effects of choices listed in Sec. 3 on the modeling of a commercial device. The example device is the output port of the Philips LVC244 3.3 V CMOS driver. This device shows a significant nonlinear dynamic behavior even for output voltage values in the range of the power supply rails and it defines a stiff modeling example. The reference transistor-level description of this device is available from the official site http://www.semiconductors.philips.com.

In order to simplify the discussion, we focus on submodel i_H in (1) only, as similar comments hold for the i_L submodel. Two test cases have been devised to highlight separately the effects of each choice listed in Sec. 3.

In this study, the accuracy of models is quantified by computing the Mean Squares Error (MSE) between their responses and the responses of the driver being modeled. The test responses are produced by multilevel signals similar to those of Fig. 1 but different from those used for the estimation of model parameters. As an additional index, quantifying the cost of model generation, the CPU time required by the estimation of models is also reported. Finally, for the example device at hand, the dynamic order r of (3) is set to $r = 2$, since we verified that larger values don't lead to better models.

Test Case 1. This test addresses the modeling setup ele-

ments of a and b of Sec. 3. The estimation waveforms are generated by 8-level stimuli where each level lasts 16 ns, that allows the device to nearly reach steady-state in every level.

Table 1: Model accuracy and model generation time for the different choices of model representation and estimation algorithm (see text for details).

#	f	Static	Estimation	p	MSE	CPU
1.	ARX	yes	[7]	8	8.95e-3	0.3s
2.	SBF	no	[8]	4	1.63e-6	17.6s
3.	SBF	yes	[8]	3	8.46e-7	13.8s
4.	SBF	yes	[8] + con.	4	7.61e-6	20.3s
5.	SBF	yes	[10]	3	6.99e-7	960s
6.	SBF	yes	[10] + con.	8	1.37e-5	1327s

Table 1 collects the main figures of models obtained by using different representations and estimation algorithms. In each row, the model is defined by the expansion used for its dynamic part (ARX or SBF, column 2), by the possible decomposition in static and dynamic part (yes or no, column 3) and by the estimation algorithm used (column 4; "+con." means that the static part of submodel f_{dH} is forced to be null during the estimation process). The fifth column list the model size, *i.e.,* the number of basis functions p of (6) for the case of nonlinear SBF models or the size of the regression vector (3) for the case of linear ARX models (5). Finally, the last two columns report the performance of the estimated models quantified by the MSE index and by the CPU time required for the estimation of the models.

The figures of Tab. 1 highlight that the ARX model has a large MSE value and can hardly reproduce the behavior of the example device. Nonlinear SBF models lead to better accuracy figures. This remark is confirmed by the validation curves of Fig. 2 and 3, that compare the reference output port current response and the responses of the first four models of Tab. 1 for the validation stimuli.

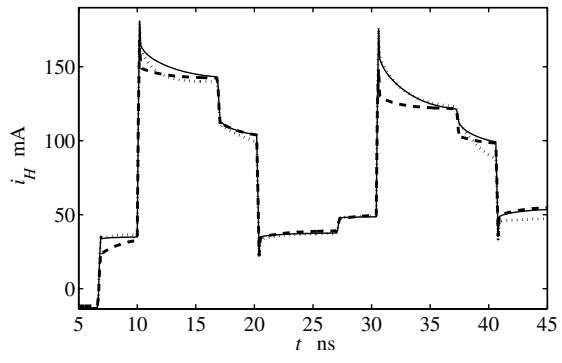

Figure 2: Validation output port current response. Solid line: reference; dashed line: model #1; dotted line: model #2

The SBF models #2, #3 and #4 have comparable MSE values, yet models #3 and #4 that exploit the splitted representation of (4) approximate the steady state values of the validation curves of Fig. 2 better. In addition, Figure 4 compares the device output port static characteristic for the HIGH logic state and the static characteristics of models #2-#4 of Table 1. The same Figure also shows the error curves between the reference and predicted responses. This Figure shows that model #2 roughly approximates the device static behavior outside the range of voltages explored by the port voltage stimuli of the estimation process, whereas models #3 and #4 approximate the device static behavior on a wider range of voltage values better.

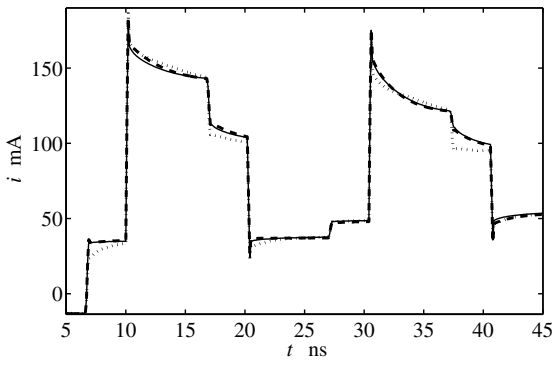

Figure 3: Validation output port current response. Solid line: reference; dashed line: model #3; dotted line: model #4.

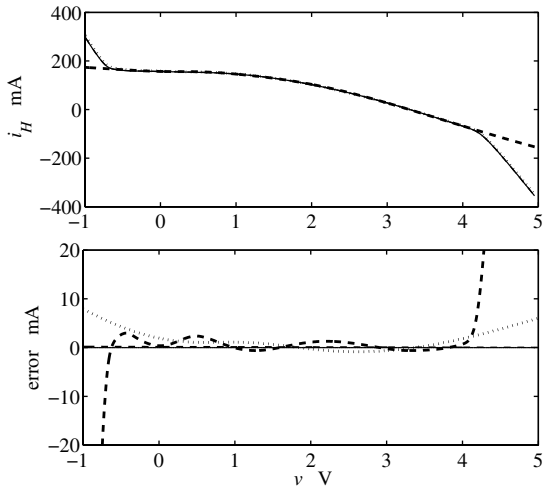

Figure 4: Output port static characteristic i_H (top panel) and error quatified as the difference between reference and predicted curves (bottom panel). Solid thin line: reference; dashed line: model #2; dotted line: model #3; dash-dotted line: model #4.

As a final comparison of this test, an estimation algorithm that solve a recurrent problem [10] is also considered (rows 5 and 6 of Tab. 1). This improved estimation algorithm leads to models that perform nearly as models #3 and #4 estimated by algorithm [8], yet it requires much larger CPU times.

Test Case 2. This test addresses the effects of starting values for parameter estimation and of the spurious static contribution of the dynamic part f_{dH} of the splitted representation (4) (paragraph c of Sec. 3). In this comparison, only models #3 and #4 of Tab. 1 are considered and and the starting values for parameter estimation have been randomly chosen as described in [9].

Figure 5 shows the device output port static characteristic for the HIGH logic state and the static characteristics of models #3 and #4 of Tab. 1. The same Figure also shows the error curves between the reference and predicted responses. The different curves of model #3 are obtained for different runs of the estimation procedure and different parameter initialization. From this Figure, it is clear that the initialization of model parameters weakly affect the quality of estimated models since almost the same order of the maximum error is obtained and that the constrained optimization problem is required for a better approximation of the static behavior of estimated models.

Test Case 3. In this study, the effects of the estimation waveforms on the quality of generated models have been also addressed (paragraph d of Sec. 3). From all the tests carried out, we found that estimation stimuli belonging to the class of multilevel waveforms shown in Fig. 1 weakly affect the quality of estimated models. Besides, it is worth noting that a larger number of levels benefits the estimation of models rather that a larger duration of the steady-state parts of the port voltage stimuli.

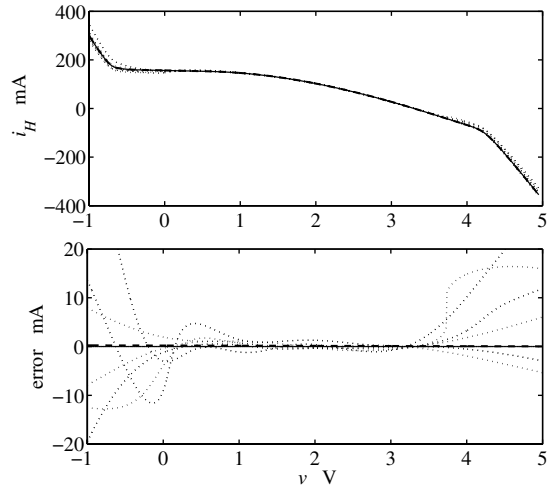

Figure 5: Output port static characteristic i_H (top panel) and error quantified as the difference between reference and predicted curves (bottom panel). The curves are generated by different initialization of model parameters in the estimation process. Solid thin line: reference; dashed line: model #4; dotted line: model #3 for different run of the estimation procedure and different parameter initialization.

5. CONCLUSIONS

This paper presents a systematic discussion of the impact of the modeling setup on the performance of the estimated models for the behavioral modeling of driver circuits. An extensive numerical study is performed on the modeling of a commercial device with a pronounced nonlinear dynamic behavior. This study hightlights that *(i)* nonlinear parametric models must be used to capture the nonlinear dynamic behavior of actual devices, even for operation voltages within the range of power supply rails, *(ii)* the inclusion of the actual static characteristic of the device in the model structure improves the quality of the estimated models, *(iii)* more accurate static behaviors of models outside the voltages explored by identification signals can be achieved by constraining the optimization problem for the computation of model parameters, *(iv)* for the device considered of this study and most drivers, static algorithms for the parameter estimation are much faster that the corresponding dynamic ones and my lead to even more accurate results, *(v)* for the proposed model representation, the choice of the port voltage stimuli to generate the estimation waveforms weakly affect the quality of estimated models.

Acknowledgements

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4. REFERENCES

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