On-the-fly Estimation of IC Output Port Macromodels

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Abstract

This paper addresses the generation of IC output buffer macromodels from responses recorded during regular operation of devices. The proposed methodology is based on the estimation of suitable parametric relations via a well established procedure and does not requires specific modeling setup and test fixtures. The feasibility of the approach for the modeling of a real device from noisy measured data is demonstrated via numerical simulation.

Introduction

The design of modern electronic equipments operating in the GHz range requires, at the early stage of the design process, the assessment of SI/EMC effects on critical interconnect paths. Such an assessment, that is achieved by the simulation of signals propagating on interconnect structures like the one sketched in Fig. 1, relies on the availability of accurate and efficient macrommodels of the ports of digital integrated circuits (ICs) that act as the nonlinear terminations of interconnects. As an example, a macromodel for the output buffer in Fig. 1 is represented by a suitable nonlinear dynamic relation between voltage v and current i of the device port.

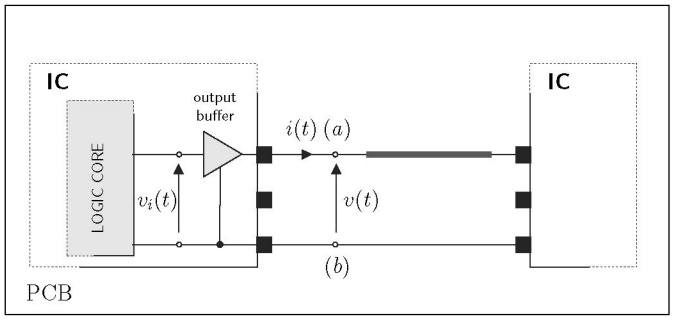

Figure 1: Typical interconnect structure with the main IC blocks and the relevant electrical variables.

Different approaches are in use to obtain IC port macromodels. The most common approach is based on simplified equivalent circuits derived from the internal structure of the modeled devices. This approach leads to the I/O Buffer Information Specification [2], that is widely supported by EDA tools and dominates modeling applications. More recent approaches are based on the use of parametric relations to approximate the device port equations and on the identification of their parameters from device responses [1]. These approaches offer enhanced modeling capabilities, that facilitate and improve the modeling of recent devices, like preemphasis drivers.

For both approaches, however, the generation of macromodels requires the availability of transistor-level models of the device, or the capability to control the device operation, *i.e.*, the use of dedicated test fixtures to stimulate and measure specific device behaviors. As an example, the estimation of parametric models for the output buffer in Fig. 1 exploits port responses recorded while the buffer is forced (*e.g.*, through the internal logic signal v_i) in a fixed logic state or is forced to perform complete state switchings [1] on suitable test loads. In real devices with complex logic cores, output buffer states can be hardly controlled and model generation from measured data becomes unpractical.

In this paper, we propose a new technique for the generation of macromodels from actual measurements, avoiding the need of dedicated test fixtures and device control. Macromodels are obtained from device port transient responses measured on devices mounted directly on the board and operating in normal conditions as in the simplified scheme of Fig. 1.

Model structure, estimation and validation

Parametric macromodels of the output buffers of digital ICs exploit the following two-piece parametric relation

$$i(t) = w_H(t) i_H(v, d/dt) + w_L(t) i_L(v, d/dt) \qquad (1)$$

where w_H and w_L are switching signals accounting for the device state transitions and playing the same role of the internal voltage v_i in Fig. 1, and i_H and i_L are nonlinear parametric relations accounting for the device behavior in fixed logic high and low states, respectively [7]. More details on the model representation (1) and on the use of parametric relations for the modeling of IC ports can be found in [1] and references therein.

The estimation of model (1) amounts to computing the parameters of submodels i_H and i_L and the weighting signals w_H and w_L from suitable port voltage $v(t)$ and current $i(t)$ responses. Model parameters are computed by minimizing suitable error functions between the model responses and the measured port responses, that are used as references to be fitted [7, 8].

The problem addressed in this paper is how to obtain device responses useful for model parameter estimation while the device is mounted on an application board and operates in normal mode. For the sake of simplicity, the discussion is based on the output port of a commercial Texas Instruments transceiver, whose HSPICE transistor-level description is available from the official website of the vendor. The example device is a 8-bit bus transceiver with four independent buffers (model name SN74ALVCH16973, power supply voltage VDD =1.8 V). The example device operates at 167 Mbps, *i.e.*, the bit time is 6 ns, and is driven to produce a 2048 long pseudo-random bit stream. The HSPICE simulations of the transistor-level model of the driver are assumed as the reference curves hereafter.

Figure 2 shows static characteristics of the example device and

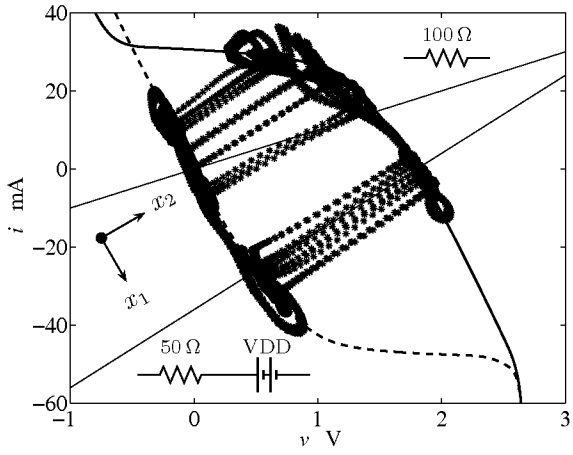

Figure 2: Static characteristics of the example driver in fixed high state (solid thick line) and low state (dashed thick line) superimposed to the characteristics of two lumped resistive loads and the samples $\{v(t),i(t)\}$ of the port transient responses in Fig. 3 (star line).

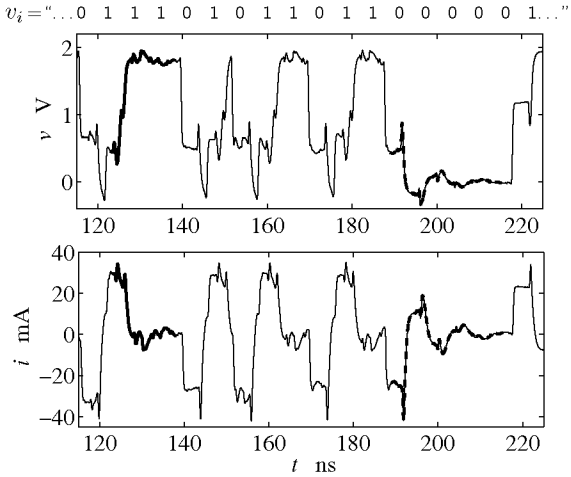

Figure 3: Output port voltage $v(t)$ and current $i(t)$ responses computed for the example driver connected as in Fig. 1 with a mismatching stub placed between terminals (a) and (b) (see text). The thick parts of the $v(t)$ and $i(t)$ signals are the waveforms used for the estimation of the submodels i_H and i_L in (1) (see text for details).

trajectories of device transient response in the output voltage and current plane. The upper (lower) curve is the device output static characteristic when the device is in the HIGH (LOW) logic state, and the cloud of dots are samples of output current and voltage transient responses recorded during ordinary switching operation. The output transient responses leading to the trajectories of Fig. 2 are shown in Fig. 3 and are recorded while the device is connected as in Fig. 1. This circuit is composed of a standard point to point topology augmented by a shunting stub connected between terminals (a) and (b). From the experimental point of view, this circuit can be easily obtained by shunting the proper trace of an application board. For the simulations of Fig. 2, the stub is modeled as an ideal transmission line (characteristic impedance $Z_0 = 50\Omega$, time delay $T_d = 2\,ns$) loaded by a 10 pF capacitor. Figure 2 highlights that the transient responses obtained with the shunting stub can densely explore the portion of voltage and current plane around the device static output characteristics. Hence they are good candidates to serve for the identification of model parameters. In contrast, transient responses obtained by connecting different loads, as simple resistors, do not explore a relevant portion of the output variables and can be hardly used for model parameter estimation. These observations suggest the following two-steps procedure for the estimation of model (1):

(i) Estimation of submodels. As in [1], the parametric models used for i_H and i_L in (1) are discrete-time parametric representations based on sigmoidal expansions [7], whose parameters can be estimated by standard algorithms like [8]. The estimation waveforms for submodel i_H (i_L) must be voltage and current transient responses containing enough information on the port dynamic behavior while the device is in High (Low) logic state. For the example device, the estimation waveforms of i_H can be obtained from the solid thick parts of the signals $v(t)$ and $i(t)$ of Fig. 3. These signals are obtained by considering the slice of the port responses recorded while the device is kept through the internal (non-accessible) input signal v_i in the fixed High state for a number of consecutive logic ones. Similarly, the estimation waveforms of submodel i_L can be the dashed thick parts in Fig. 3.

In order to facilitate the modeling process, the estimation of submodels is carried out in terms of the auxiliary variables (x_1, x_2) defined by the following linear transformation

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 1 & -50 \\ 1 & 50 \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} \qquad (2)$$

Submodels i_H and i_L, in fact, must be defined over the same range of the (voltage) input variable values. In (x_1, x_2) plane, the trajectory of state transitions have nearly constant x_1 values (see Fig. 2), thereby leading to a reduced modeling range for the x_1 input variable. For the example device of this study, the submodels i_H and i_L turns out to have both dynamic order 3 and are composed of 2 and 3 sigmoidal terms, respectively [1].

(ii) Computation of weighting signals. The weighting signals w_H and w_L are computed after the estimation of the submodels i_H and i_L from port responses occuring during state switchings, as discussed in [1]. In our problem, this amounts to solving the single linear equation (1) where v and i are the voltage and current responses recorded during single transition events while the device operates in regular conditions as in Fig. 1 and w_L is assumed to be $w_L = (1 - w_H)$. In principle, such an assumption can be removed and two set of port responses can be used to compute two independent w_H and w_L signals. However, the latter simplification benefits the quality of the complete model since it reduces possible ill-conditioning or inaccuracies of the solution of the linear problem arising from noisy measured data or from the approximated responses of submodels i_H and i_L.

Once all model parameters are computed, the model equations are converted into a macromodel to be plugged in a standard

simulation environment, *e.g.*, SPICE or any hardware description language allowing for analog parts. Implementation details are described in [1].

Validation results

In this section, the macromodel estimated for the example device of this study is validated by comparing its static characteristics and transient responses to a test load with those obtained from the reference transistor-level model of the example driver. The validation load is an ideal transmission line (characteristic impedance $Z_0 = 50\Omega$, time delay $T_d = 1\ ns$) loaded by the shunt connection of a $100\,\Omega$ resistor and a $5\,\mathrm{pF}$ capacitor. All the static characteristics and the transient response of the reference model and of the SPICE-type implementation of the macromodel are computed by means of HSPICE. The top panel of Fig. 4 shows the comparison of the actual static characteristics of the device compared to the static characteristics of submodels i_H and i_L estimated by the proposed procedure. This comparison confirms the accuracy of estimated models to capture the static information of the device. Besides, the bottom panel of Fig. 4 shows part of the port voltage waveform $v(t)$ computed by the reference transistor-level model and by the macromodel and recorded while the driver is connected to a distributed load different from the one used in the estimation process. The transient curves in Fig. 4 highlights the high accuracy of the complete macromodel running in normal operation conditions.

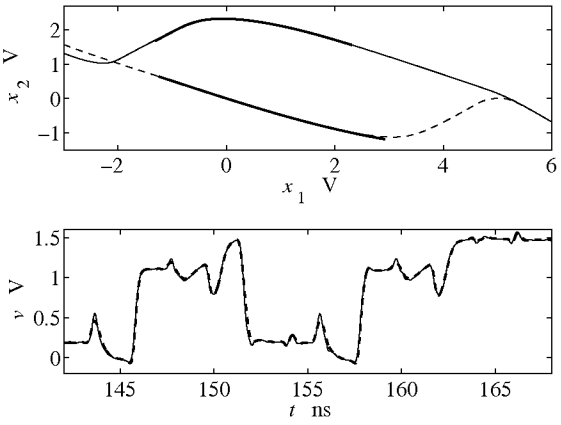

Figure 4: Top panel: static characteristics of submodels i_H and i_L in (1) (solid thick curves) superimposed to the actual characteristics of the example driver in fixed high state (solid line) and low state (dashed line); bottom panel: Port voltage $v(t)$ response computed for the example driver connected to a validation load. Solid curve: reference; dashed: macromodel.

As a second and more realistic test, aimed at verifying the feasibility of proposed approach for the generation of macromodels from actual measurements, the estimation of submodels i_H and i_L has been carried out from noisy responses. For this second test case, the estimation of submodel parameters is carried out by means of the algorithm [9]. The above algorithm is a modification of the basic version [8] used for the noiseless case in which a suitable penalty function is introduced in the minimization scheme to average the effects of noise and thus to avoid problems of spurious dynamics of estimated models. As an example, Fig. 5 shows the transient responses used for the estimation of submodel i_H that is corrupted by a superimposed gaussian white noise with standard deviation $\sigma = 4\%$ of the voltage and current swing. The top panel of Fig. 6 shows the comparison between the actual static characteristics of the device and the static characteristics of submodels i_H and i_L. Besides, the bottom panel shows part of the port voltage waveform $v(t)$ computed by the reference transistor-level model and by the macromodel and recorded while the driver is connected to the same validation load of the previous test. The comparison carried out in this second test highlights the robustness of the proposed estimation procedure and the good accuracy of the complete macromodel estimated from on-line measured data.

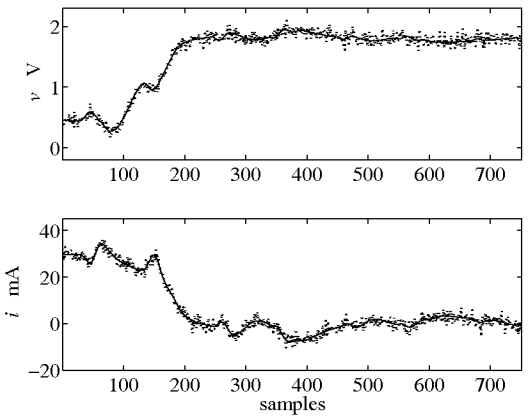

Figure 5: Port voltage $v(t)$ and current $i(t)$ signals used for the estimation of submodel i_H, *i.e.*, the solid thick signals in Fig. 2, with a superimposed gaussian white noise with standard deviation $\sigma = 4\%$ of the voltage and current swing.

Conclusions

This paper addresses the development of accurate and efficient macromodels of the output ports of digital integrated circuits. The proposed models are parametric relations reproducing the external behavior of devices that can be effectively estimated from port transient responses recorded during the normal operation of devices. The proposed procedure avoids the need of dedicated test fixtures and device control thus overcoming the previous limitations of existing methodologies in generating macromodels of real devices from actual measurements. The approach is demonstrated via numerical simulation, also for model estimation based on noisy measurements.

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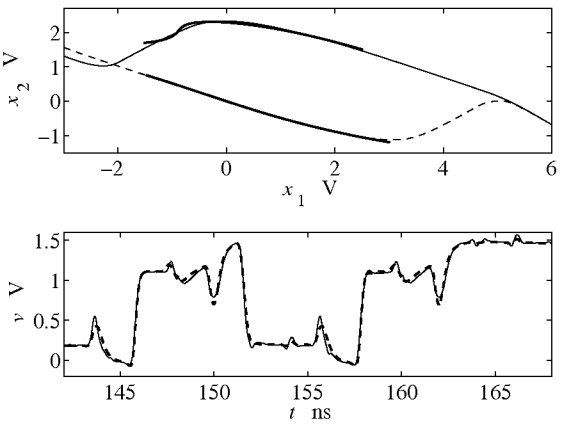

Figure 6: Top panel: static characteristics of submodels i_H and i_L in (1) estimated from noisy signals (solid thick curves) superimposed to the actual characteristics of the example driver in fixed high state (solid line) and low state (dashed line); bottom panel: Port voltage $v(t)$ response computed for the example driver connected to a validation load. Solid curve: reference; dashed: macromodel.

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