[Article] Evolution of Organic Chip Packaging Technology for High Speed Applications

Evolution of Organic Chip Packaging Technology for High Speed Applications

Erich Klink, *Member, IEEE*, Bernd Garben, Andreas Huber, Dierk Kaller, Stefano Grivet-Talocia, *Member, IEEE*, and George A. Katopis, *Fellow, IEEE*

***Abstract*—The high dense interconnect (HDI) organic chip packaging technology has made rapid development advancements in the last few years. Due to the dense wiring structures in the build up layers and the recently introduced fine line core with micro vias, high signal input/output (I/O) applications and dense chip area array footprints can be supported. These technology improvements support specific new dense chip applications. In this paper the electrical characteristics and the evolution of this packaging technology is described. The electrical description is especially focussed on material characteristics and the signal integrity including cross talk. In addition the impact on high speed data transmission and the performance differences between single-chip module (SCM) and multichip modules (MCM) are discussed. Also the power integrity is described on the basis of the results of a mid frequency power noise analysis.**

***Index Terms*—HDI, MCM, SCM.**

I. Technology Evolution

THE EVOLUTION of the high dense interconnect organic chip packaging technology has taken very fast development steps during the last eight years and a similar rapid advancement can be predicted for the near future.

The standard card and board technology, used as chip carrier, is generally considered as the first generation of organic chip packaging technology. (see Fig. 1) The first generation was only capable to support wire bonded chips with very low signal input/output (I/O) counts. The large plated thru holes (PTH) and their large metal lands and via pitch, limited the fan out wireability of chip footprints significantly. In addition the drilled and plated thru holes did not allow that chips could be placed on top of the vias. Therefore only wire bond applications could be applied [1].

The invention of build up layers with micro via-holes in 1992, which are symmetrically attached at both sides of the laminated core, enabled this technology to facilitate also flip chip applications with modest signal I/O counts. This technology is considered as the second generation (GEN 2, see Fig. 2).

The micro vias were first manufactured using photosensitive materials and etch processing. Today these processes are mostly replaced by laser drilled micro vias.

Manuscript received September 1, 2003; revised December 5, 2003.

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Digital Object Identifier 10.1109/TADVP.2004.825457

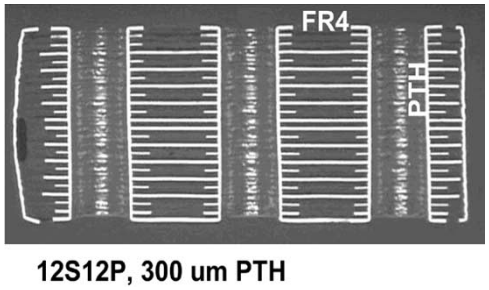

Fig. 1. First generation of organic chip packaging technology.

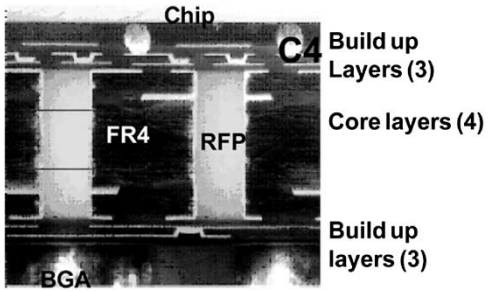

Fig. 2. Second generation of organic chip packaging technology.

The core contains plated thru holes (PTHs), reaching from the top build up layer to the bottom build up layer and also buried core vias. The buried core vias penetrate only the core but not the build up layers. These vias are filled with resin to achieve a flat surface for further planar processing of build up layer. Due to the planar structure the build up layers can support wires above the buried vias. The buried core vias are called "resin filled plated thru holes" (see RFP in Fig. 2).

The significant improvement of generation 3 arise from the introduction and full availability of the fine line core layer with micro vias as described in Fig. 3. The microvias in the core are realized by using laser drilled vias not only in the build up layers but also in the core.

Table I shows the key factors of the technology roadmap spanning from the GEN 1, GEN 2, GEN 3 into the predicted future generation. One of the key factors is the conductor line width in the build up layers and core layers (Table I). The second important factor is the via land size. Table I shows significant improvements in line width and the reduction of the core via land size. Both factors are the main achievements of generation 3, obtained due to the development of the fine line core technology. The dense fine line core has now a very similar wiring and via density as the build up layers. This solves the disadvantage of GEN 2 that the high wiring capacity of the top and bottom build

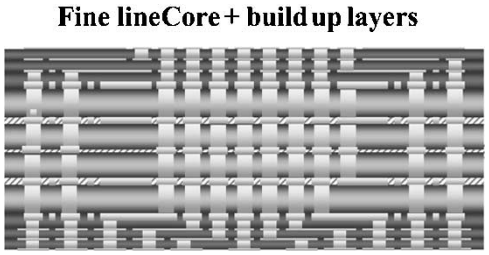

Fig. 3. Third generation of organic chip packaging technology.

up layers are not any more disturbed or even "disconnected" by the coarse core. In generation 2, the large core via land size blocked the connectivity between the wiring in the top build up layers with the wiring in the bottom build up layers. If chip pads cannot be wired in the top build up layers, they can drop in Gen 3 with micro vias directly thru the core and make use of the wiring capacity of the bottom build up layers. This enables the third generation to support very high signal I/O counts with more than 1000 signals per chip. In addition also small multi-chip modules (MCMs) can be wired and some applications will be shown in this paper.

II. Packaging Applications

With the introduction of GEN 3 the applications are extended to high I/O single chip modules with dense area array flip chip footprints. The chip footprints can achieve bump pitches below 200 μm. Fig. 4 shows such a typical SCM application using only a fine line core. The single chip module can consist of a multilayer fine line core with or without build up layers on top and bottom side of the core. Fig. 5 shows an SCM application with fine line core and build up layers. This structure achieves a higher wiring capacity and more chip signals can be fanned out. The off-module connections are usually provided with solder ball connects but can also be performed by pins. A specific SCM application is shown in Fig. 6. The structure is a combination of fine line and thick core. It can however also be a combination of thick core with build up layers. In the pocket of the thick core on the backside of the fine line core or build up layers, several small size SMT capacitors are assembled. They are connected with many small microvias to the voltage and GND pads of the processor chip. Due to the high amount of short micro vias a very low inductive loop is achieved which significantly helps to reduce the on chip power noise. A similar structure is described in [3] by Intel's recently announced bumpless build up layer technology. In this case the build up layers are not any more connected thru solder balls to the chip pads, but directly into the chip metal layers [3].

Due to the high wiring capabilities MCM applications can also be supported. The classical MCM is realized by assembling two chips side by side close to each other on the top side of the module as shown in Fig. 7.

A typical MCM application can consist of the processor chip (CP) and its private L2 cache chip. Fig. 10 also shows the data path comparison from CP to L2 for SCM versus MCM applications. For the SCM application the typical data path lengths are in the range of 10 mm on SCM and 70 mm on card. For the

TABLE I
Organic Chip Carrier Technology Roadmap

	Gen. 1	Gen. 2	Gen. 3	Future
Core via land	650 μm	550 μm	150 μm	80 μm
BU via land	-	150 μm	70 μm	55 μm
Core line width	100 μm	75 μm	30 μm	25 μm
BU line width	-	65 μm	30 μm	20 μm

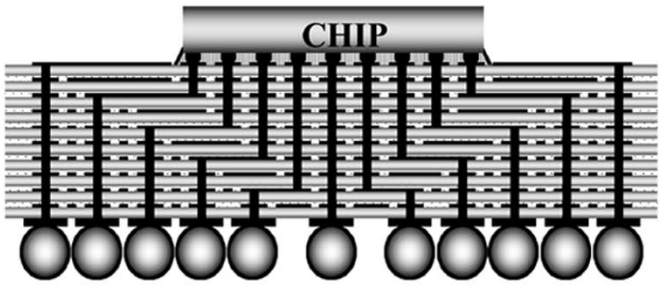

Fig. 4. Typical SCM application with fine line core.

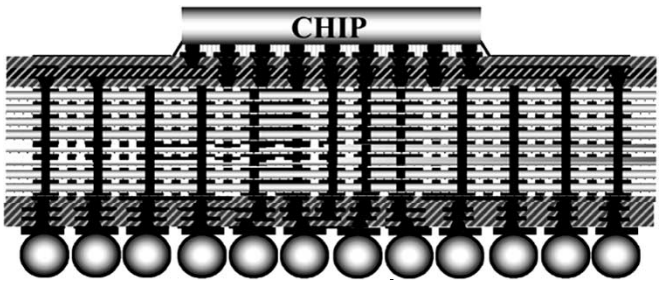

Fig. 5. SCM application with fine line core and build up layers.

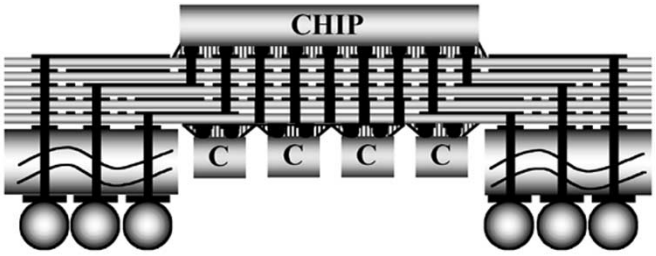

Fig. 6. SCM application with fine line core and thick core.

MCM application the data path is typically realized by 40 mm of on-MCM wiring.

A very high dense and extremely short CP-L2 data path is shown in Fig. 8. In this specific MCM application the cavity in the thick core is used for the back side mounted L2 cache chip. Due to the dense vertical structure, the chip to chip signal and power connections are basically only stacked via-holes through the build up layers or fine line core layers. This very short data path supports the CP-L2 interface performance at processor cycle.

The high number of signals in conjunction with the fast cycle time leads to a very high CP-L2 bandwidth. This specific double

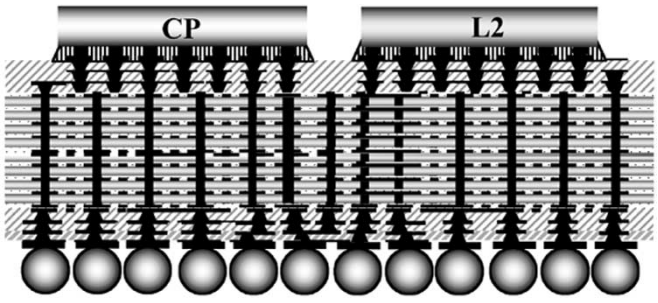

Fig. 7. MCM application with single sided (top side) assembly.

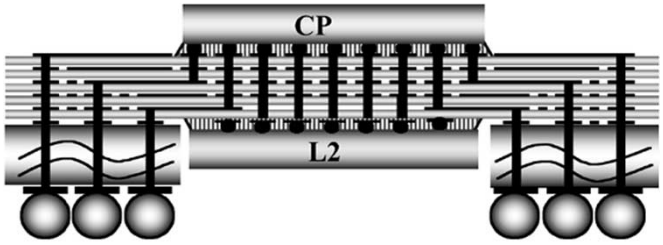

Fig. 8. MCM application with double sided assembly.

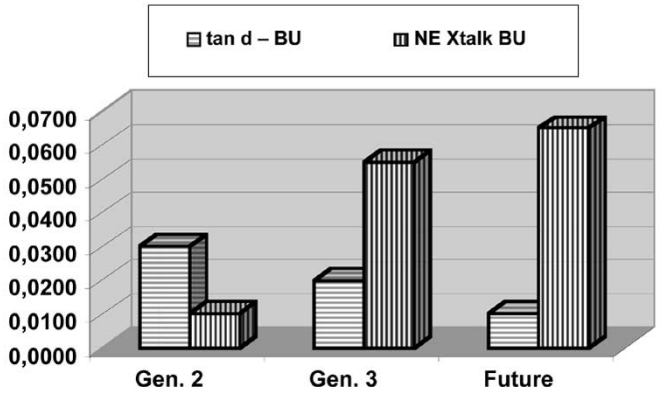

Fig. 9. Trend of key electrical parameters.

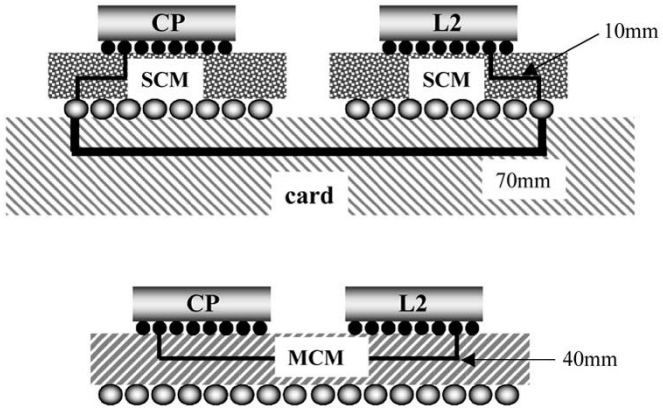

Fig. 10. Data path comparison CP-L2 on SCMs and on MCM.

sided structure requires that the chip footprints of the CP and L2 chip have to be optimized together. The high number of Voltage and GND bumps and MCM via-holes also help to achieve a single sided cooling system assuming a moderate power consumption of the L2 chip.

TABLE II
SUMMARY OF KEY ELECTRICAL PARAMETERS

	Gen. 2	Gen. 3	Future
ε – BU/core	4.0	3.5	3.0
tan δ – BU	0.03	0.02	0.01
tan δ – core	0.03	0.01	0.003
Z0 BU	40 Ω	50 Ω	50 Ω
Z0 core	50 Ω	50 Ω	55 Ω
NE Xtalk BU	1 %	5.5 %	6.5 %
NE Xtalk core	6 %	8 %	9 %

III. ELECTRICAL CHARACTERISTICS

Table II summarizes the key electrical parameters of the technology generations. The values for the dielectric constant reduce from 4.0 of today's build up layer and core materials to 3.0 in the near future. In addition the dielectric loss decreases significantly by a factor of ten from 0.03 to the very low value of 0.003 for future core materials. The impedance of the build up layers is below 50 Ω for the second generation (GEN 2) and will increase to 50 Ω. The impedance of the core layers is at 50 Ω today and increases to values above 50 Ω. It has to be emphasized that the characteristic impedance varies because of the decreasing spacing between lines. The coupling between adjacent lines increases continuously due to denser wiring. The saturated near end cross talk (NEXT) values in Table II demonstrate this tendency. This behavior is similar to the on-chip wiring development, described in [2]. The maximum routing lengths are increasingly determined by cross talk effects. In Fig. 9 two key parameters—dielectric loss and near end cross talk are described. It is visible that both parameters have opposite trends. The cross talk values are not excessively high but increase and have to be controlled carefully as explained below.

Fig. 11 describes in details the cross talk analysis of an on-MCM line pair with a parallel line length of 40 mm. The voltage curves of near end (NE) and far end (FE) cross talk noise are shown for build up and core layers. The active line is connected to a 50 Ω driver and contains a signal rise time of 100 ps with 500 mV swing.

The results in the four pictures (near end and far end cross talk for core and build up layers) show that the near end (NE) and far end (FE) coupled noise values increase through the generations, because of the significant increasing wiring density as shown in Table II. The far end noise values are much smaller than the near end values due to the stripe line structure and the difference of coupling coefficients. Although the coupled noise values are not high, especially the near end noise has to be carefully taken into account during system design. This is achieved with a detailed system timing and coupled noise analysis including all coupling segments along the lines. The exclusion of any impact of near end noise can be achieved by routing the

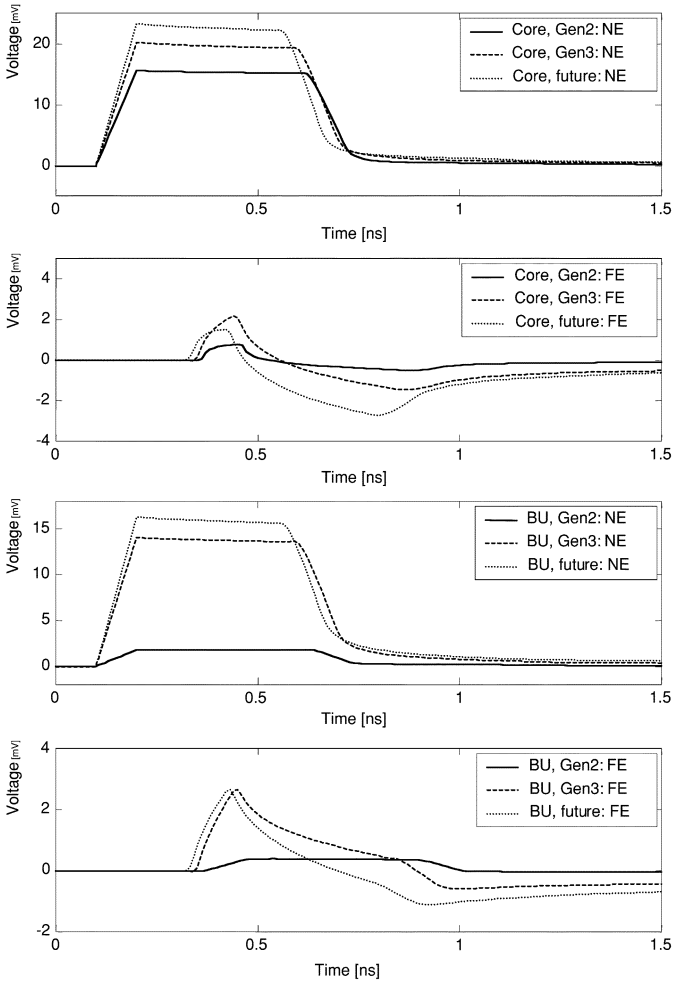

Fig. 11. Comparison of near end (NE) and far end (FE) coupled noise of 40 mm parallel line pair in core and in BU layers.

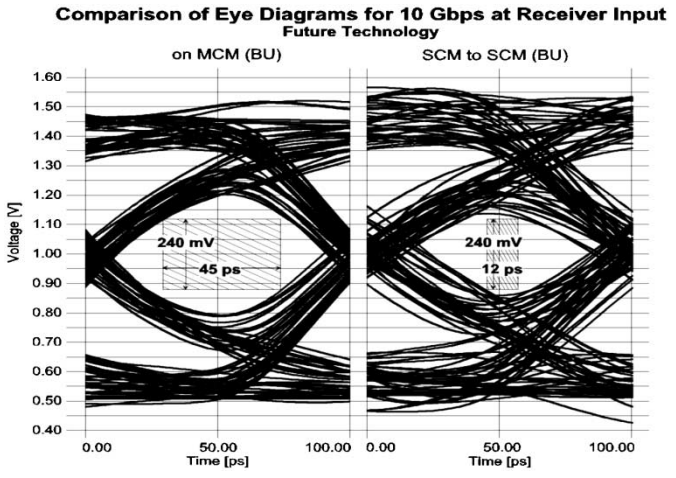

Fig. 12. Eye simulation with opening criteria for secure signal transmission (min width = 50 ps, min amplitude = ±120 mV).

busses accordingly so that only unidirectional signals are adjacent to each other. To guarantee timing and noise accuracy, the transmission line models and the simulation algorithm must account for frequency dependent parameters.

The parallel line length of 40 mm is a typical value valid for small MCMs. For single-chip modules however the dense parallel line length is significantly shorter (ca. 10 mm).

Fig. 12 compares the transmission eyes for on-MCM nets versus SCM to SCM nets as described in Fig. 10, using a single rail (not differential) signal transmission scheme. The coupling of one neighbor line is also included. To achieve a secure signal transmission from the driver to the receiver, the criteria for the opening of the signal transmission eye is a minimum of the half bit time. This means for a bit time of 100 ps (10 Gbps) an opening of 50 ps is needed. The vertical height for this eye is defined by the used receiver technology. It has to be noted that this criteria does not define the highest possible transmission frequency for the transmission channel, but is used as a simplified standard rule. There exist additional circuit methodologies for high speed data transmission, such as driver predistortion, channel equalization, coupled noise cancellation etc., which increase the channel bandwidth. However these methods are not described in this paper. Fig. 12 shows that the eye opening for on-MCM nets is much larger than for the SCM to SCM nets. The eye opening of the MCM net is 45 ps, while the eye opening for the SCM to SCM net is only 12 ps applying the future build up layer (BU) technology.

In Table III the timing and noise simulation results for the eye opening are summarized for various generations of build up layer technologies assuming a cycle time of 100 ps. Due to increasing line to line coupling and especially increasing attenuation, the eye opening decreases in general going to smaller line dimensions. In the MCM case the eye opening is significantly larger than the SCM case due to much less attenuation and disturbance due to the shorter net length as shown in Fig. 12. This means that the SCM-SCM nets are far away to meet the eye opening criteria.

Fig. 13 shows schematically an equivalent subcircuit model for the power distribution system from the card to the chip. The current sources i(t) represent synchronously switching on-chip currents and the elements C1, R1 represent a portion of the on-chip decaps. The elements L2, C2, R2 depict the on-module capacitors and L3, C3, R3 the on-card capacitors. The inductances L5, L6, and the resistances r5, r6 belong to voltage and ground planes and vias of the package. For the mid-frequency power noise analysis the commercial full-wave simulation tool SPEED2000 from Sigrity Inc. was used.

Fig. 14 compares the power noise simulation results of the first, second, and third technology generations. The power noise is reduced by 40% for the second generation due to the reduced loop inductance from the noise sources on the chip to the on-module decoupling capacitors. This is achieved by the build up layer with thin dielectric between voltage and ground planes. As the dielectric thickness of the build up layers continues to decrease from generation 2 to generation 3, the mid-frequency power noise is further reduced by 10%.

IV. Conclusion

The electrical and wiring characteristics and benefits of the organic chip packaging technology have been demonstrated. It

TABLE III
COMPARISON OF EYE OPENING FOR 40 mm MCM LINES WIRED IN BU LAYERS AT 10 Gbps

Eye opening	BU GEN 2	BU GEN 3	BU Future
On MCM	63 ps	49 ps	45 ps
SCM-SCM	44 ps	30 ps	12 ps

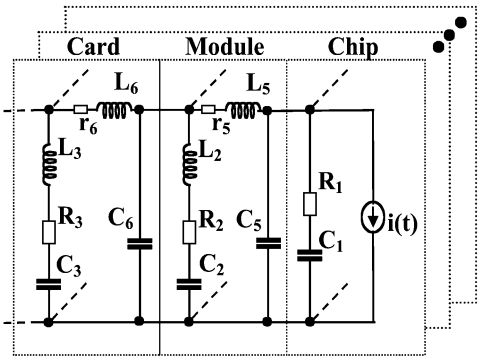

Fig. 13. Equivalent subcircuit for mid-frequency power noise analysis.

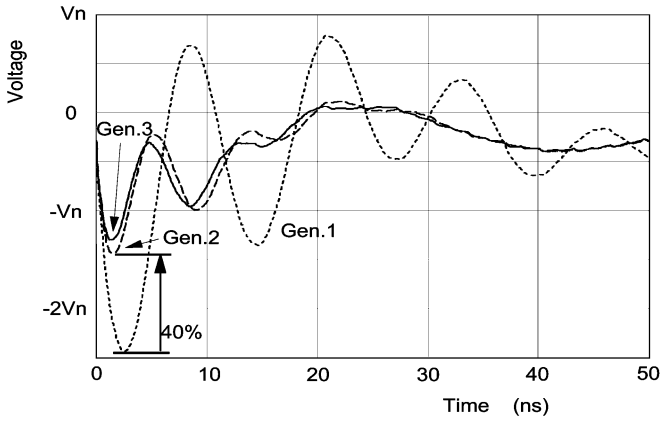

Fig. 14. Mid-frequency power noise comparison of the organic chip carrier generations 1, 2, and 3.

has been shown that the third generation has superior characteristics with regards to wireability. Therefore large and dense chip footprints can be uitilized. This supports high signal I/O count single-chip and small MCM applications.

The signal integrity analysis revealed low cross talk values for far end and near end. Although these noise amplitudes are not very high, a careful control during the system design is recommended. The mid frequency power noise analysis displayed high reductions of the power noise values. Overall the generation 3 with the substantially increased wireability gives significant bus performance advantages especially for MCM applications. Compared to other published high dense packaging technologies like HyperBGA and 3M's VCP, the GEN3 of the organic packaging technology has major advantages in wiring capacity, due to the larger number of high dense wiring layers in the core and in the top and bottom build up layers. Another advantage is the lower cost of the manufacturing process, which is based on the standard large panel process for cards and boards.

ACKNOWLEDGMENT

The authors would like to thank E. Blackshear, IBM Fishkill, and T. Nishio, IBM Yasu, for their helpful feedback and discussions.

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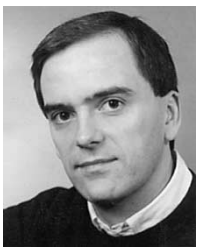

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