Comparative Study of the MASH Digital Delta-Sigma Modulators

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***Abstract*—The paper focuses on the Multi-stAge noise SHaping (MASH) digital delta-sigma modulator (DDSM) that employs multi-moduli (MM-MASH). Different architectures of the MASH DDSM are compared. In particular, it is proven that a higher-order error feedback modulator (EFM) has the same sequence length as a first-order EFM (EFM1) in an MM-MASH. In addition, the method that is required to setup the quantisation moduli of the MM-MASH is introduced. The theory is validated by simulation.**

I. INTRODUCTION

Digital delta-sigma modulators (DDSM) are widely used in consumer electronic equipment such as cellular telephones, MP3 players and wireless-LANs. A DDSM is composed of several error feedback machines (EFM). The architectures of EFMs decide the sequence length of DDSMs. Since a short sequence length results in unwanted frequency components in the output frequency spectrum [1], much research has been done into maximising the sequence length. There are two approaches to lengthen the sequence length: stochastic and deterministic methods. The most common stochastic approach is that of dithering [2] [3]. However, it requires extra hardware and inherently introduces additional noise in the the useful frequency band. Thus, some deterministic design methodologies have been proposed to maximise the sequence length.

Borkowski [4] sets the initial condition of the registers to make the sequence length of the conventional MASH DDSM reach its maximum value. Hosseini [5] modifies the structure of DDSMs to make the quantizer modulus a prime number. The period of such a sequence is proven by mathematical analysis [6]. Xu [7] introduces a digital delta-sigma modulator structure to further increase the sequence length. It proposes that the modulus of each quantizer is set as a different value from each other. Note that each quantizer has only one modulus. Furthermore, all of the moduli are co-prime numbers. The difference between the co-prime numbers and the prime numbers [8] is stated as below:

1) A prime number is a natural number which has exactly two divisors: 1 and itself.
2) If the greatest common divisor of any two numbers is 1, they are co-prime numbers. They do NOT have to be prime numbers.

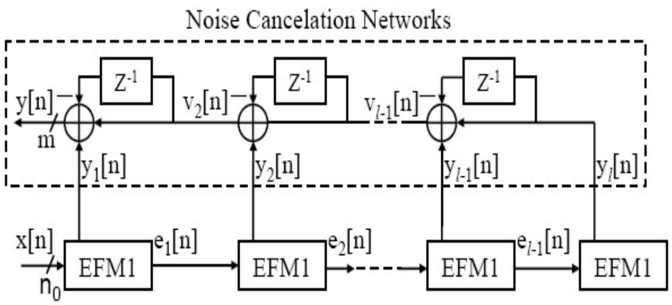

Fig. 1. MASH DDSM architecture.

The hardware requirement is reduced, if the MASH DDSM utilises higher order EFMs [9]. However, it results in poorer noise performance. This paper examines the use of higher-order MM-EFMs. In section II, the different architectures of the EFM1s are introduced. Their sequence length is compared. In section III, the sequence length of higher-order MM-EFMs is derived. The simulation results are illustrated in section V.

II. PREVIOUS WORK WITH EFM1S

The architecture of an lth order MASH DDSM is illustrated in Fig. 1. It contains l first-order error-feedback modulators (EFM1). $x[n]$ and $y[n]$ are an n_0-bit input digital word and an m-bit output, respectively. The relationship between them is

$$mean(y) = \frac{X}{M} \tag{1}$$

where $mean(y)$ represents the average value of y, X is the decimal number corresponding to the digital sequence $x[n]$ [10], i.e., $x[n] = X \in \{1, 2, ..., M-1\}$, and M is the quantizer modulus which is set as 2^{n_0} in the conventional DDSM.

A. Conventional EFM1

The model of the EFM1 is shown in Fig. 2. This is a core component in the make-up of the MASH digital delta-sigma modulator (DDSM). The rectangle Z^{-1} represents the register which stores the error $e[n]$ and delays it for one time sample. $Q(\cdot)$ is the quantization function:

$$y[n] = Q(u[n]) = \begin{cases} 1, & u[n] \geq M \\ 0, & u[n] < M \end{cases} \tag{2}$$

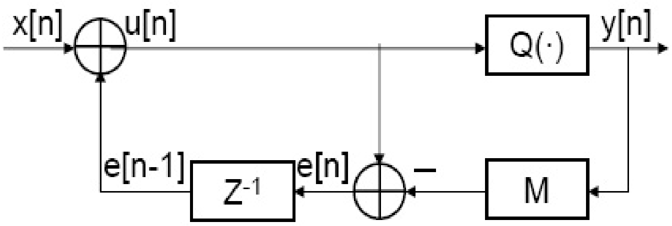

Fig. 2. EFM1: First-order error-feedback modulator.

where

$$u[n] = x[n] + e[n-1]. \tag{3}$$

The guaranteed and maximum sequence lengths for this structure have been found from simulations [4], and are as shown in Table I. To achieve both of these sequence lengths, the first stage EFM1 must have an odd initial condition. This is implemented by setting the register. The modulator period varies between the guaranteed and maximum sequence length dependent on the value of the input. It is found that the conventional MASH modulator period will always be approximately equal to the maximum sequence length if the quantizer modulus, M, is set as a prime number [6].

TABLE I
THE SEQUENCE LENGTH SUMMARISED IN [4].

Modulator Order	Guaranteed Period	Maximum Period
2	2^{n_0-1}	2^{n_0+1}
3	2^{n_0+1}	2^{n_0+1}
4	2^{n_0+1}	2^{n_0+2}
5	2^{n_0+2}	2^{n_0+2}

B. HK-EFM1

The architecture of the modified EFM1 used in the HK-MASH is illustrated in Fig. 3. The only difference between it and the conventional EFM1 in Fig. 2 is the presence of the feedback block aZ^{-1}. a is a specifically-chosen small integer to make $(M-a)$ the maximum prime number below 2^{n_0} [5]. The sequence length of it is $(2^{n_0}-a)^l \approx (2^{n_0})^l$.

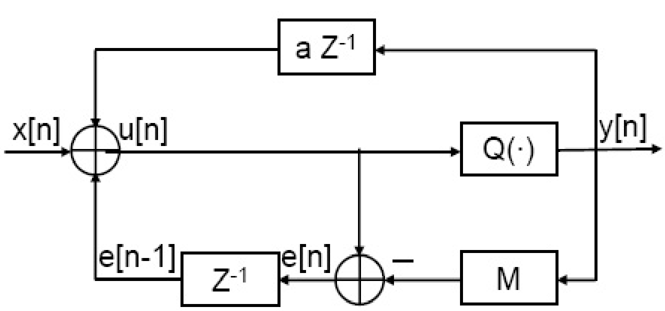

Fig. 3. The modified EFM1 used in HK-MASH.

C. MM-EFM1

The structure for the MASH digital delta-sigma modulator (DDSM) employing multi-moduli [7] is reviewed here. It is termed the MM-MASH. As illustrated in Fig. 4, M_p represents the quantizer modulus in pth stage of MM-EFM1. The crucial points to note about this structure are:

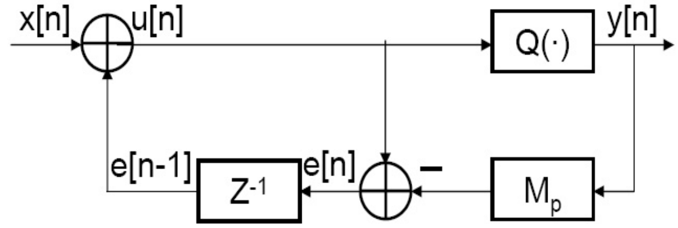

Fig. 4. MM-EFM1: The modified first-order error-feedback modulator used in MM-MASH.

1) Every MM-EFM1 has a different modulus
2) Each MM-EFM1 still only has ONE quantizer modulus.

The sequence length of the pth effective stage EFM1 depends on the previous EFM1 stage:

$$\sum_{k=1}^{N_p} y_p = \frac{K}{M_p} \sum_{k=1}^{N_{p-1}} e_{p-1} \tag{4}$$

where

$$K = \frac{N_p}{N_{p-1}}. \tag{5}$$

The expression for the sequence length of the pth EFM1 in an lth order MASH modulator is:

$$N_p = \frac{M_1 M_2 ... M_i}{\lambda_p} \tag{6}$$

where $p \in \{1, 2, 3, ..., l\}$ and λ_p is the maximum common divisor of $\lambda_{p-1} M_p$ and $M_1 M_2 ... M_{p-1} mean(e_{p-1})$. Note that when $p = 1$, $mean(e_0) = X$ and $\lambda_0 = M_0 = 1$.

Then the lth order MASH DDSM sequence length is expressed as:

$$N = \frac{M_1 \cdot M_2 \cdot ... \cdot M_l}{\lambda} \tag{7}$$

where λ is a parameter to make N the least common multiple of the sequence length of each stage N_i.

If the two conditions shown below are satisfied:

C1: X and M_1 are co-prime numbers
C2: $\{M_1, M_2, ..., M_l\}$ are co-prime numbers

the sequence length is maximised to

$$N_{max} = M_1 \cdot M_2 \cdot ... \cdot M_l. \tag{8}$$

D. Comparison of the Sequence Length

The sequence length is only 1024 from a 9-bit conventional MASH 1-1-1. The sequence lengths of the HK-MASH and the MM-MASH are compared in Table II. The MM-MASH achieves a longer sequence when the word length is 8, 9, 10 and 11, and hence is deemed superior.

TABLE II
A COMPARISON OF THE SEQUENCE LENGTHS FOR THE HK-MASH AND MM-MASH.

Word length	HK-MASH	MM-MASH	Difference
8 bit	15.81×10^6	16.39×10^6	+0.58×10^6
9 bit	131.87×10^6	133.17×10^6	+1.3×10^6
10 bit	1.06×10^9	1.07×10^9	+10×10^6
11 bit	8.48×10^9	8.55×10^9	+70×10^6

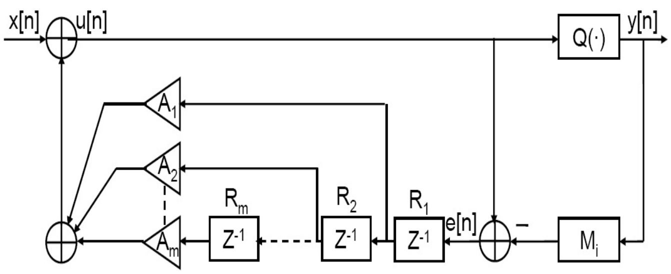

Fig. 5. Higher order error-feedback modulator.

III. THE ARCHITECTURE OF THE MM-EFM

A. The Sequence Length of the MM-EFM

The structure of an mth order EFM (EFMm) is illustrated in Fig. 5. The symbols $R_1, R_2, ..., R_m$ and $A_1, A_2, ..., A_m$ represent the initial condition and gain of the ith registers, respectively, where $i \in \{1, 2, ..., m\}$. The noise transfer function is

$$NTF = \frac{(Z-1)^m}{Z^m}. \tag{9}$$

The value of the gains A_i is obtained as:

$$\sum_{i=1}^{m} A_i Z^{-i} = 1 - NTF. \tag{10}$$

Now the calculation for the sequence length of a second-order EFM (EFM2) will be shown below as an example, since EFM2 is the most popular higher-order EFM in practice [4]. The coefficients $[A_1, A_2]$ are obtained from (10) as $[2, -1]$. The EFM2 is assumed as the pth stage in a MASH DDSM. Thus the state variable u is dependent on the output of previous stage:

$$u_p[1] = e_{p-1}[1] + 2R_1 - R_2. \tag{11}$$

Using (11), the error is expressed as

$$\begin{aligned} e_p[1] =& u_p[1] - M \cdot y_p[1] \\ =& e_{p-1}[1] + 2R_1 - R_2 - M_p \cdot y_p[1] \end{aligned} \tag{12}$$

After several time steps, the values of the registers are changed from their initial conditions to e_p. Then

$$e_p[2] = e_{p-1}[2] + 2e_p[1] - R_2 - M_p \cdot y_p[2] \tag{13}$$

$$e_p[3] = e_{p-1}[3] + 2e_p[2] - e_p[1] - M_p \cdot y_p[3] \tag{14}$$

$$\vdots$$

$$e_p[N_p] = e_{p-1}[N_p] + 2e_p[N_p - 1] - e_p[N_p - 2] - M_p \cdot y_p[k]. \tag{15}$$

The sum of all of the above equations (12)-(15) is

$$\begin{aligned} \sum_{k=1}^{N_p} e_p[k] =& \sum_{k=1}^{N_p} e_{p-1}[k] + 2\sum_{k=0}^{N_{p-1}} e_p[k] \\ & - \sum_{k=-1}^{N_{p-2}} e_p[k] - M_p \cdot \sum_{k=1}^{N_p} y_p[k] \end{aligned} \tag{16}$$

Since e_p is periodic with the period N_p [6] in the steady state,

$$\sum_{k=1}^{N_p} e_p[k] = \sum_{k=0}^{N_{p-1}} e_p[k] = \sum_{k=-1}^{N_{p-2}} e_p[k] \tag{17}$$

Then (16) becomes

$$\sum_{k=1}^{N_p} y_p = \frac{1}{M_p} \sum_{k=1}^{N_p} e_{p-1}. \tag{18}$$

If the relationship between the sequence length of the pth and $(p-1)$th stage EFM is

$$N_p = K \cdot N_{p-1} \tag{19}$$

(18) is modified to

$$\sum_{k=1}^{N_p} y_p = \frac{K}{M_p} \sum_{k=1}^{N_{p-1}} e_{p-1}. \tag{20}$$

Obviously, (20) is the same as (4). Thus, the sequence length of the EFM2 is same as that of the EFM1, if both of them are the pth stage in a lth stage DDSM. In other words and the crucial point, the sequence length of a MASH DDSM does not depend on the order level, but on the number of EFMs. For example, the period of MM-MASH 1-2 is

$$N = \frac{M_1 \cdot M_2}{\lambda} \tag{21}$$

where λ is a parameter to make N the least common multiple of N_1 and N_2. If the two conditions, C1 and C2, shown in Section II-C are satisfied, the maximum sequence length is

$$N = M_1 \cdot M_2. \tag{22}$$

This is same as the period of the MM-MASH 1-1.

B. The Setup of the Quantisation Moduli

M_1 is set as a prime number around 2^{n_0}. This is to make X and M_1 always mutual prime numbers and therefore satisfy C1. This condition must be satisfied to maximise the sequence length of the MASH DDSM and to make the sequence length independent of the value of input. In order to maintain the modulator output accuracy, the value of the input DC X is adjusted to

$$X = M_1 \cdot mean(y) \tag{23}$$

where $mean(y)$ is the required output to control the static frequency divider in a fractional-N frequency synthesizer.

In an l stage MM-MASH, there are l co-prime numbers around 2^{n_0} that need to be found in order to satisfy C2. The higher the modulator order, the greater difficulty in finding suitable values for these moduli. Fortunately, the most popular MASH DDSM in modern communication systems has only 2 or 3 stages [4]. Note that all of the quantizer moduli should be chosen no bigger than 2^{n_0} to avoid necessitating extra hardware. Some quantizer moduli chosen by the authors for a MM-MASH contains 3 stages EFMs are given in Table III.

TABLE III
SOME SAMPLE MODULI OF THE 3RD ORDER MM-MASH.

Word length	M_1	M_2	M_3
8 bit	251	256	255
9 bit	509	512	511
10 bit	1021	1024	1023
11 bit	2039	2048	2047

IV. SIMULATION RESULTS

All of the models of the EFM1, EFM and MASH are built and simulated in **Simulink**. The autocorrelation function [4] is used to determine the sequence length of the MASH DDSM. As seen in Fig. 6, the sequence length of a 9-bit MM-MASH 1-2 is 260608 and this equals $M_1 \cdot M_2$ as given in Table III.

The power spectrum is compared to examine the noise performance of the various architectures. The power spectral density [11] of the 9-bit MM-MASH 1-1-1 and 9-bit MM-MASH 1-2 is compared in Fig. 7. Both of these are 3rd order. It is evident from the figure that the MM-MASH 1-1-1 has a better noise performance than the MM-MASH 1-2. This is as expected as the sequence length of the former is longer than that of the latter as shown in Section III-A. However, the MM-MASH 1-2 has the advantage on less hardware requirements and so a balance between hardware cost and noise performance is required in the selection of the most suitable structure.

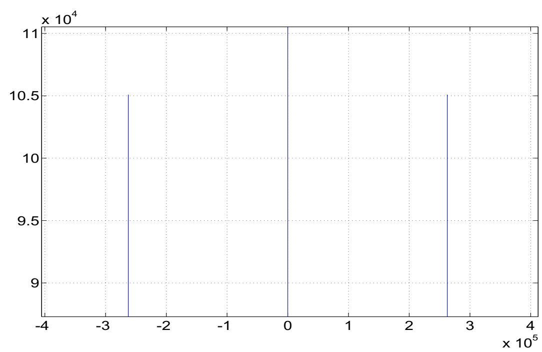

Fig. 6. The autocorrelation result for the 9-bit MM-MASH 1-2.

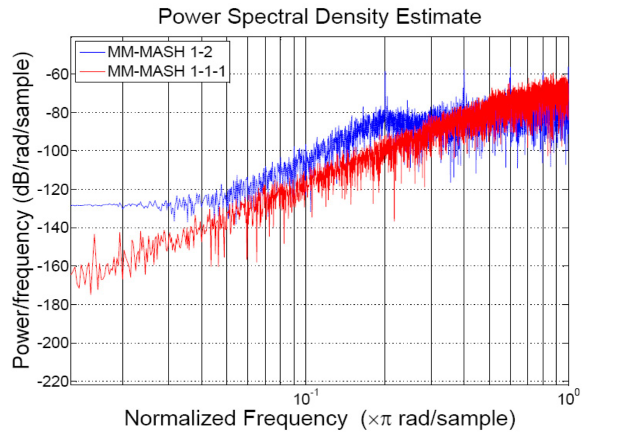

Fig. 7. The power spectral density of the dithered conventional MASH DDSM and non-dithered MM-MASH.

V. CONCLUSIONS

The structures of different MASH DDSMs are compared. The proposed MM-MASH has the longest sequence length and hence is advantageous from the perspective of noise performance. In this paper, the use of higher-order EFMs in the MM-MASH is investigated. The sequence length of the MM-MASH 1-1 is the same as the MM-MASH 1-2. It is shown that the MM-MASH 1-1-1 has the better noise performance than the MM-MASH 1-2. Both are 3rd order but the latter one requires less hardware. The decision regarding structure choice is therefore a balance between the noise performance requirements and the hardware requirements.

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REFERENCES

[1] D. Reefman, J. Reiss, E. Janssen, and M. Sandler, “Description of limit cycles in sigma-delta modulators,” *IEEE Trans. on Circuits and Systems-I: Regular Papers*, vol. 52, no. 6, pp. 1211–1223, June 2005.

[2] S. Pamarti, J. Welz and I. Galton, “Statistics of the Quantization Noise in 1-Bit Dithered Single-Quantizer Digital Delta-Sigma Modulators,” *IEEE Trans. on Circuits and Systems-I: Regular Papers*, vol. 54, no. 3, pp. 492–503, March 2007.

[3] S. Pamarti and I. Galton, “LSB Dithering in MASH Delta-Sigma D/A Converters,” *IEEE Trans. on Circuits and Systems-I: Regular Papers*, vol. 54, no. 4, April 2007.

[4] M. J. Borkowski, T. A. D. Riley, J. Häkkinen, and J. Kostamovaara, “A Practical $\Delta - \Sigma$ Modulator Design Method Based on Periodical Behavior Analysis,” *IEEE Trans. on Circuits and Systems-II: Express Briefs*, vol. 52, no. 10, pp. 626–630, Oct. 2005.

[5] K. Hosseini and M. P. Kennedy, “Maximum Sequence Length MASH Digital Delta-Sigma Modulators,” *IEEE Trans. on Circuits and Systems-I: Regular Papers*, vol. 54, no. 12, Dec. 2007.

[6] K. Hosseini and M. P. Kennedy, “Mathematical Analysis of a Prime Modulus Quantizer MASH Digital Delta-Sigma Modulator,” *IEEE Trans. on Circuits and Systems-II: Express Brief*, vol. 54, no. 12, Dec. 2007.

[7] T. Xu and M. Condon, “The MASH Digital Delta-Sigma Modulator with Multi-Moduli,” submitted to *IET Circuits, Devices & Systems*.

[8] R. E. Crandall and C. Pomerance, *Prime numbers: a computational perspective*, Springer, 2001.

[9] L. Sun, T. Lepley, F. Nozahic, A. Bellissant, T. Kwasniewski and B. Heim, “Reduced Complexity, High Performance Digital Delta-Sigma Modulator for Fractional-N Frequency Synthesis,” in *Proc. IEEE International Symposium on Circuits and Systems*, Orlando, USA, June 1999, vol.2, pp. 152-155.

[10] M. J. Borkowski and J. Kostamovaara, “Spurious Tone Free Digital Delta-Sigma Modulator Design for DC Inputs,” in *Proc. IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May 2005, pp.5601–5604.

[11] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing.* Upper Saddle River, NJ: Prentice-Hall, 1999.