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GaAs integrated circuits with normally-off processes : a real market opportunity

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INTRODUCTION

GaAs normally-off FET processes have now reached a maturity level such that their application domains extend to VLSI digital circuits, analogue and mixed-signal analogue/digital circuits. They represent a real market opportunity for the GaAs industry and several manufacturers both in the US and Europe offer now stabilised and industrial normally-off processes.

This paper describes typical representative normally-off processes and review the main application areas with a critical comparison between the competing technologies. Future trends are also presented.

PROCESS DESCRIPTION

The main manufacturers offering now normally-off processes are described in the following table :

MANUFACTURER/FOUNDRY	PROCESS CHARACTERIZATION
Triquint (US)	QED/A 3 Vt's, Au based gate mixed signal process
Vitesse (US)	Self align., refrac. gate VLSI process
Mitsubishi (J)	refract. gate + Au cap analogue process
NTT (J)	refract. gate + Au cap substitut. gate (SAINT) mixed signal processes
TRW (US)	E/D process
ITT (US)	refractory gate MSAG process mixed signal process
Rockwell (US)	QED/A (second source to Triquint)
TCM (France)	ED process refractory gate SAGA (derived from Vitesse's process) mixed signal process
PML (France)	ER07AD process 2 Vt's Au based gate mixed signal process

Triquint's QED/A has airbridge interconnect to reduce interconnect capacitances and offers three values of theshold voltages: -2V -0.6V and +0.15V.

Refractory self-aligned gate processes as defined for digital applications are not optimum for analogue circuits because they have a high gate resistance (square resistance of a few ohms compared with 0.1 ohm for conventional Ti/Pt/Au) and a low drain breakdown voltage (below 5V).These limitations have been addressed by several foundries such as ITT, Mitsubishi and Thomson TCM.An example of refractory gate self aligned mixed signal process is ITT's MSAG (Multifunction self aligned gate) (7).A titanium tungsten nitride gate is patterned by Reactive Ion Etching. Symmetric FET's are fabricated for digital elements.For low-noise and power elements a photoresist spacer is used during source and drain areas implantation to move the highly doped drain area from the gate thus improving the breakdown voltage.Gate length is 0.4 micron. The gate resistance is reduced by post alignment of a gold cap. This approach is preferred to the use of multifingered transistors which reduces the gate resistance but at the expense of process complexity and large parasitic capacitances.

NORMALLY-OFF DIGITAL LSI AND VLSI CIRCUITS AND APPLICATIONS

1. Present market and perspectives

The world GaAs IC merchant market for digital circuits (excluding development funding) is estimated (8) to grow from 83 millions US $ in 1991 to 300 to 400 millions US $ in 1995.The majority of this market will be based on normally-off processes.

The main growth incentive is in the US where several mainframe manufacturers are working on the insertion of GaAs ASICs in their system.46% of the market of GaAs digital circuits will be for the computer industry in 1995. As an example, Convex puts on the market the C3800 computer series which can be configured with 1 to 8 processors comprising GaAs chips fabricated with H-GaAs III Vitesse's process.

2. Competing technologies

GaAs digital circuits are facing fierce competition essentially from silicon bipolar and BICMOS processes.

Since bipolar circuits are limited in integration level by power dissipation, the comparison is especially valid up to medium scale integration (a few 10,000 gates) circuits.In this category, very impressive results have been published recently with silicon bipolar circuits : 8 bit 650 MHz ADC (4.5 W) (9) and 30 Gbit/s 2:1 and 1:2 mux demux (10). There is no clear advantage in terms of speed but for certain applications at the same speed GaAs VLSI circuits dissipate 3 to 4 times less.This would mean that air cooling could be used in large computers instead of water cooling. Wherever this power dissipation issue is less critical,the question of the usefulness of GaAs digital circuits remains open.

BICMOS and CMOS are the technologies of choice for very large scale integration but the gap with GaAs circuits has narrowed recently (1 million gates for CMOS compared with 350,000 for GaAs). Furthermore since the power consumption of CMOS increases linearly with frequency, GaAs circuits are less power consuming for clock rates above 200 MHz.

III-V HBT is another alternative technology. It is not mature enough now but will certainly play a role towards the end of the decade.Very promising results have been obtained recently: 27 GBit/s 4:1 mux (11),36 GHz divider (12) for instance.

3. Application examples

The following table shows representative examples of state of the art components:

- the high impedance semi-insulating substrate enables an easy integration of good quality factor inductances and low parasitics capacitors.
- MESFET show a much lower noise figure (Fmin about 1 dB at 4 GHz compared to 4 dB for bipolar transistors).This good noise performance is hardly dependent on the gate width and enables the fabrication of ultra-low DC power low noise amplifiers (4 mW, 2.5 dB NF at 2 GHz).

GaAs MESFET free running oscillators show a larger phase noise because of the conversion of the 1/f noise.However the difference vanishes when comparing PLL synthesizers because GaAs prescalers have similar phase noise performance as silicon ones.

As for digital circuits the key factor is price: GaAs high performance mixed signal circuits can be produced in large quantities at costs around 3 US $ which is 4 times higher than high end silicon bipolar circuits.The difference is however small enough to enable system manufacturers to insert GaAs components because of their superior performance (21).

3. Application examples

A whole range of basic GaAs cells have been demonstrated : low noise amplifiers, VCO's, frequency synthesizers, IF amplifiers, single and double balanced mixers, image rejection mixers.

TYPE OF CIRCUIT	FOUNDRY/ PROCESS	CIRCUIT CHARAC.	APPLIC.
L band Low noise amplifiers (22)	ER07AD PML	*NF = 1.6 dB, G = 21 dB IP3out = 13 dBm, P = 40 mW NF = 2.5 dB, G = 10 DB IP3out = -3 dBm, P = 3.6 mW avail. plast.pack.	mobile comm.
L band downconv.(3)	ER07AD PML	RF = 0.95-2GHz conv.gain = 9 dB NF (SSB) = 11 dB LO leakage at RF -30 dBm P = 130mW avail. plast.pack.	
L band downconv.(3)	QED/A Triquint	RF = 0.8-2GHz conv.gain = 22 dB NF (SSB) = 4 dB no integ. LO P = 60mW	mobile comm.
Receiver downconv. DSP(23)	QED/A Triquint/ Rockwell	5 channels	GPS
L band image reject. mixer (24)	PML ER07AD	30 dB rej. (500 MHz) NF = 2 dB P = 120 mW	mobile comm.

FUTURE TRENDS

Future developments of E/D processes will be along 2 directions

- smaller gate width (0.2 micron) together with thinner active layers and buried p type layers will gain more acceptance.Their usefulness has already been demonstrated by NTT (18).