COMPUTER SIMULATION OF GaAs AND SOI DEVICES USING TCAD TOOLS: AN REU PROJECT

Ashok Goel, Sarah Bergstrom* and Aleli Mojica-Campbell**

Department of Electrical Engineering
Michigan Technological University
Houghton, MI 49931 (USA)
E-mail: goel@mtu.edu
WWW: http://www.ee.mtu.edu/faculty/goel

Abstract --- **An undergraduate research project is outlined whose goal was to use the TCAD tools to simulate the performances of GaAs- and SOI-based devices and to compare them with the corresponding silicon-based devices. Students used the Silvaco Corporation's "Virtual Wafer Fab" (VWF) package consisting of process simulation software called ATHENA, device layout software called DevEdit and device simulation software called ATLAS to simulate GaAs, SOI as well as conventional silicon devices. They explored the capabilities of these TCAD programs for five different GaAs and SOI devices including short- and long-channel JFETs, digital GaAs E-MESFETs, HEMTs and SOI BJTs.**

I. INTRODUCTION

Active research experience is one of the most effective techniques for training and motivating undergraduate students for careers in science and engineering. In the USA, National Science Foundation (NSF) recognizes this and supports undergraduate research under two programs:

a) Under their "Research Experiences for Undergraduates (REU) Supplements" program, NSF encourages principal investigators of NSF-funded research grants to include one or two undergraduate students in their existing projects.

b) Under their "REU Site" program, NSF provides funds to set up undergraduate research sites consisting of nearly ten students to work on state-of-the-art research projects under the supervision of a faculty member.

Continuous advances in integrated circuit technology have resulted in smaller transistor dimensions, larger chip sizes and increased complexity. There is an increasing demand for circuits with higher speeds and higher component densities. Because of its semi-insulating property and the fact that the mobility of electrons is an order of magnitude higher in Gallium Arsenide (GaAs) substrate than in the widely used Silicon substrate, GaAs has emerged as a preferred substrate for the development of very high-speed integrated circuits [1,2]. In fact, during the last few years, GaAs technology has emerged rapidly from basic research to device and circuit development. In addition, growth of GaAs on silicon (Si) substrate has met with a great deal of interest because of its potential applications in the new hybrid technologies. GaAs-on-Si unites the high speed and optoelectronic capability of GaAs circuits with the low material cost and superior mechanical properties of the Si substrate. The heat sinking of such devices is better since the thermal conductivity of Si is three times more than that of GaAs. This technology is expanding rapidly from material research to device and circuit development. Functional GaAs SRAMs of up to 1K in complexity have been demonstrated on Si substrate. LED modulation rates up to 27 Mbit/s have been demonstrated on monolithically integrated GaAs/AlGaAs LEDs and Si MOSFETs. Further, it may be recalled that CRAY-4 supercomputer is based primarily on the GaAs-based high-speed circuits. Recently, Silicon-on-Insulator (SOI) technology has also been adopted as a preferred technology by IBM and Motorola [3].

In this paper, a research project carried out by the undergraduate students at the undergraduate research site on GaAs-based high-speed circuits set up at the Michigan Technological University is summarized.

II. UNDERGRADUATE RESEARCH SITE

During summer 1998, funded by a three-year grant from the National Science Foundation, an undergraduate research site was established for the second year at the department of Electrical Engineering at Michigan Technological University in the area of GaAs-based very high-speed integrated circuits. This site consisted of ten undergraduate students selected on a competitive basis from institutions all over the USA. Eligibility criteria for participation were:

a) Citizenship or permanent resident of the United States.

b) Completion of at least two years in electrical engineering, physics, computer science, computer engineering or a related field with a grade point average of 3.0 or over.

Major objectives of this REU site were:

a) Enhancement of student experience, competence, confidence and self esteem by working on a state-of-the-art electrical engineering research project.

b) Encouragement of students to pursue graduate studies in electrical engineering and to choose a career in microelectronics/VLSI research.

c) Improvement of student oral and written skills through written report and formal presentations.

In addition to the host institution, students were selected from University of Notre Dame, State University of New York at Buffalo, University of Texas at El Paso, Swarthmore College, University of Florida, University of Illinois at Urbana-Champaign and Rice University. Undergraduate students worked with electrical engineering graduate students and faculty members for ten weeks on projects [4, 5] ranging from designing a GaAs-based floating point adder/subtractor [6] and a GaAs-based mini central processing unit to modeling the electromigration-induced failure effects in the high-speed VLSI interconnects [7] to computer simulations of GaAs- and SOI-based devices and circuits using the various technological computer-aided design (TCAD) tools. Faculty interaction was maximum during the first few weeks and decreased as students became more and more independent in carrying out their projects. During the last week of the REU site, students submitted formal written reports and presented formal seminars on their projects.

III. UNDERGRADUATE RESEARCH PROJECT

First, REU students compared the GaAs technology with the TTL, ECL and CMOS technologies. This was done by simulating the power consumption/gate and propagation delay/gate in a 381 ALU designed by using each of the four technologies. These results are shown in Table 1. This table shows that while GaAs technology results in lowest propagation delays among the four technologies, its power consumption, though lower than the TTL and ECL technologies, is greater than the CMOS technology. An REU student also investigated the rapidly emerging Silicon-on-Insulator (SOI) technology for high-speed integrated circuits and concluded that the SOI technology results in higher circuit speeds, lower power consumption and greater immunity to radiation-induced errors and is compatible with the existing IC fabrication processes.

TABLE 1
Comparison GaAs technology with the TTL, ECL and CMOS Technologies

	TTL	ECL	CMOS	GaAs
Power dissipation/gate	16 mW	25 mW	10 nW	0.5 mW
Switching speed/gate	4 ns	2 ns	10 ns	50 ps
Power dissipation/ALU	0.53 W	0.82 W	32 uW	164 mW
Delay/ALU	26 ns	12 ns	320 ns	700 ps

Students realized that, as device sizes shrink and new materials are added, it becomes more expensive, time-consuming and physically difficult to test each component and that device simulations using the semiconductor technological computer aided design (TCAD) tools is an economical alternative to experimental testing saving large amounts of time, money and other resources. They worked on a project whose goal was to use the TCAD tools to simulate the performances of several GaAs- and SOI-based devices and to compare them with the corresponding silicon-based devices. They realized that while silicon is still the cheapest and most widely available material for integrated circuits (ICs), several products including many high-frequency low-power communication devices are possible only by using the newer more expensive materials such as SOI and III-V semiconductors, especially GaAs. They found out that the Silvaco Corporation's "Virtual Wafer Fab" (VWF) package consisting of process simulation software called ATHENA, device layout software called DevEdit, device simulation software called ATLAS and TonyPlot for displaying results could be used to simulate GaAs, SOI as well as conventional silicon devices. They explored the capabilities of these TCAD programs for five different GaAs and SOI devices including short- and long-channel JFETs, digital GaAs E-MESFETs, HEMTs and SOI BJTs. For example, the doping profile in a GaAs E-MESFET using ATHENA is shown in Fig. 1, that in an SOI-based FET is shown in Fig. 2 and the I-V curves for a long channel GaAs MESFET for various gate biases obtained by using ATLAS are shown in Fig. 3. The schematic diagram of a GaAs-based High Electron Mobility Transistor (HEMT) constructed by using DEVEDIT is shown in Fig. 4.

These simulations were designed to show both the efficacy of the materials and the simulation programs themselves.

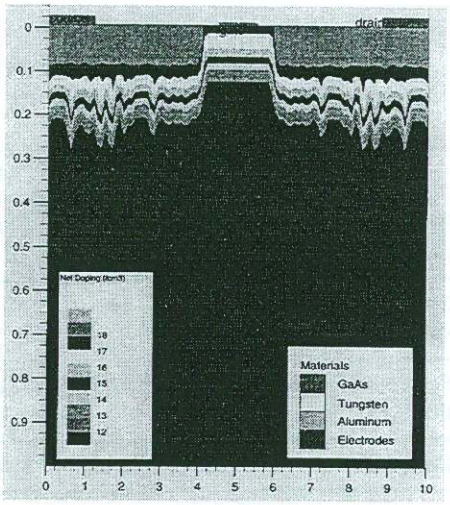

Fig. 1: Doping profile in a GaAs E-MESFET using the TCAD tool called ATHENA

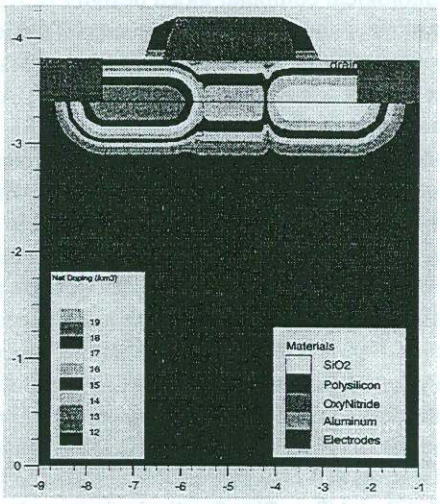

Fig. 2: Doping profile in an SOI-based FET structure using ATHENA

IV. ACKNOWLEDGEMENTS

This work is based on research supported by a grant from the National Science Foundation under Grant no. EEC-9619646. Authors like to thank Wen-Szu Lin and Tolga Aytek for their help during this project. The support provided by the Michigan Technological University is also acknowledged.

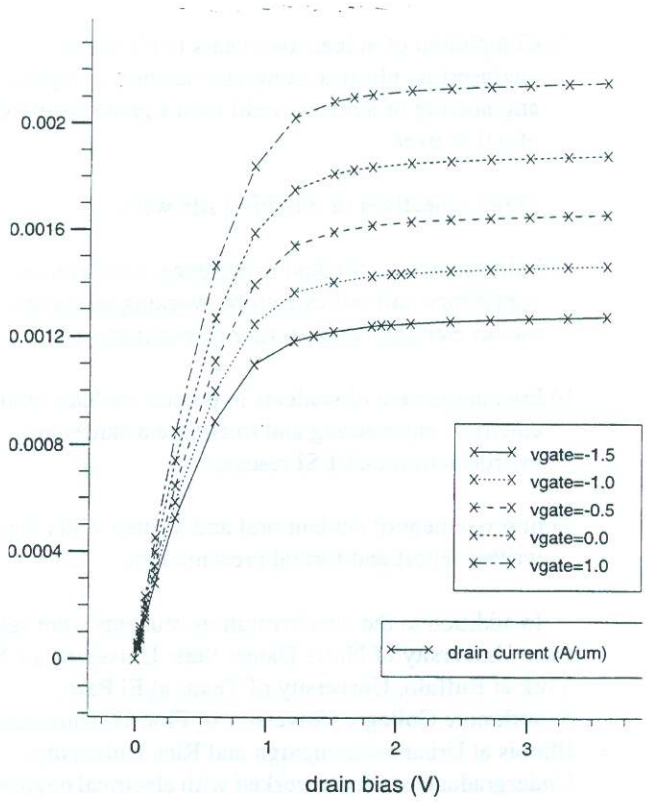

Fig. 3: I-V curves for a long channel GaAs MESFET for various gate biases obtained by using ATLAS

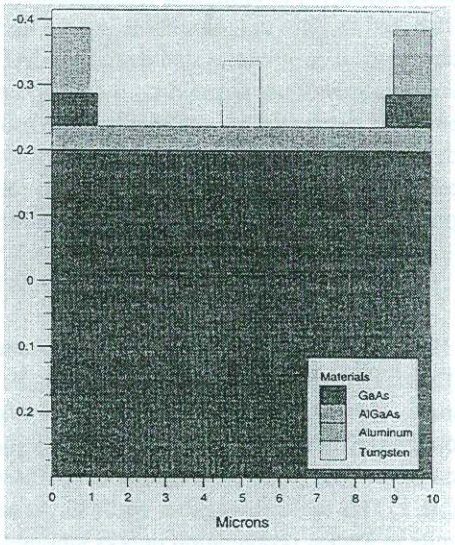

Fig. 4: The schematic diagram of a GaAs-based High Electron Mobility Transistor (HEMT) constructed by using the TCAD program called DEVEDIT

V. CONCLUSIONS

We have successfully used the various TCAD tools to simulate the performance of several GaAs and SOI based devices. This shows that, in the present age of ever emerging new devices with shrinking dimensions, device simulations using the semiconductor technological computer aided design tools is an economical alternative to experimental testing saving large amounts of time, money and other resources.

VI. REFERENCES

* Visiting undergraduate student from the Swarthmore College, Pennsylvania, USA

** Visiting undergraduate student from the University of Texas at El-Paso, Texas, USA

[1] I. Deyhimy, "Gallium Arsenide Joins the Giants," *IEEE Spectrum*, pp. 33-40, Feb. 1995

[2] R.C. Eden, A.R. Livingston and B.M. welch, "Integrated Circuits: The Case for Gallium Arsenide," *IEEE Spectrum*, pp. 30-37, Dec. 1983.

[3] M.L. Alles, "Thin Film SOI Emerges," *IEEE Spectrum*, 1997.

[4] A.K. Goel, M.E. Sloan, T. Aytek, S. Bachhuber, R. Cadena, F. Damstra, L. Huynh, B. Jesiek, P. Kern, D. Lemmer, W. Lin and K. Price, "Research Experiences for Undergraduates in Design, Modeling and Measurements of GaAs-Based Very High-Speed Integrated Circuits," *Proc. American Society for Engineering Education North Central Section Spring Conf.*, pp. 54-58, April, 1998

[5] A.K. Goel, M.E. Sloan, S. Bergstrom, A. Mojica-Campbell, C.T. DuBois, M. Innus, Y.J. Lu, J. Meteer, S. Palmer, N. Ramler and V.A. Singh, "Research Experiences for Undergraduates in Design, Modeling and Measurements of GaAs-Based Very High-Speed Integrated Circuits" Proc. ASEE Annual Conf., 1999.

[6] A.K. Goel, F. Damstra and B. Jesiek, "Gallium Arsenide Based Floating Point Adder/Subtractor," *Proc. 13th Int. Conf. Computers and Their Applications,* pp. 348-351, March 1998.

[7] A.K. Goel, L. Huynh and B. Jesiek, "Computer Simulation of Crosstalk in the VLSI Interconnections: An REU Project," *11th Int. Conf. Comp. Appl. Industry & Engrg*, Nov. 1998.