High linearity of double channel GaAs pHEMT using a very high selective wet etching

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ABSTRACT

Realisation and characterisation of $Al_{0.22}Ga_{0.78}As/In_{0.22}Ga_{0.78}As/GaAs$ multifinger linear power pHEMT's, using a citric acid selective wet etching for the gate recessing, are reported. A very high uniformity of the drain current and the threshold voltage values have been obtained. This high linearity is confirmed by a quasi flat transconductance over a wide gate source voltage. Power and intermodulation distortion at 16 GHz are also reported. A maximum output power of 1.1 W/mm and an IP3 value of 25 dBm have been measured.

I. INTRODUCTION

Linear solid state power amplifiers are required for microwave and millimetre wave wireless or space communication applications. To limit third order intermodulation distortion generated by power amplifiers, it is necessary to reduce the device nonlinearities. By the way, GaAs material is a good candidate for space applications due to its low radiation. Actually, the AlGaAs/InGaAs pHEMT has demonstrated its capability to deliver a high power density of 1 W/mm at 30 GHz [1].

From this generic pHEMT structure, we started an original work based on a two channel pHEMT to get high power and high linearity simultaneously. The upper channel is in GaAs and the other is in InGaAs. As power applications are aimed, multifinger structures with large total gate width are necessary. So the technological process requires a high uniformity to get identical electrical performance along each gate finger.

We report the application of a citric acid/hydrogen peroxide/ammonium hydroxide solution to etch selectively the gate recessing of AlGaAs/InGaAs/GaAs multifingers pHEMTs. The device processing is presented in the first part. The second part is about DC characterisation with the electrical characteristics uniformity and the extrinsic transconductance evolution. And the last part concerns RF measurements, including small signal Sij measurements to get the electrical element and large signal measurements, with intermodulation distortion performance at 16 GHz.

II. DEVICE PROCESSING

The pHEMT structure used in this study was grown by solid source molecular beam epitaxy. The epilayer has been optimized using 1D modelling software based on Schrödinger-Poisson equation resolution [2]. Our optimization criterion is the linearity of the charge control. So it consists of a 70 nm n^+ GaAs cap layer with a doping level of $5x10^{18}$ cm^{-3}, a 20 nm undoped $Al_{0.22}Ga_{0.78}As$ Schottky barrier, a first Si δ-doping (δ1) with an undoped GaAs channel followed by a second Si δ-doping (δ2) with an undoped $In_{0.22}Ga_{0.78}As$ channel (Fig.1).

Layer	Thickness
GaAs $5x10^{18}cm^{-3}$	70 nm
$Al_{0.22}Ga_{0.78}As$	20 nm
GaAs	0.4 nm
δ1	
GaAs	0.4 nm
$Al_{0.22}Ga_{0.78}As$	3 nm
GaAs	12 nm
AlAs/GaAs 6x	5 nm
δ2	
GaAs	0.4 nm
$Al_{0.22}Ga_{0.78}As$	2 nm
GaAs	1 nm
$In_{0.22}Ga_{0.78}As$	12 nm
GaAs	1.5 nm
$Al_{0.22}Ga_{0.78}As$	150 nm
GaAs	300 nm
GaAs Substrate	

Figure 1: Schematic of the pHEMT structure

Two epilayers have been grown, the first with $\delta1=\delta2=3.5x10^{12}cm^{-2}$ will be named device A and the second with $\delta1=\delta2=4x10^{12}cm^{-2}$ will be named device B.

In our application, we need the maximum of aluminum concentration in the high band gap layer to obtain a good electron confinement in the channel, a high barrier discontinuity [3] and a better control of the gate recessing because the selectivity between GaAs and AlGaAs increases with the aluminum concentration [4]. But in the case of an important Al mole fraction, problems could appear due to DX-Centers [5]. So, we have chosen an Al mole fraction of 22% to minimize these problems.

The process fabrication started with device isolation through mesa etching. The Ni/Ge/Au/Ti/Au ohmic contacts were annealed at 400°C during 40 s. A contact resistance of 0.07 Ω.mm is obtained. The source drain distance is 1.3 µm. The 0.2 µm centered gate length is defined by electron beam lithography. We have developed a new citric acid / hydrogen peroxide selective wet etching to perform the gate recessing [6]. The pH of the solution is adjusted by ammonium hydroxide. For a pH value of 6.4, the selectivity is better than 200 at room temperature. Moreover, our study has shown a very good surface morphology of the etched material and a large stability of the solution over the time. Ti/Pt/Au is evaporated for the gate metallization. A 500 Å Si_3N_4 film is deposited in a plasma enhanced chemical vapor deposition reactor to passivate the device and to minimize the effects of electrical stress on the gate breakdown voltage [7].

III. DC CHARACTERISATION

The I-V characteristics at room temperature of a $8*50*0.2\ \mu m^2$ pHEMT is presented in Fig 2.

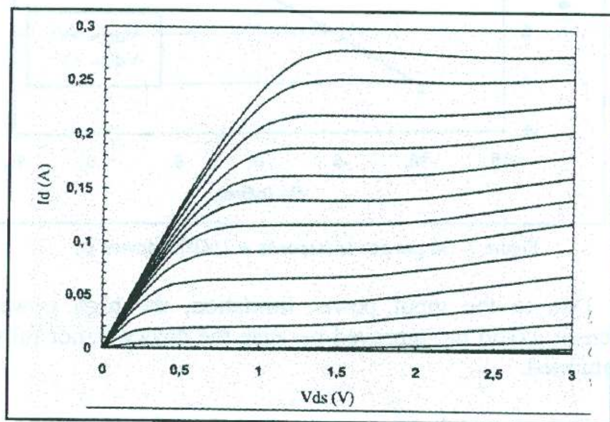
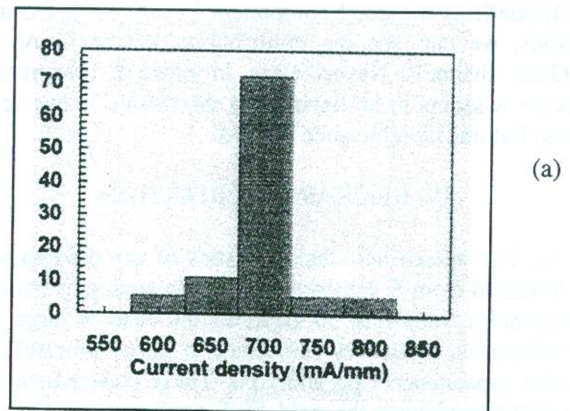


Figure 2: 8x50 µm IV characteristics of the device A
Vgsmax=0.8 V, Vgs step = 200 mV

The maximum drain current value is 700 mA/mm at Vgs=0.8V with a breakdown voltage of 7 V in transistor configuration. It clearly presents a linear variation versus the gate source voltage. Fig. 3 shows the drain current density and the pinch-off voltage histograms measured across the sample and realised for more than 100 components with different gate developments (from 2x20 µm to 8x75µm).Very good standard deviation values of 39 mA/mm and 32 mV have been obtained respectively for the drain current density and the pinch-off voltage. This Vth standard deviation measured for large gate width multifinger transistors is better than what has been reported in the litterature for monofinger transistors using dry etching [8]. It is probably due to the higher selectivity of the citric acid solution we used.



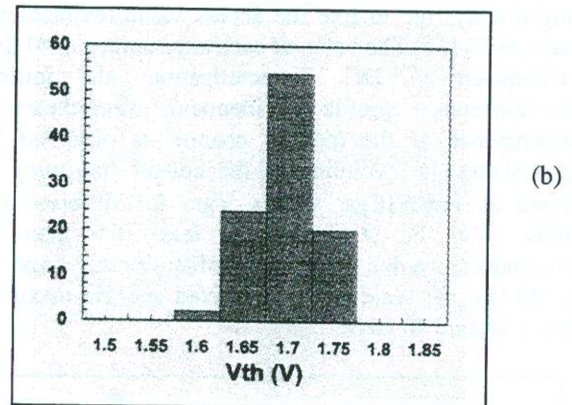


Figure 3: Drain current (a) and pinch-off (b) histograms for the device A

The extrinsic transconductance is quasi flat over a wide gate source voltage of 2 V with a maximum value of 350 mS/mm fig. 4.

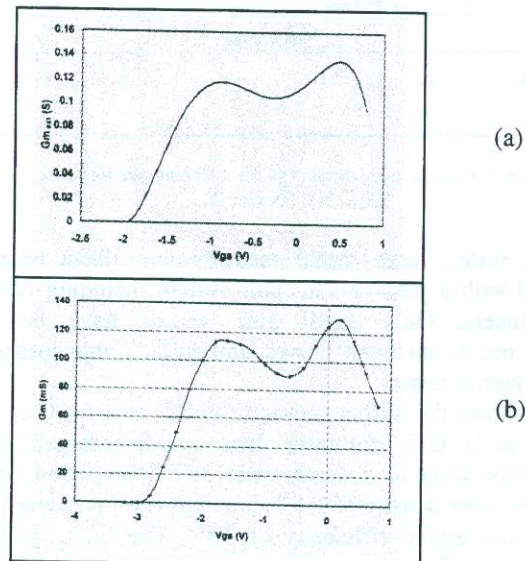


Figure 4: Evolution of the extrinsic transconductance versus Vgs at Vds=2 V for the device A (a) and B (b)

It confirms the good component linearity [9]. On these graphs, we can see the contribution of the GaAs and InGaAs channels. Nevertheless, in terms of linearity, the device A seems to be better than the device B due to the quasi flat transconductance profile.

IV. RF CHARACTERIZATION

A) The microwave characteristics of the devices were determined from S parameter measurements, performed at frequencies from 1 to 50 GHz. In the case of large gate development, it is very important to know precisely the access capacitance Cpg and Cpd. These capacitances can be determined with the cold FET configuration [10] and using a scaly rule to fixe the access value (extrapolating data at w=0) [11] The value of each capacitance is 40 fF.

Compared to DC characterization, the intrinsic transconductance profile is identical. Nevertheless, a predominance of the InGaAs channel is observed [2]. Fig. 5 shows the evolution of the cut-off frequency Fc, defined as gm/2ΠCgs, versus Vgs, for different gate widths. The Fc evolution is less flat than the transconductance due to the Cgs profile. On this graph, we can see that the scale law is respected and the maximum value is around 70 GHz.

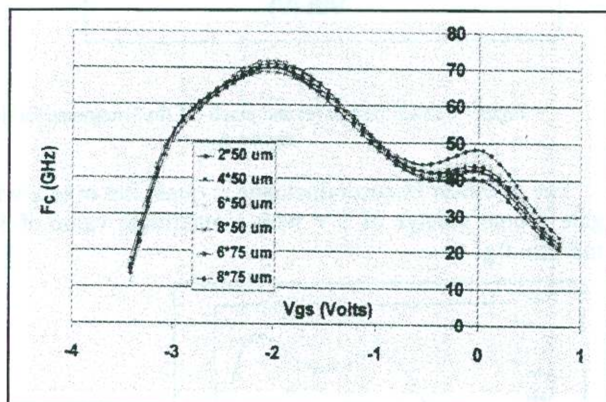


Figure 5: Fc evolution versus Vgs for different gate widths at Vds = 3 V (Device B)

B) On wafer, large signal measurements have been performed with a passive load pull system including two manual tuners. Only small gate widths have been measured due to an input power limitation. Cable losses are taken into account.

Fig. 6 shows the output power response of a 6x20 µm device A at 16 GHz, for three drain-source voltages, at Vgs corresponding to a weak class AB polarisation. A maximum power density of 1.1 W/mm has been measured, with a power added efficiency of 37%. The linear gain value is arround 9.5 dB.

The same characterization is reported in Fig. 7 for the device B. The output power density is now 1.025 W/mm, and a power added efficiency of 30%, with a linear gain value of 10 dB.

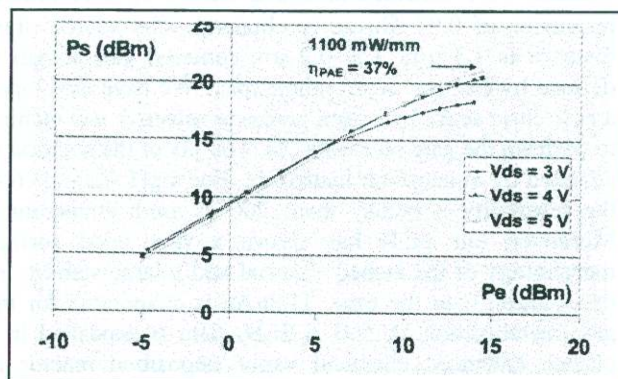


Figure 6: Output power response at 16GHz (device A)

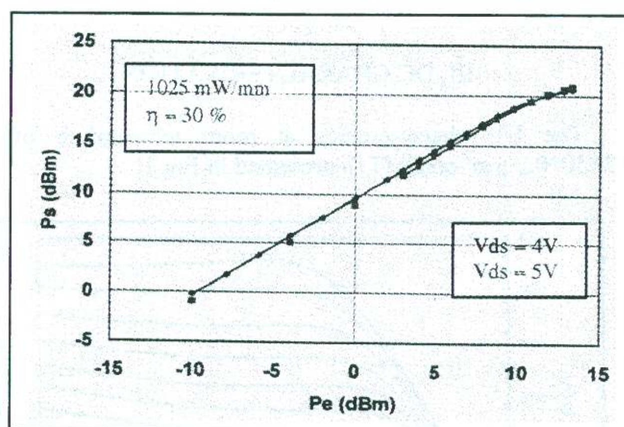


Figure 7: Output power response at 16GHz (device B)

Due to the input power limitation, the high power density could be improved because the device is not fully saturated.

C) Intermodulation measurements have been performed with the same principle excepted that tuners have been take off. Output power response have been reported in Fig. 8 in the case of F1=16 GHz and F2=16.01 GHz for three values of Vds.

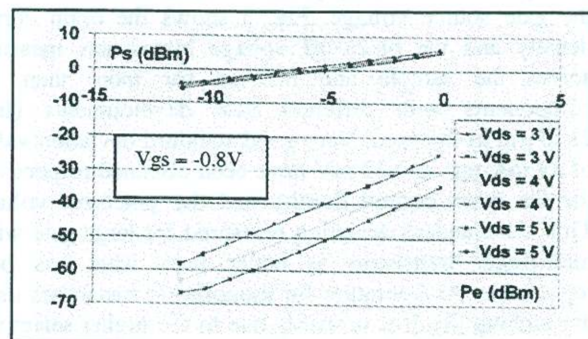


Figure 8: Intermodulation power response at 16 GHz (device A)

The C/I ration increases as Vds increases. This can be explained by the fixed load value of 50 Ω which is more suitable as Vds increases. This behaviour could be different in the case of tuner at the input or output device plane. Nevertheless, an IP3 value of 25 dBm has been found.

V. CONCLUSION

The uniformity improvement of linear power pHEMTs electrical characteristics using a very high selective wet etching is reported. Low standard deviations of 39 mA/mm and 32 mV have been obtained for the drain current and the pinch-off voltage on multifinger transistors, respectively. A quasi flat transconductance has been measured over a wide gate source voltage of 2 V. This results confirm the good device electrical uniformity. Large signal measurements also indicate the good capabilities of the device to get simultaneously high linearity and high power density, with an IP3 of 25 dBm.

VI. ACKNOWLEDGMENT

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VII. REFERENCES

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