A highly integrated MMIC chipset for 28 GHz LMDS Applications

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Abstract – This paper is intended to give an insight in the development of PHEMT multifunction MMICs (MFC) in the millimetre wave frequency range. It applies to the fast growing Local Multipoint Distribution System (LMDS) market, offering a two-chip solution for the subscriber transceivers. The focus is on the up and down converter dedicated to the Customer Premise Equipment (CPE) at 28GHz. These two chips include a sub-harmonic mixer, a buffer amplifier for the local oscillator and a low noise amplifier used either as a LNA (for Rx) or transmit driver (for Tx). The design was oriented toward low chip-size in order to being able to reach the cost requirement for such systems. Results are shown from a demonstrator assembly built with these two MMICs MFCs.

I. INTRODUCTION

The availability of millimetre-wave short haul communication systems opens the door to a low-cost and truly broadband wireless access to interactive multimedia services (telephone, video, computer data), targeting residential family entertainment as well as business operations. The so-called LMDS system (Local Multipoint Distribution System) is actively developed for this purpose, and will be operated in the 27.5-31.3GHz frequency band. The quantities foreseen for this market are huge as compared to the volume of production on today's market. This implies to reduce the number of components required to build such radios. This opens the way to producible highly integrated millimetre wave multifunction.

In this paper, we present the performances of the first pass of the 28GHz MMIC chipset developed for this application. The feasibility is then demonstrated. Using this MMIC chipset, a complete transceiver module can be easily designed with a reduced parts number leading to decrease the overall cost of the radio.

II. CHIP-SET DESCRIPTION

A. Description of the 28GHz LMDS MMIC chipset

The block diagram of the LMDS transceiver front-end is given in Fig.1.

It is composed of a receiver and a transmitter (for the return path). This transceiver has been designed to use the LMDS 27.5-31.3GHz frequency band and to be fully compatible with the DTH (Direct-To-Home) standard format for the satellite digital TV broadcast, using the same 0.95-2.15GHz intermediate frequency (IF) band.

A full MMIC solution has been retained, and two complex multifunction MMICs have been designed:

- a receiver MMIC, including a LNA and a down-converter mixer ;
- an up-converter MMIC, including a mixer and a driver amplifier ;

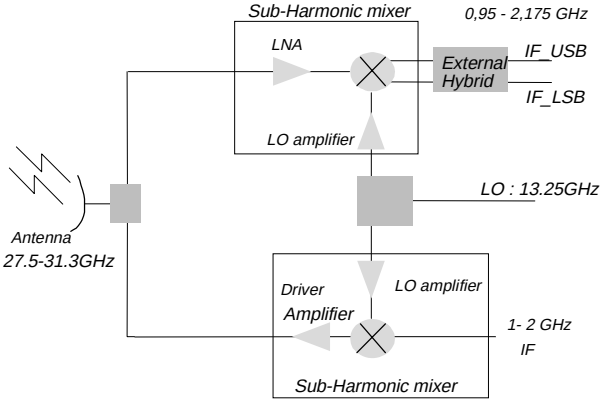

Fig.1 : Block diagram of the transceiver

All MMICs use UMS pseudomorphic HEMT MMIC process (PH25) with 0.25µm Al gates, dedicated to very low-noise and small/medium signal circuits up to 40GHz.

The photograph of the demonstrator assembly is given in figure 2. The purpose of this assembly is to demonstrate the functionality of the MMICs and not at all to realise a real radio for LMDS. The local oscillator (LO) is fed on the left access while the RF input (top) and RF output (bottom) are available on the right hand. For both transmit and receive, we use identical external SMD broadband quadrature coupler.

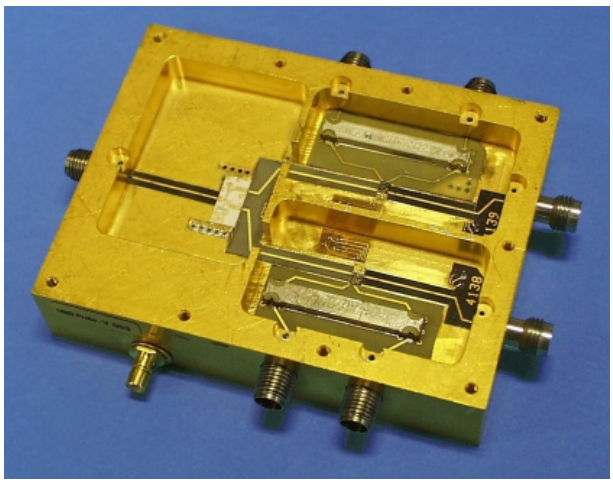

Fig.2 : Photograph of the LMDS transceiver demonstrator at 28GHz.

B. Receiver circuit

The receiver circuit MMIC integrates a 28GHz LNA, a 14GHz local oscillator buffer amplifier and a sub-harmonic single side band mixer (IRM and LO suppression). The sub-harmonic approach was chosen in order to reduce the required chip-size. It suppresses the need for a multiplier, and allows to design a Single Side Band (SSB) mixer with half the size as compared to a fundamental mode mixer, thanks to the anti-parallel topology of the diodes. This particular topology naturally suppresses the second harmonic of the LO at the output of the mixer. So, to realise a SSB mixer, we only need two individual cells balanced in quadrature. Furthermore, this topology is usable for both up and down conversion.

The in-phase and 90° RF signals are obtained using a Lange coupler and the IF signals must be recombined off-chip for image frequency rejection. The overall measured conversion gain of the receiver circuit is typically 3.0dB in Upper Side Band (USB), with a noise figure of 5.0dB and the image frequency rejection is better than 10dBc. The results in Lower Side Band (LSB) are slightly better due to a different combination of the slope in frequency of the IF filter and the RF one.

The LO buffer amplifier is useful to isolate the mixer from the external (assembly) and also to reduce the required power for the LO (typically 0dBm) that may radiate from the bonding wire. This feature is very important to reduce the level of the spurious in the radio, as the specifications are more and more demanding on these aspects. The layout of this MMIC is displayed in figure 3. The chip-size is 4.2mm².

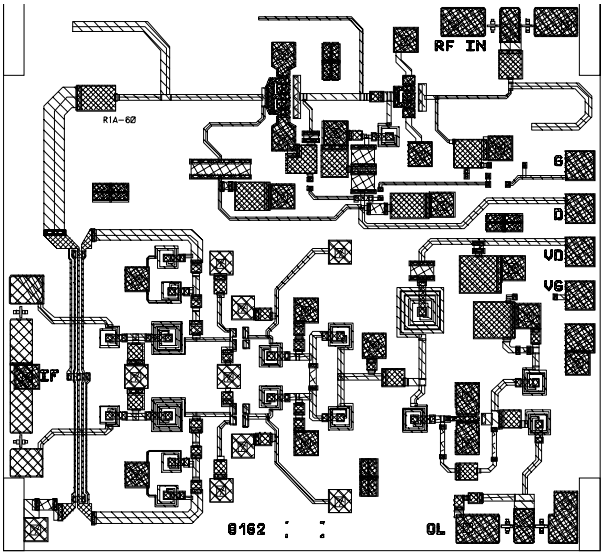

Fig. 3 : Layout of the down-converter MFC.

Two accesses are provided for the IF in order to use the IF external quadrature combiner for the image suppression.

The LNA is designed around a two-stage topology providing typically 15dB of gain and exhibits below 2.5dB of noise figure in the 27-32GHz frequency band. These results shown in figure 4 include all the effects of the assembly and external hybrid combiner (figure 2).

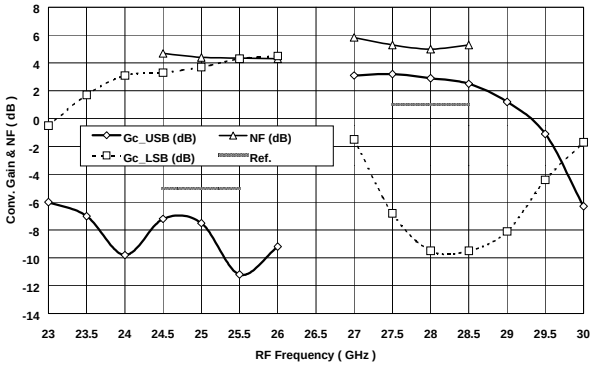

Fig. 4 : Conversion Gain (USB & LSB), Image Suppression and Noise Figure.

C. Transmitter circuit

The circuit is a MMIC up-converter which integrates a LO buffer amplifier, a single side band (SSB) mixer for LO and image suppression, and a two-stage driver amplifier. The layout of this MMIC is displayed in figure 5. The chip-size is 4.2mm².

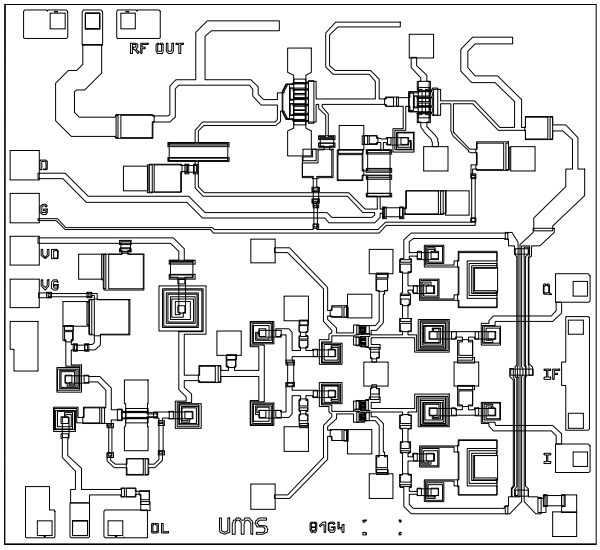

Fig. 5 : Layout of the up-converter MFC.

The SSB mixer is composed of two mixer cells based on anti-parallel diodes. The in-phase and 90° RF signals are combined through a Lange coupler to feed the driver amplifier. The topology of this MFC is the same than for the receiver, with a mirrored connection of the low noise amplifier. The results from the demonstrator are displayed on figure 6.

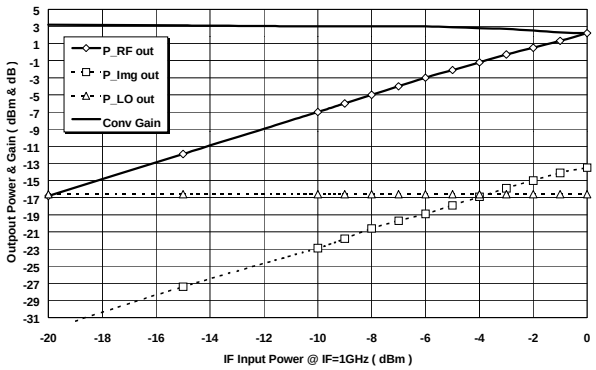

Fig. 6 : Up-Converter Pin/Pout
and LO leakage @ 27.5GHz RF.

The conversion gain for an IF frequency of 1.0GHz is typically +3.0dB and the LO to RF isolation at the RF port is better than 15dBc for -5.0dBm IF input power. The image suppression is 16dBc. The Pout for 1dB gain compression is achieved for an input power of 0dBm. The biasing conditions are Vd=+3.5Volt and Id=220mA. The figure 7 shows the behaviour of this circuit in the frequency band. This first cut exhibits a shift toward low frequencies of about 10%. This is identified, due to the RF filter, and will be corrected on the second pass under fabrication.

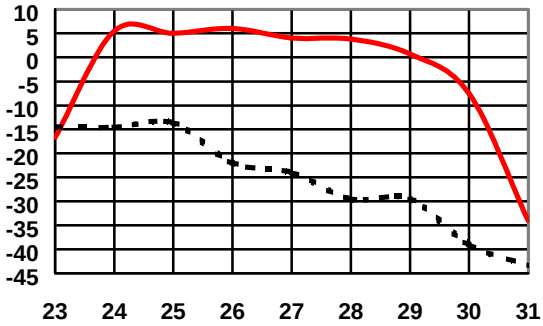

Fig. 7 : Up-Converter conversion gain
and LO leakage in dBc @ 1GHz IF.

III. CONCLUSION

We have demonstrated the development of a chipset including two complex 28GHz multifunction circuits, providing a full MMIC solution for the fabrication of a transceiver module of a LMDS subscriber terminal. A second design is completed and under fabrication in order to improve the gain bandwidth and the image suppression.

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REFERENCES