Fault isolation in distributed generation connected distribution networks

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Abstract- Protection of a distribution network in the presence of distributed generators (DGs) using overcurrent relays is a challenging task due to the changes in fault current levels and reverse power flow. Specifically, in the presence of current limited converter interfaced DGs, overcurrent relays may fail to isolate the faulted section either in grid connected or islanded mode of operation. In this paper, a new inverse type relay is presented to protect a distribution network, which may have several DG connections. The new relay characteristic is designed based on the measured admittance of the protected line. The relay is capable of detecting faults under changing fault current levels. The relay performance is evaluated using PSCAD simulation and laboratory experiments.

1. Introduction

Most existing electrical distribution networks are radial where currents flow from substation to customers in a unidirectional manner [1-3]. Overcurrent (OC) protection is usually used to protect radial networks from faults [4]. However, the connections of DGs in a feeder can cause bidirectional power flow, which can adversely affect protection coordination [2, 5]. Moreover, the fault current levels in the network will also change aggravating the situation further [6]. According to the IEEE standard 1547 [7], DGs should be disconnected from the network when a fault occurs. However such a strategy will reduce the system reliability significantly, especially when the penetration level of DGs increases. Therefore new protection methods are

required for DG connected distribution networks to improve supply reliability [5].

In a traditional radial network, the relay immediately upstream of the fault point trips the connecting circuit breaker causing a power outage to all customers downstream from the fault. The system reliability can be increased using the DG sources, if the faulted section is isolated and downstream unfaulted sections are allowed to operate in an electrical island [3]. This will prevent unnecessary customer power interruptions. Therefore, the benefits of DG installations can be maximized by allowing the DGs to operate in both grid-connected and islanded modes. To achieve this goal, the smallest possible faulted section should be isolated from both the upstream and downstream side of a network. The relay placed immediately upstream of a fault senses the sum of the utility current and the current supplied by any DG connected upstream. On the other hand, the relay located immediately downstream from the fault point will sense the fault current supplied by all the DGs connected further downstream.

Some of the DGs connected to the network are either intermittent in nature (e.g., solar photovoltaic based DGs) or not connected all the time (e.g., peak load gas generators). Therefore different fault current levels can be seen in the network depending on the number of DG connections [8]. As a result, the fault current level can be different at different times and this will considerably complicate the existing OC relay coordination. Furthermore, all the power electronic converter based DGs are equipped with internal fault current limiters to protect the switches from high currents [9, 10]. As a result, the converters may not be able to supply sufficient fault current to correctly trigger the OC relays which are located downstream of a fault [9].

In this paper, a novel inverse time admittance (ITA) relay is presented. The ITA relay utilizes the measured admittance of the protected line to identify a faulted condition in a network. It will be shown later that these relays are insensitive to fault current level. Therefore

these relays can overcome the deficiencies of OC relays. The proposed relay performance is validated by PSCAD/EMTDC simulations, MATLAB calculations and laboratory tests.

2. Comparison of OC relay with ITA relay

Several protection schemes have been proposed by researchers for DG connected distribution networks. However, most of them need a reliable communication medium. In [2] and [3], protection algorithms are proposed to locate a fault and isolate the faulty zone from the network. In [2], protection of the distribution network is achieved using neural network. In this, the system has different zones and the relay at the substation communicates with the zone breakers to take appropriate actions. A current protection scheme based on communication to a multi-source distribution system has been proposed in [5]. Wide area measurement is used to decide the appropriate protection actions to locate the fault through the use of a communication channel. A method proposed in [6] is based on analyzing the sign of wavelet coefficients of the fault current transient to locate and isolate a faulted segment. In this, relay agents are proposed to implement the proposed protection scheme. A multi agent approach based on communication is proposed in [11] to facilitate coordination between different protective devices in the presence of DGs. However, the ITA relay presented in this paper is capable of operating without any communication amongst relays under changed fault current levels in a network. The comparison between OC relay and ITA relay is given below.

Consider the line segment in a radial distribution feeder as shown in Fig. 1. The node *R* represents the relay location, while an arbitrary fault point at distance *X* from the relay is denoted by node *F*. The current and voltage seen by the relay for the fault is given by I_x and V_x respectively. The IEEE standard inverse time OC relay tripping characteristic is given by [12]

$$t_p = \left[\frac{A}{M_I{}^p - 1} + B \right] \times TDS \qquad (1)$$

where the constants A, B and p are used to select the relay characteristic curve, M_I is the ratio between the fault current seen by the relay and the relay pickup current and the tripping time is denoted by t_p.. The time dial setting (TDS) is used for the coordination of the OC relays. Let the relay pickup current be denoted by I_p. Then M_I in (1) is given by,

$$M_I = \frac{I_x}{I_p} \tag{2}$$

For a particular OC relay in the network, all the constants (A, B, p and TDS) are pre-selected and only M_I changes depending on the fault current level. Therefore M_I will solely decide the OC relay tripping time. If the fault current I_x changes in the presence of DGs due to their intermittent nature, different relay tripping times can be experienced. Also, if these relays are used to isolate the faults from downstream side of a converter connected radial feeder, the fault may not be detected due to lower fault current levels. Therefore, the settings of OC relays will be difficult due the intermittent nature of DGs. Let us assume that an OC relay is set to detect an upstream fault by lowering its pickup current. Nuisance tripping can then occur if the loads downstream from the relay are at their minimum, while the DG generation is at maximum.

To overcome the issue associated with faulted section isolation using conventional OC relays, either the relay settings should be changed continuously or a relay which is not dependent on fault current level should be used, depending on the DG connections. In this regards, the ITA relay, whose features are explained below, has a superior performance.

Instead of multiple of pickup current M_I, another quantity, called normalized admittance, which is not dependent on the network fault current level, is introduced. The ITA relay characteristic is given by,

$$t_p = \frac{A}{Y_r^{\rho} - 1} + k \tag{3}$$

where A, ρ and k are constants and Y_r is the normalized admittance, which is defined as

$$Y_r = \left| \frac{Y_m}{Y_t} \right| \qquad (4)$$

where Y_t is the total admittance of the protected line segment and Y_m is the measured admittance between the points R and F (see Fig. 1). The voltage at the relay point, corresponding to the pickup current I_p, is defined as V_p. To obtain the same sensitivity for the ITA relay as that of an OC relay, the total line admittance should be set to the admittance given by I_p and V_p. The normalized admittance can be expressed for the feeder shown in Fig. 1 as

$$Y_r = \frac{Y_m}{Y_t} = \frac{(I_x / V_x)}{(I_p / V_p)} = \frac{(I_x / I_p)}{(V_x / V_p)} \qquad (5)$$

From (2) and (5) we get

$$Y_r = \frac{M_I}{M_V}, \quad where \;\; M_V = \frac{V_x}{V_p} \qquad (6)$$

M_V can be defined as the multiple of pickup voltage. Note that $M_V < 1$ when a fault occurs in the system. It can be seen from (6) that the ITA relay uses both current and voltage multiples instead of only current based multiple used in OC relays. As a result, an ITA relay detects faults effectively irrespective of the available fault current in the network.

The constants in the ITA relay characteristic can be chosen according to the required fault clearing time and coordination requirements. However, the normalized admittance should be greater than 1.0 for relay tripping. This implies that the measured admittance is greater than the total admittance during a fault, i.e.,

$$Y_r > 1 \Rightarrow \left| \frac{Y_m}{Y_t} \right| > 1 \Rightarrow |Y_m| > |Y_t| \qquad (7)$$

The relay reach can be set by choosing a suitable value for Y_t. For a particular relay, different values of Y_t can be assigned to generate a number of required zones. The ITA relay has different types of protection elements such as earth elements and phase elements to detect

different types of faults. All elements are designed to operate based on the measured admittance of the protected line. Any upstream relay always provides the backup protection for the immediate downstream relay. A detailed description of ITA relay fundamentals, relay grading and relay reach settings is given in [13].

The ITA relays use directional elements to differentiate between upstream and downstream faults. The fault direction can be determined using relative phase angle between fault current and pre-fault voltage [14]. Also the negative sequence impedance [15] or the positive sequence directional element proposed in [16] can be also used to identify the fault direction.

3. Comparison of impedance type relay with ITA relay

To show how the ITA relay can be related to a conventional impedance type relay, real imaginary (R-X) plane representation is considered with the relay tripping curve. Only Zone-1 of the ITA relay is considered for this illustration. The ITA relay characteristic can be represented in both distance-tripping time and R-X plane as shown in Fig. 2. The tripping time characteristic curve of ITA relay can be mapped into circles in R-X plane, in which each circle has a unique tripping time. For example, consider the point *D* on tripping time curve. This point corresponds to a fault with tripping time t_4. When the point *D* is mapped into R-X plane, the point becomes a circle which gives the same tripping time of t_4. In a similar manner, four more circles are shown in R-X plane corresponding to fault points *A*, *B*, *C* and *E* on the tripping time curve of the relay. It can be concluded that an infinite number of concentric constant tripping time circles exist for Zone-1 of the ITA relay. Therefore, the ITA relay can be identified as similar to an impedance relay with an infinite number of zones to give different tripping times depending on the location of the fault point.

4. Simulation results

An ITA relay can isolate a faulted section under low fault current levels. It can also respond under changing fault current levels, thereby allowing DGs to supply power to unfaulted sections either in grid-connected or islanded mode of operation. Simulation studies are conducted to evaluate the ITA relay performance and to compare the performance of the ITA relay with the OC relay.

A. Change in source impedance

The behavior of OC and ITA relays is compared when the source impedance changes. A system, as shown in Fig. 3(a), is considered in which two parallel transformers are connected between buses A and B. The supply feeder starts at BUS-B. The impedance of each transformer is taken to be 0.3 p.u., while feeder impedance is chosen as 0.1 p.u. The relay response is shown in Fig. 3(b) for faults between BUS-B and BUS-C when only one transformer is connected as well as when both transformers are connected. Since an OC relay response depends on the fault current levels, there are two different curves for this relay. However, the ITA relay shows the same response irrespective of the impedance change caused by transformer connections.

B. Fault isolation in a radial feeder containing converter interface DGs

The faulted section isolation using ITA relays is investigated for different fault current levels. Consider the radial feeder containing 3 DGs as shown in Fig. 4. The system parameters are given in Table 1. It is assumed that all the DGs are connected to the feeder through converters, where they limit their output currents to twice the rated current during a fault. The ITA relays R_1, R_2 and R_3 are located at BUS-1, BUS-2 and BUS-3 respectively. The relay reach settings and tripping characteristics for each zone are given in Table 2. The relay response is observed by creating single line to ground (SLG) faults at different locations along the feeder. Results are obtained through PSCAD simulation.

The ITA relay response is observed by changing the DG connectivity to the network since all the DGs may not be connected all the time. The fault clearing time of respective relay(s) for a SLG fault with fault resistance of 0.5 Ω is listed in Table 3. It can be seen that ITA relays are capable of isolating the faulted section in the feeder from both upstream and downstream side irrespective of the number of DGs connected. After successful fault isolation, DGs supply power to the unfaulted sections without disconnecting from the feeder. The converter control strategy used is not presented here. Furthermore the resynchronization of the islanded sections after fault removal is not discussed here. Note that the OC relays cannot be used in this application with the same reach setting since the fault current is low and can change.

C. Fault isolation in a mesh network

To demonstrate an application of the ITA relays in a mesh network, the system shown in Fig. 5 is considered. This has a partly mesh network containing BUS-1, BUS-2 and BUS-5. There are three converter connected DGs with different power ratings and three loads. Eight ITA relays are employed for secure and reliable operation of the system. The relay locations are shown in the figure. One of the main aims of the ITA relays is to isolate the faulted segment quickly in the event of a fault allowing unfaulted sections to operate either in grid connected or islanded mode depending on the fault location. The feeder impedances and relay settings are similar to those given in Table 1 and Table 2. In this study, to provide a simple and cost effective solution, no communication between relays is considered.

The relays, R_{12}, R_{21}, R_{15}, R_{51}, R_{52} and R_{25}, which are located in the mesh network, have the directional blocking feature in which these relays only respond to forward faults. This results in proper relay coordination within the mesh network. For example, consider relay R_{15}. It protects the line segment between BUS-1 and BUS-5. Also it provides the backup protection for the line segment between BUS-5 and BUS-2. However, R_{15} is blocked for the reverse faults since R_{12} should operate for the faults between BUS-1 and BUS-2. The relays R_{12} and

R_{52} cover the line segment between BUS-2 and BUS-3 in forward direction. On the other hand, the relay R_{32} has the directional feature and thus it can detect faults in either sides of BUS-3. The relay R_{43} is also a directional blocking relay which only responds for reverse faults since it is located at the end of the feeder.

The system is simulated in PSCAD. A SLG fault is created at the middle of each line segment with a fault resistance of 0.5 Ω at 0.2 s. The ITA relay fault clearing times are listed in Table 4. As can be seen from the results, the relays respond to isolate the faulted segment effectively. For example, in the event of a fault between BUS-1 and BUS-2, the both relays R_{12} and R_{21} respond to isolate the faulted segment. In this case, the rest of the system operates in grid connected mode after the successful isolation of the faulted segment.

5. Experimental implementation of ITA relay

The ITA relay performance is examined in a single-phase test feeder. A schematic diagram of the experimental setup is shown in Fig. 6. The source voltage can be controlled according to the requirement. Five buses are defined in the feeder. However, only one ITA relay is located at BUS-1 and it provides the protection for the whole test feeder. A National Instruments (NI) PXI-1042Q chassis is used to implement the ITA relay algorithm. The NI chassis has a PXI-8187 windows XP Embedded card, two analog input cards and an output relay card. The voltage and current signals at the relay location are acquired via the analog cards. A line to ground fault is created using one of the switches in the output relay card. This switch can be fully controlled by the LabVIEW software. A typical fault location is shown in Fig. 6. The fault location however has been changed to study the relay performance. The fault is created at a random time by closing the switch of the output relay card, while the ITA relay sends fault clearing signal to the same switch. It is to be noted that CB1 provides back up protection in case the switch does not operate to clear a fault. The system parameters of the test system are given in Table 5.

The ITA relay algorithm is modeled in LabVIEW. A Fast Fourier Transform (FFT) is used to extract the fundamental component of sampled voltage and current signals. The measured admittance is then calculated using the extracted fundamental components. The relay reach setting is manually entered according to the line parameters. The relay algorithm issues the fault detection signal and it calculates the tripping time when a fault occurs based on the measured admittance. The same relay tripping characteristic as given in Table 2 is used in the experiments. A digital oscilloscope is used to capture the faulted phase voltage at relay location and the fault current. A number of tests are carried out under different test feeder configurations to evaluate the relay performance.

A. ITA relay response for different fault locations

The ITA relay response for faults is investigated by changing the fault location and the source impedance to demonstrate the robustness of the relay operation. The relay should give higher tripping time when the fault point moves away from the relay location due to the inverse time characteristic. Also, the relay should respond in the same manner irrespective of source impedance. To observe these features, several tests are carried out. However few of the test results are given in Table 6.

According to the results given in Table 6, the relay response time is close to the calculated theoretical values. However, the actual fault clearing time is slightly higher than the relay response time values due to the fault clearing time taken by the hardware switch. Once the relay issues the trip command, the hardware switch may take up to 10 ms to open [17].

The captured voltage and current signals at relay location for the faults at BUS-2 are shown in Fig. 7. The source current lags the voltage before the fault. The current increases rapidly after the initiation of the fault while the voltage reduces. During the fault, the normalized admittance becomes higher than 1.0 and it causes the relay to initiate the trip signal. The tripping time is decided based on the value of the normalized admittance. In Fig.

7(a) and Fig. 7(b), the points on the current cycle at which the faults occur are different. However, the relay response time is the same for tests 1 and 2 (see Table 6). It is to be noted that several tests are carried out by increasing the source impedance, all resulting in similar test results since the ITA relay response does not change with the source impedance.

6. Analysis of ITA relay degradation factors

The calculated value of the normalized admittance for a particular zone will depend on the measured admittance since the total admittance setting for that zone is constant. Therefore, the calculated relay tripping time can deviate from the expected value if the measured admittance is not accurate. Thus, the factors which can affect the measured admittance should be considered and they should be minimized to improve the relay performance.

Typically, two types of errors, which can affect the measured admittance, are identified. The first type occurs due to the fault resistance and downstream sources (called here as infeed). The calculated measured admittance errors due to the fundamental extraction can be considered as the second type. Current transients, harmonics, and decaying dc component can cause errors in the fundamental extraction. Both the error types will be explained and investigated experimentally in following two sub-sections.

A. The effect of fault resistance and infeed

To explain the change of relay response in the presence of fault resistance, a fault between relays R_1 and R_2 is considered in the network shown in Fig. 8. The Thevenin equivalent line impedance between R_1 and fault point is denoted by Z_f, while that between R_2 and fault point is denoted by Z_r. The fault current fed from the source is denoted by I_S, while the fault current

fed from the downstream side DGs is denoted by I_{DG}. The measured admittances seen by relays R_1 and R_2 in the presence of fault resistance (R_f) and DGs can respectively be given by

$$Y_{m(R_1)} = \frac{I_S}{Z_f I_S + R_f (I_S + I_{DG})} = \frac{1}{Z_f + R_f \left[1 + \frac{I_{DG}}{I_S}\right]} \quad (8)$$

$$Y_{m(R_2)} = \frac{I_{DG}}{Z_r I_{DG} + R_f (I_s + I_{DG})} = \frac{1}{Z_r + R_f \left[1 + \frac{I_s}{I_{DG}}\right]} \quad (9)$$

As per (8) and (9), an error occurs in the measured admittances due to the fault resistance. If fault resistance is zero, the error becomes zero. When fault resistance is present, the ratio between source current and DG current (I_S/I_{DG}) also affect the error on measured admittance. For fault detection, the measured admittance (Y_m) should be greater than the total admittance (Y_t). Generally, $I_S > I_{DG}$ since I_S is fed by a utility with higher capacity than the DGs. Therefore, for a particular DG penetration level and a particular value of fault resistance, the error on the measured admittance R_2 ($Y_{m(R2)}$) is greater than that of R_1 ($Y_{m(R1)}$). Thus it can be seen that fault resistance will affect the downstream relay more than the upstream relay. However, once the upstream relay isolates the fault, source current I_S becomes zero. This results in reducing the error due to source current as can be seen from (9). However, the error due to R_f will still remain. The maximum value of fault resistance for which the relay reliably detects the faults can be calculated based on the relay reach settings and the DG capacity.

The same experimental setup as shown in Fig. 6 is used to test the relay performance in the presence of fault resistance and infeed. The test feeder is modified by connecting another source at BUS-5 to represent a DG located downstream to the relay. The response of the upstream ITA relay is obtained for the faults at BUS-2, BUS-3 and BUS-4 with a fault resistance of 1.89 p.u. (with the base of 230V and 10kVA). The calculated and the experimental relay parameters during the faults are given in Table 7. It can be seen that experimental results are close to the calculated results. Thus the ITA relay is capable of

isolating the fault. However, the tripping time has increased due to the fault resistance and infeed. The variation of normalized admittance during the fault at BUS-2 is shown in Fig. 9. The normalized admittance increases beyond the value 1, causing the relay to trip after 138 ms.

B. The effect of fundamental extraction

Harmonics, current transients and decaying dc magnitude and time constant can be identified as the major challenges on fundamental extraction. The decaying dc component can usually appear in the current signal. However, the decaying dc magnitude and time constant cannot be calculated before a fault occurs since it depends on the system configuration (X/R ratio), fault location and the value of fault resistance. A 415 V, three phase synchronous generator connected test feeder shown in Fig. 10 is considered for the analysis. A SLG fault is created at the end of line segment as shown in the figure. Several tests were conducted to investigate the ITA relay behavior during the fault. However, only one result is presented here.

The faulted voltage and current captured during a SLG fault is shown in Fig. 11(a). It can be seen that the current waveform has a decaying dc component during the transient period while the voltage has harmonics during the faulted period. The values of extracted current and voltage using FFT during each cycle are shown in Fig. 11(b). The extracted rms current is higher than the steady state fault current during the first three cycles. The extracted rms voltage also takes few cycles to reach steady state. Also note that depending on the instant at which a fault occurs, the first cycle of the rms calculation may contain a part of unfaulted voltage/current samples. Therefore it is always expected that the first cycle will have transient data.

The measured admittance and the tripping time calculated in each cycle are also shown in Fig. 11(b). It can be seen that the tripping time reduces slightly with the change of measured admittance. However, in these tests, the fault duration is intentionally maintained for a defined

time period to observe the relay parameters for a few cycles. The results show that the FFT can be used in ITA relay to extract fundamental in the presence of harmonics and signal noises as expected. However, the FFT is not immune to the decaying dc component. Therefore, the calculated tripping time of the relay can vary slightly.

To improve the accuracy of the relay tripping time, an accurate method can be used to calculate the fundamental component in the presence of decaying dc component. In [18], a method is proposed to eliminate the effect of decaying dc component by calculating the time constant of the faulted current waveform. A discrete Fourier transform (DFT) based filter algorithm is presented in [19] for digital distance relays to extract the fundamental accurately. In [20], a method is described to remove the decaying dc component for an application of protective relays. Thus one of the above algorithms can be used in the ITA relay application to minimise the error in tripping time calculation. However, the speed of the calculation and burden on the processor should be carefully considered when selecting a particular algorithm.

7. Conclusions

An inverse time admittance (ITA) relay is presented in this paper to isolate a faulted section in a DG connected radial distribution network. The limitations of the existing overcurrent relays for detecting faults under lower fault current levels and changing fault current levels in the presence of converter connected DGs can be avoided using the proposed ITA relay. To illustrate the effectiveness of the ITA relay, the relay performance is evaluated in a radial and a mesh distribution network containing DGs. Furthermore, the experimental validation is carried out in a laboratory test feeder and the limitations of proposed ITA relay are discussed. The results reveal that proposed relay can be reliably used in a distribution network with DGs to isolate the faulted section, thereby maximizing the DG benefits.

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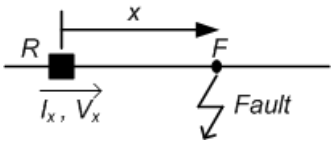


Fig. 1 Faulted line with a relay

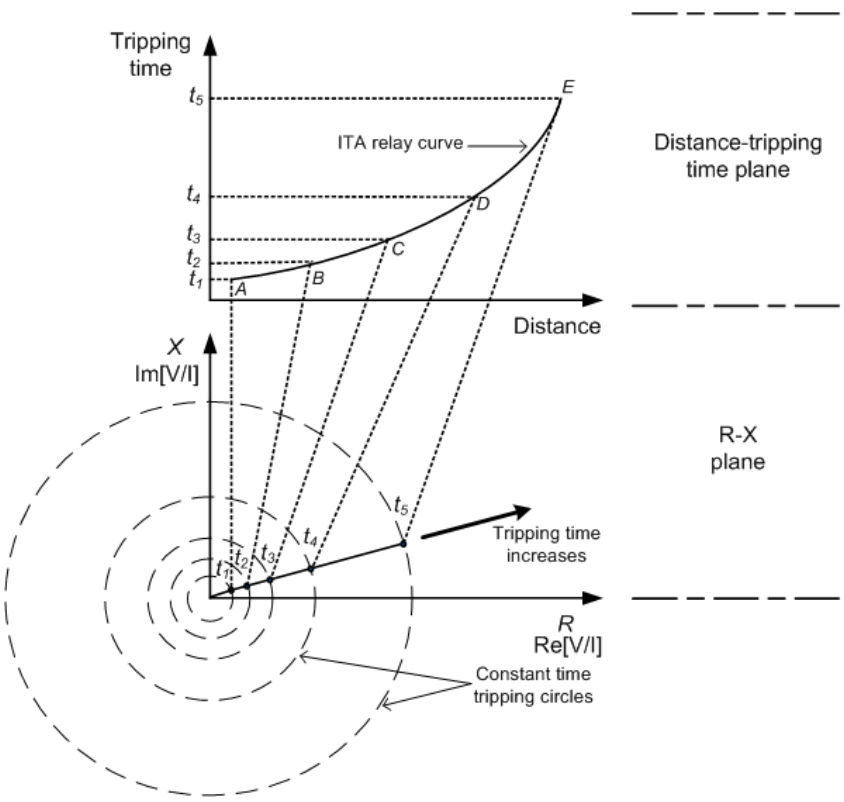
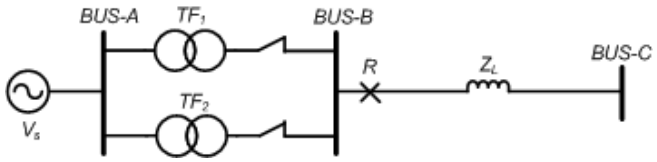
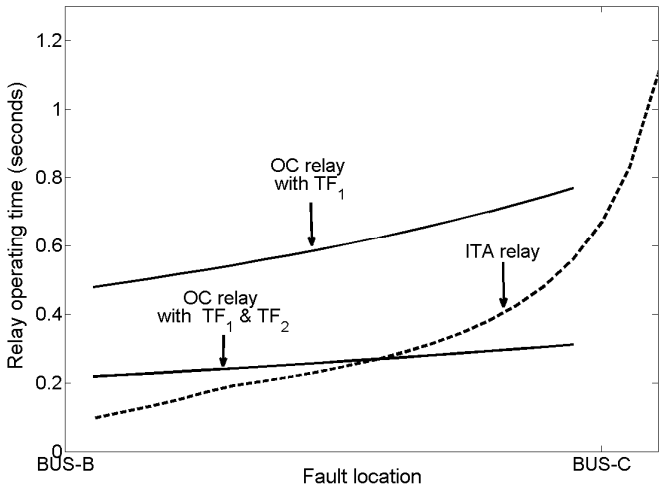


Fig. 2 ITA relay characteristic in R-X diagram



(a) System with two parallel transformers



(b) Relay response for impedance change

Fig. 3 OC and ITA relay response for different system configurations

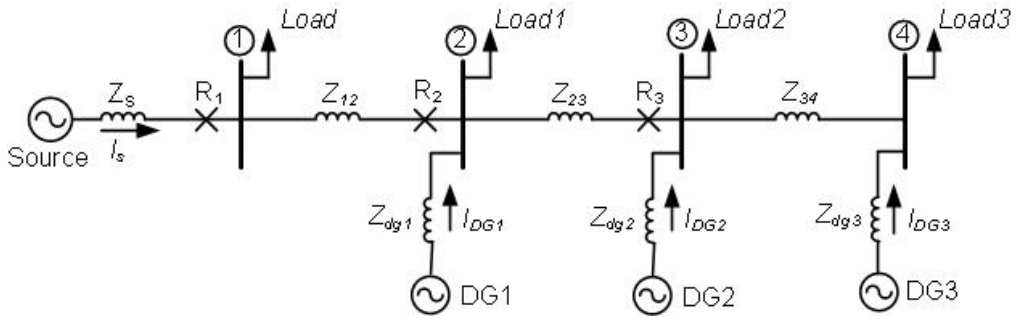


Fig 4. DG connected radial distribution feeder

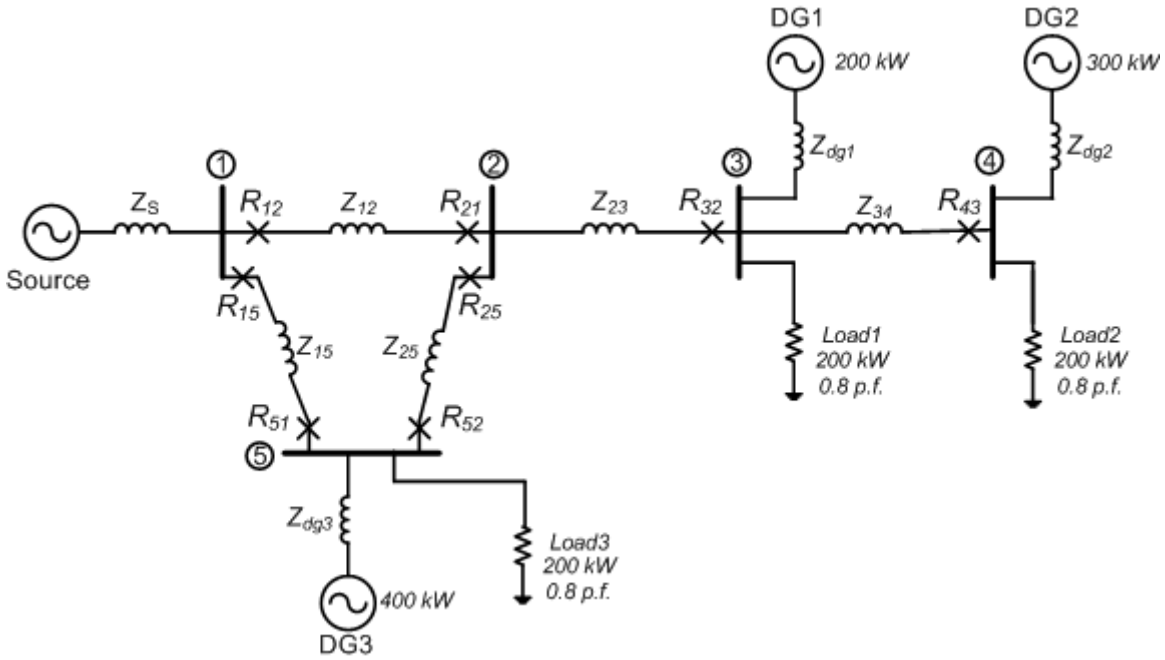


Fig. 5 Mesh network under study

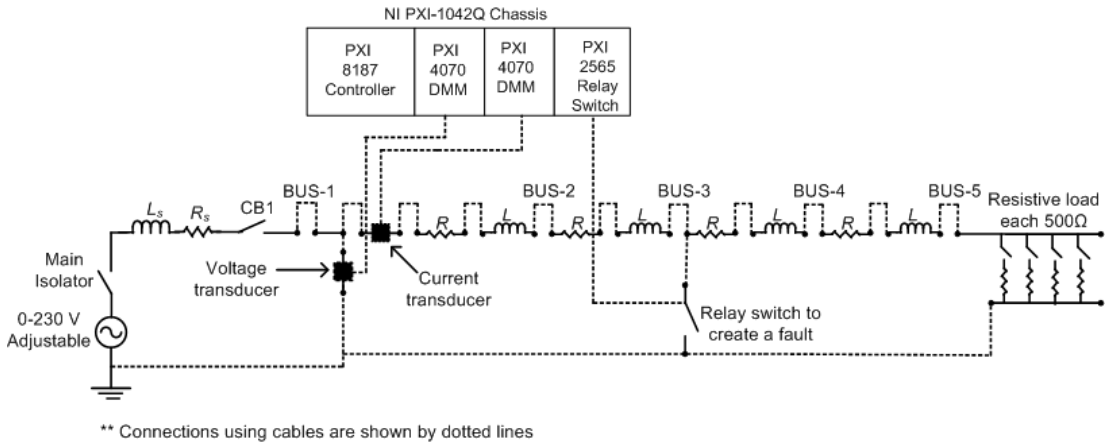
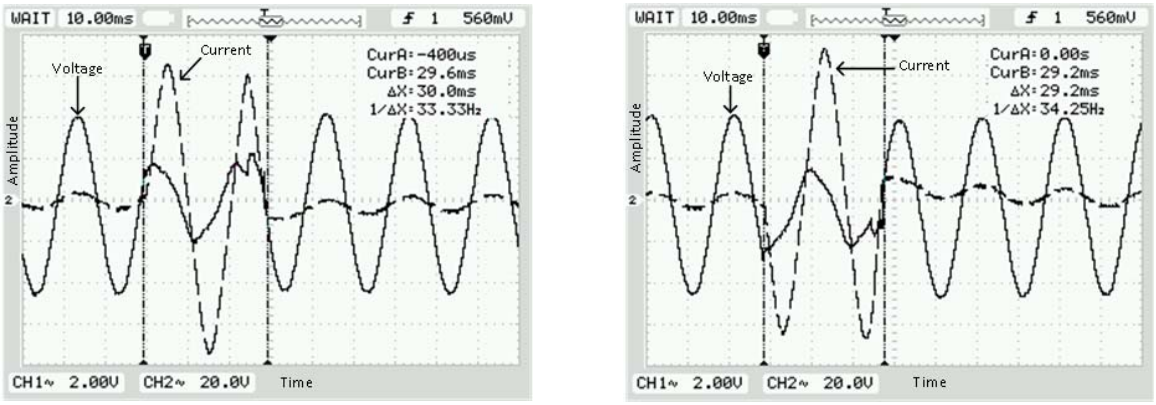


Fig. 6 Single line diagram of experimental setup



(a) Test-1 (b) Test-2

Fig. 7 The variation of voltage and current for SLG faults at BUS-2

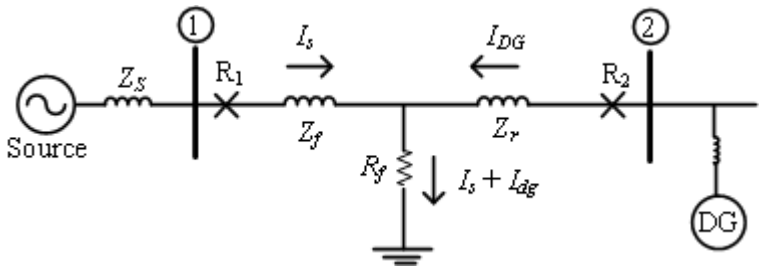


Fig. 8 Equivalent representation of the faulted network with DGs

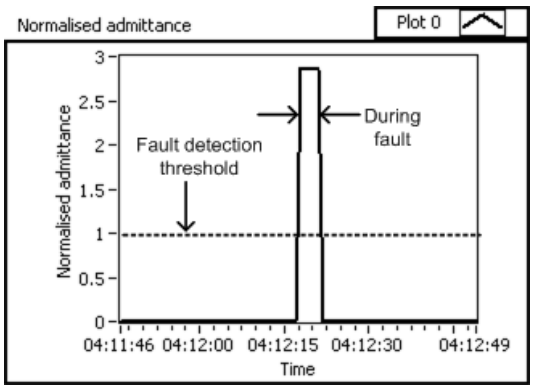


Fig. 9 Change of parameters during a fault at BUS-2 with fault resistance and infeed

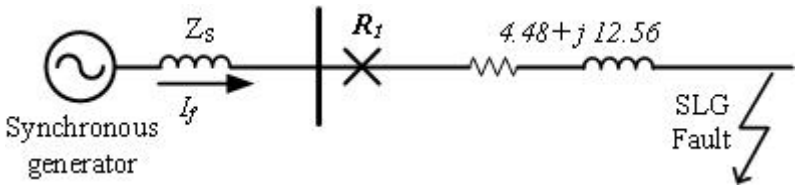
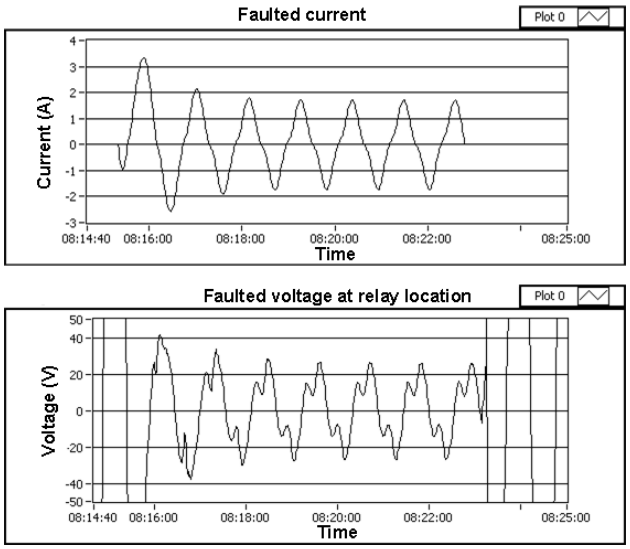
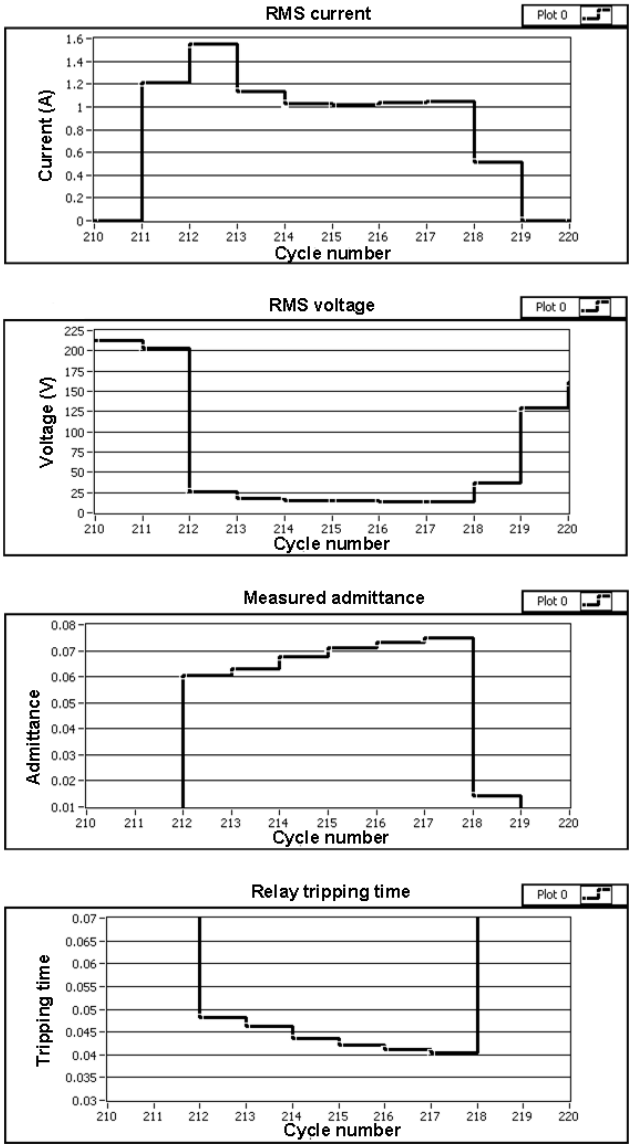


Fig. 10 A SLG fault at synchronous generator connected feeder



(a) Faulted current and voltage



(b) Values of calculated relay parameters during a SLG fault

Fig. 11 The faulted waveforms and ITA relay parameters during a fault

Table 1: System parameters

System data	Value
System frequency	50 Hz
Source voltage	11 kV rms (L-L)
Source impedance (Z_s)	$0.078 + j\,0.8634\ \Omega$
Source impedance (Z_{dg})	$0.39 + j\,3.927\ \Omega$
Feeder impedance (Z_{12}=Z_{23} =Z_{34})	$0.585 + j\,2.9217$
Each load power	0.5 MVA, 0.8 p.f.
Each DG power output	0.5 MVA

Table 2: Relay reach setting and tripping characteristic for each zone

Relay zone	Tripping characteristic and reach
Zone-1	$Y_{t1} = \dfrac{1}{1.2 \times (0.585 + j\,2.9217)}$

	$t = \frac{0.0037}{Y_r^{0.2} - 1} + 0.02$
Zone-2	$Y_{t1} = \frac{1}{2 \times (0.585 + j\,2.9217)}$
	$t = \frac{0.003}{Y_r^{0.04} - 1} + 0.02$
Zone-3	$Y_{t1} = \frac{1}{3 \times (0.585 + j\,2.9217)}$
	$t = \frac{0.0025}{Y_r^{0.02} - 1} + 0.02$

Table 3: ITA relay response for different system configuration

Fault location (middle of two buses)	DG connectivity		
	All DGs	DG1 and DG2	DG3 only
BUS-1 and BUS-2	R_1=0.038 s R_2=0.041 s	R_1=0.038 s R_2=0.041 s	R_1=0.042 s R_2=0.048 s
BUS-2 and BUS-3	R_2=0.039 s R_3=0.044 s	R_2=0.044 s R_3=0.045 s	R_2=0.044 s R_3=0.045 s
BUS-3 and BUS-4	R_3=0.044 s	R_3=0.044 s	R_3=0.044 s

Table 4: Fault clearing time of ITA relays

Fault location	Fault clearing time (s)
BUS-1 and BUS-2	R_{12}=0.046, R_{21}=0.062
BUS-1 and BUS-5	R_{15}=0.046, R_{51}=0.063
BUS-2 and BUS-5	R_{25}=0.050, R_{52}=0.050
BUS-2 and BUS-3	R_{21}=0.060, R_{25}=0.077, R_{32}=0.102
BUS-3 and BUS-4	R_{32}=0.047, R_{43}=0.098

Table 5: System parameters of the experimental setup

System parameter	**Value**
Source	0 - 230 V rms (L-G), 50Hz
Feeder impedance	R = 1.12 Ω
	L = 0.01H (j 3.15 Ω)
Load impedance (Z_L)	125 Ω
CB1 rated current	1 A
Hardware specifications	
NI chassis	PXI-1042Q
NI controller	PXI-8187 windows XP
Transducers	
Voltage	Differential amplifier
Current	LEM LTSR 6-NP
Data acquisition	
Analog inputs	PXI-4070 FlexDMM
Digital outputs	PXI-2565 relay switches

Sampling rate	3200 samples per seconds

Table 6: ITA relay response for line to ground faults at different fault locations

Fault location	Test number	Theoretical tripping time (ms)	Relay response time (ms)	Actual fault clearing time (ms)
BUS-2	Test-1	30	29	29.2
	Test-2	30	29	30.0
BUS-3	Test-1	40	38	39.2
	Test-2	40	37	38
BUS-4	Test-1	58	57	62.4
	Test-2	58	58	64
BUS-5	Test-1	120	119	122
	Test-2	120	118	121

Table 7: Change of relay parameters due to fault resistance and infeed

Fault location	Calculated results			Experimental results		
	Y_m	Y_r	t_p (ms)	Y_m	Y_r	t_p (ms)
BUS-2	0.0709	2.8442	138	0.07	2.8	138
BUS-3	0.0500	2.0071	198	0.049	1.97	201
BUS-4	0.0354	1.4218	374	0.035	1.41	380