Power Network in Loop: A Paradigm for Real-Time Simulation and Hardware Testing

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***Abstract*—This paper discusses a new paradigm of real-time simulation of power systems in which equipment can be interfaced with a real-time digital simulator. In this scheme, one part of a power system can be simulated by using a real-time simulator, while the other part is implemented as a physical system. The only interface of the physical system with the computer-based simulator is through data-acquisition system. The physical system is driven by a voltage-source converter (VSC) that mimics the power system simulated in the real-time simulator. In this paper, the VSC operates in a voltage-control mode to track the point of common coupling voltage signal supplied by the digital simulator. This type of splitting a network in two parts and running a real-time simulation with a physical system in parallel is called a power network in loop here. This opens up the possibility of the study of interconnection of one or several distributed generators to a complex power network. The proposed implementation is verified through simulation studies using PSCAD/EMTDC and through hardware implementation on a TMS320F2812 DSP.**

***Index Terms*—Control bandwidth, power network in loop simulation, real-time simulator, voltage-source converter (VSC).**

I. Introduction

DIGITAL computer simulations have been used extensively in power systems studies for both design and testing. However, this form of evaluation tool is often not suitable for testing of protective devices like relays or testing real life controllers. To alleviate this problem, real-time digital simulators have been developed, which use high speed parallel processors to simulate a complex power network within microseconds [1]–[3]. These simulators can be interfaced with a physical controller online and this form of operation is often termed as "hardware-in-the-loop" testing.

While testing protection devices, the real-life system components interact with a digital simulation of a power network running in real time. The hardware is sent signals to represent the currents or voltages in a network with small amplifiers to make the signals compatible with the output expected from VTs and CTs. The trip signal from the protecting device is then passed to the simulator which can then open/close circuit breakers in the simulated network. The advantage of the approach is that limitations of the hardware implementation can be evaluated within a realistic environment.

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The aim of this paper is to broaden the "hardware in the loop" concept to include testing of network components. For many consumer devices, the mains supply can be treated as an ideal voltage source, and hence, the component testing only requires finding a near-ideal source for evaluating performance. This paper aims to develop the theory for online interaction between power network components and simulation using an inverter interface. For the simulation of large systems, Kron's method of tearing the network into two or more segments offers possibilities [4], [5]. The difficulty is that the theory is developed with similar network solution processes in both sections without the interface issues.

The interface of real-time controller with a simulated circuit is reported in [6]. Controller output is sent to real time virtual test bed (RTVTB) through an analog-to-digital card and simulation output is sent to micro-controller. Here the communication is at low voltage. No amplification is required. Communication is carried out through a serial port.

The network tearing aspect has been studied in a two part paper [7], [8]. In Part 1 [7], different methods of tearing are presented and compared against their performance. This paper discusses power hardware in loop (PHIL) concept through a two way interactions. But however does not discuss the hardware feasibility. The frequency response of different simulation/hardware interface schemes has been presented in [8]. It however does not present the stability analysis aspects of tearing.

We begin our discussion with an introduction to the hardware-software simulation concept. This will be followed a discussion of closed-loop VSC control employed in the paper for voltage control. The associated filtering issues will also be discussed. The proposed structure will be verified through extensive PSCAD simulation and also through an experimental setup prepared around a TMS320F2812 DSP processor.

II. The Hardware-Software Concept

The conceptual diagram of the hardware-software simulation system is shown in Fig. 1. In this diagram, the power network, simulated in a real-time simulator, is termed as the supply side, while the equipment to be tested is termed as the test side. In general the test side is assumed to contain a separate generator, which often can be a disturbed generator (DG). The supply side is represented by its Thevenin equivalent v_1, Z_1. The test side may contain a DG, feeder and any local load, which have a Thevenin equivalent of v_2, Z_2. In this figure, the voltage v_f of the test side is generated by a voltage-source converter (VSC).

In Fig. 1, the voltage v_p measurement is tracked by the VSC to produce v_f of the test side. The current-controlled current source i_f is controlled by the output of the low-pass

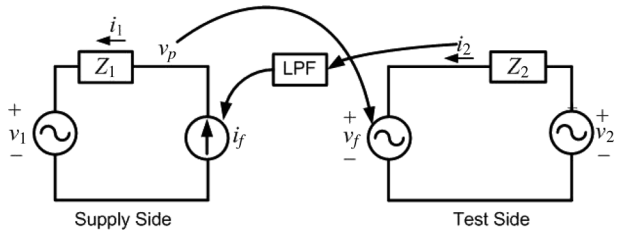


Fig. 1. Conceptual hardware–software simulation diagram: Voltage control.

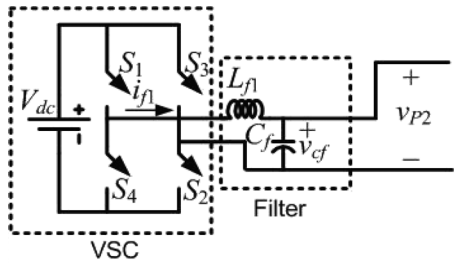


Fig. 2. Power amplifier structure.

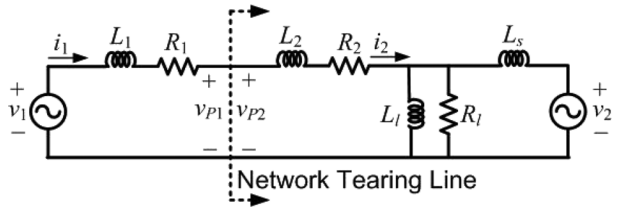


Fig. 3. Simple network under study.

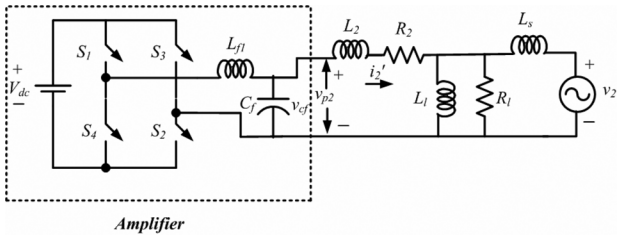


Fig. 4. Voltage controlled VSC amplifier connection with the test side.

filter (LPF). The function of the LPF is to suppress the high frequency switching components generated by the VSC of the test side current. Moreover, it also has an impact on the stability of the system, as we shall discuss later. The voltage and current are transferred from one part (supply side) of the network to the other part (test side) of the network in the form of low voltage signals with the help of voltage and current sensors. A current sensor measures the current i_2, which is then sampled and converted by an analog-to-digital converter (ADC). This signal can then be scaled to be of the same magnitude as that in the simulated circuit. The LPF is realized in the form of an averaging process in software itself. The voltage feedback from supply side to test side is amplified by the VSC, which acts as a power amplifier. The design of this amplifier is described in Section III. It is to be noted that the connection between the supply side and the test side is only through signal level through digital-to-analog converter (DAC) and ADC. Power level signals are not exchanged.

Depending on the network complexity and parallel processing hardware availability, a real-time simulator can solve the supply side dynamic equations in as little as 2 microseconds. A VSC, however, cannot be operated at this speed. Therefore a much lower switching frequency of the VSC can be chosen, provided that it is sufficient to track the desired voltage.

In Fig. 1, the VSC mimics the supply side for the test side and it is supposed to generate same voltage waveform as v_p. But when VSC tracks supply side voltage for test side, it generates high frequency switching components along with desired voltage. These high frequency components reflect in current (i_2) flowing at test side. Since these high frequency switching components are not part of network therefore elimination of these components are necessary. If this current (i_2), containing high frequency components, is fed to supply side directly, total deterioration of the system performance will occur. Hence low pass filter is used to eliminate undesired high frequency components. The effect of the LPF on the system stability is discussed in the Appendix.

The location of the tearing point will influence the stability of the simulation. However, in general, the tearing point cannot be freely chosen since it will depend on the total system being simulated as well as the hardware test components. In this paper, a common case of tearing at the middle of feeder is demonstrated.

III. Amplifier Structure

Fig. 2 shows the structure of VSC-based power amplifier. It contains one H-Bridge voltage-source converter and an LC filter with inductance of L_{f1} and capacitance of C_f at the output of converter. This filter prevents the high frequency switching components from entering the test side. VSC is connected to DC storage $V_{\rm dc}$. Output voltage v_{cf} is controlled using a voltage control scheme. Voltage signals of v_p from supply side is considered as a reference for the voltage control scheme.

To discuss the VSC control strategy used in the paper, let us consider a simple power system, as shown in Fig. 3. The network tearing line is also shown in this figure. In this, the supply side contains the voltage source v_1, while source impedance is being represented by $R_1 + j\omega L_1$. The test side voltage source v_2 has a source impedance $j\omega L_s$. It also contains a passive R-L load (R_l, L_l) and a feeder with an impedance of $R_2 + j\omega L_2$. The test side equivalent circuit is shown in Fig. 4.

Ideally, v_{p1} should be equal to v_{p2} and i_1 should be equal to i_2. However with the network being torn, this will not be so. The main idea of the VSC control is force them to be nearly equal. The success of the scheme will depend on the closed-loop control of the VSC, which enables it to track the reference voltage accurately. Closed-loop voltage tracking in the presence of a filter, however, is a nontrivial task. In this paper, a strategy of close loop voltage control is discussed.

IV. Hybrid Discontinuous Voltage Control

In this control scheme, the converter switching decision is made based on inductor current (i_{f1}) and capacitor voltage (v_{cf}) of LC filter to control the output voltage of amplifier. All the three states ($+1$, -1 and 0) of inverter are used here. In $+1$ and -1 states, the output voltages of converter are $+V_{\rm dc}$ and $-V_{\rm dc}$ respectively and the 0-state is the diode state where all

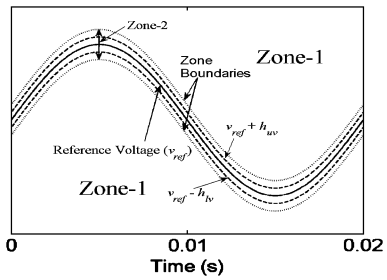


Fig. 5. Two zones voltage control scheme.

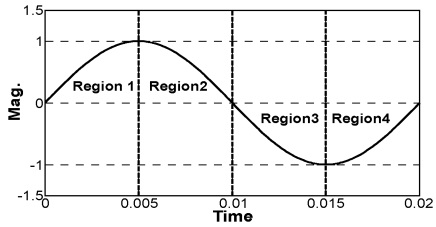


Fig. 6. Four regions of one cycle of a sinusoidal wave.

four switches are turned off. In the diode state, with the help of the free-wheeling diode, the inductor current is forced to zero. This state introduces discontinuity in the converter output current (i_{f1}).

Based on zones, control action between inductor current control and capacitor voltage control is switched as shown in Fig. 5. If error between reference voltage and capacitor voltage is high then control action is assumed in Zone-1 where converter decision is made based on filter inductor current and it is controlled inside a band. Once error reduces due to the control action of Zone-1, control action is switched to Zone-2, where converter switching decision is made based on filter capacitor voltage.

To track a sinusoidal capacitor voltage reference, one cycle is divided in four regions as shown in Fig. 6, where each region is divided into two zones explained above. For each zone, the hysteresis band is defined separately. In Zone-1, the hysteresis band is defined for the inductor current and in Zone-2, the band is defined for the capacitor voltage. In Regions 1 and 3, the capacitor is charged for positive and negative voltage respectively. Thus the switching control logic is very much similar in Regions 1 and 3. Only reference changes from positive to negative.

If the reference of the capacitor voltage is in Region 1, then switching in Zone-1 will be defined as

$$\text{If } i_{f1} \geq h_i \text{ then } S_{1-4} = 0 \tag{1}$$

where h_i is the upper current hysteresis band. This implies that if the current i_{f1} is greater than or equal to h_i, turn all the switches off. However, if this current is less than zero, which is lower current band limit, apply positive voltage at the VSC output, i.e.,

$$\text{If } i_{f1} < 0 \text{ then } S_{1,2} = +1 \text{ and } S_{3,4} = 0. \tag{2}$$

Let the upper and lower voltage hysteresis bands (for Zone-2) be denoted by h_{uv} and h_{lv}, respectively. Then, for Zone-2, we have the following switching logic:

$$\text{If } v_{cf} \leq v_{ref} - h_{lv} \text{ then } S_{1,2} = 1 \text{ and } S_{3,4} = 0 \tag{3}$$

$$\text{If } v_{cf} > v_{ref} - h_{lv} \text{ and } v_{cf} < v_{ref} + h_{uv} \text{ then } S_{1-4} = 0 \tag{4}$$

$$\text{If } v_{cf} \geq v_{ref} + h_{uv} \text{ then } S_{1,2} = 0 \text{ and } S_{3,4} = 1. \tag{5}$$

The switching for Region 3 will be the same as above except that $-V_{\rm dc}$ state will be chosen instead of $+V_{\rm dc}$ state.

The switching for Region 2 two is defined as follows. The switching in Zone-1 is

$$\text{If } i_f \geq 0 \text{ then } S_{3,4} = 1 \text{ and } S_{1,2} = 0 \tag{6}$$

$$\text{If } i_f \leq h_i \text{ then } S_{1-4} = 0. \tag{7}$$

Similarly for Zone-2, we have

$$\text{If } v_{cf} \geq v_{ref} + h_{uv} \text{ then } S_{3,4} = 1 \text{ and } S_{1,2} = 0 \tag{8}$$

$$\text{If } v_{cf} < v_{ref} + h_{uv} \text{ and } v_{cf} > v_{ref} - h_{lv} \text{ then } S_{1-4} = 0 \tag{9}$$

$$\text{If } v_{cf} \leq v_{ref} - h_{lv} \text{ then } S_{3,4} = 0 \text{ and } S_{1,2} = 1. \tag{10}$$

Switching for Region 4 can be obtain in the same way as in Region 2, the only difference being the capacitor discharges from negative to zero instead of positive to zero.

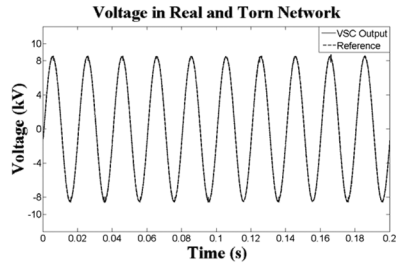
Example 1: To demonstrate the voltage tracking ability of the VSC, let us consider the system of Fig. 3. Here it is assumed that network is torn in two parts (supply and test) from network tearing line as shown in Fig. 3. The torn network is interfaced with the help of VSC amplifier as shown in Fig. 4. Efficiency of amplifier can be judged with the help of error between voltage (v_{p1}) at tearing point in actual network (Fig. 3) and voltage v_{p2} at test side in the torn network. Ideally these two voltages should be identical. The system parameters chosen for the study are

$$\text{System Frequency} = 50 \text{ Hz},$$
$$v_1 = 9\sin(\omega t)\text{kV},\ v_2 = 9\sin(\omega t - 30^\circ)\text{kV},$$
$$L_1 = 60 \text{ mH},\ L_s = 5 \text{ mH},\ R_1 = 0.94\ \Omega,.$$
$$\text{Feeder \& Load} : R_2 = 1.25\ \Omega,\ L_2 = 80 \text{ mH},\ R_l = 50\ \Omega,$$
$$L_l = 100 \text{ mH}.$$
$$\text{VSC \& Filter} : V_{\rm dc} = 15 \text{ kV},\ L_{f1} = 10\ \mu\text{H},\ C_f = 2500\ \mu\text{F}.$$
$$\text{LPF}(s) = \frac{20000}{s + 20000}.$$

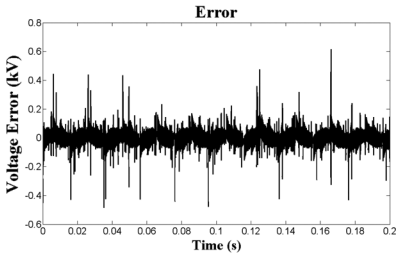
The system is simulated using PSCAD with a simulation step size of 10 μs. Voltage tracking results of hybrid discontinues voltage control is shown in Fig. 7(a) which shows reference voltage v_{p1} of the total (real) network (Fig. 3) and output voltage of amplifier (v_{p2}). Since the difference between two voltages is not visible from this figure, the error between them is plotted in Fig. 7(b). The average error is less than 0.55%.

Fig. 8(a) shows the reference current i_2 of the total (real) network (Fig. 3) and the current flowing in torn network (i_2'). The error between these two currents is plotted in Fig. 8(b). The steady state average and maximum errors in current are about 0.58% and 1.56%.

Inverter-based amplifiers have finite bandwidth and gain. Higher switching frequency can result high bandwidth and gain. However, the switching frequency is limited by the power rating of amplifier/switches. The proposed amplifier (control) is well capable to accommodate 13th harmonic in its bandwidth. Since most of the power system testing do not consider more than a few low order harmonics, this amplifier would be

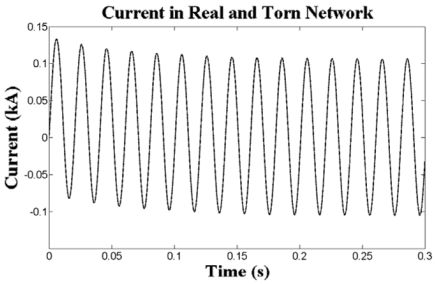


(a)

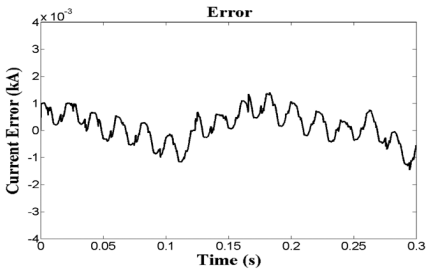


(b)

Fig. 7. (a) Voltages v_{p1} and v_{p2} and (b) voltage tracking error.



(a)



(b)

Fig. 8. (a) Currents i_1 and i_2 and (b) the error between these two currents.

adequate for those studies. Low pass filters can help to prevent high frequency oscillations caused by imperfect amplifiers or simulator step size. However the prevention of oscillation can impact on the bandwidth of the replication of the true connected circuit. In the examples shown in the paper, the low pass filter has cut-off frequency around 3.2 kHz, where the amplifier has a basic bandwidth 650 Hz. Thus the LPF does not a significant impact on the bandwidth of the total simulation compared with the bandwidth limitation of the amplifier.

V. Experimental Results

A hardware setup is built to test and verify the practical feasibility of the power network-in-loop concept. One H-Bridge single phase inverter is used for amplifier. Texas instrument DSP board TMS320F2812 is used to control the VSC and is also used

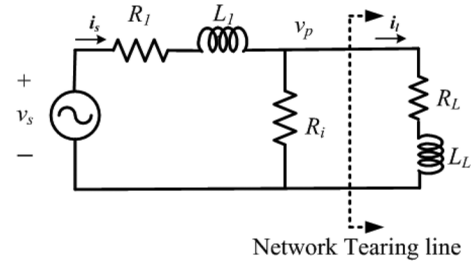


Fig. 9. Test circuit of Example 2.

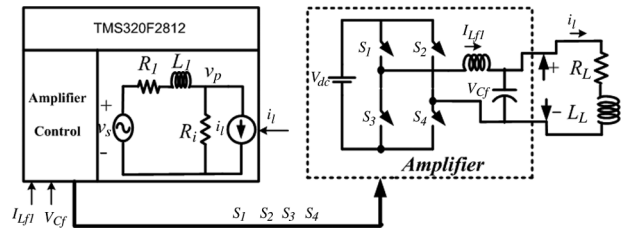


Fig. 10. Schematic diagram of the hardware setup for Example 2.

to simulate the test side network. LEM current sensor is used to measure the filter inductor current. For the capacitor voltage of the LC filter of the amplifier, voltage is scaled down and measured with the help of an operational amplifier. The PCC voltage (v_p) was used as reference voltage for amplifier. Test side current is sensed using LEM current sensor and an analog-to-digital converter which is inbuilt in this DSP.

Example 2: Here, a simple circuit, as shown in Fig. 9, is tested. The tearing line is as shown in this figure. Since supply side circuit is simulated and the amplifier control is computed in the same DSP chip, the reference voltage (v_p) for amplifier is directly passed and no DAC is required here. The supply side is simulated using discrete time state equation with a time step of 40 μs. The schematic diagram of the hardware setup for this example is shown in Fig. 10.

The state equations for supply side circuit are represented as follows:

$$A = \frac{-(R_s - R_i)}{L_s}, \quad B = \begin{bmatrix} \frac{1}{L_s} & 0 \\ 0 & \frac{R_i}{L_s} \end{bmatrix}. \tag{11}$$

The discrete-time equivalent of the circuit for a sampling time $(T_s = 40\ \mu\text{s})$ is given by

$$x(k+1) = Fx(k) + Gu_c(k) \tag{12}$$

where $x(k) = i_s$ and $u_c^T = [v_s\ i_l]$.

The system parameters are: $R_l = 10\,\Omega$, $R_L = 200\,\Omega$, $L_l = 20$ mH and $L_L = 54$ mH. The supply voltage is chosen with a peak of 20 V and a frequency of 50 Hz. The load current (i_l) is taken to the supply side using current sensor and an analog-to-digital card. It is then filtered using an averaging process.

The entire (complete) network without tearing is simulated in PSCAD. This is then compared with the experimental results obtained with torn network, as per the experimental set up discussed. Fig. 11 shows the PCC voltage (v_p), while Fig. 12 depicts the test side current (i_l). It is clear that the experimental results with network tearing are similar to simulation results with

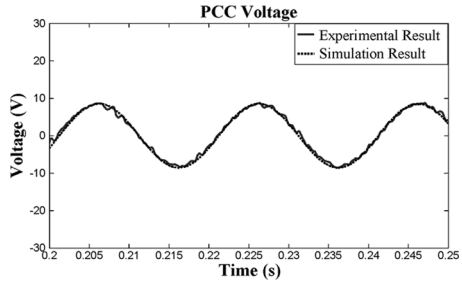


Fig. 11. Experimental and simulation result for PCC voltage (v_p).

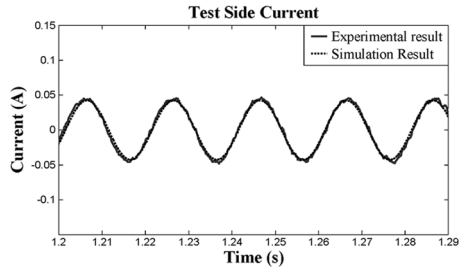


Fig. 12. Experimental and simulation result for i_l.

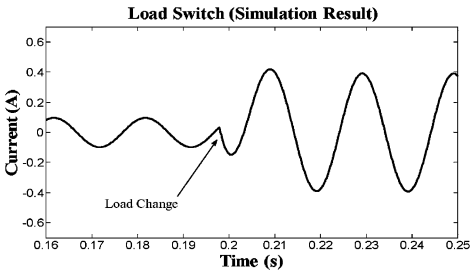


Fig. 13. Simulation result for i_l.

the complete network. These results prove that the testing of power system network is practically feasible using power network-in-loop concept.

In the next step of this test, a 30 μF capacitor is connected in series with R_L and L_L and value of R_L was reduced to 10 Ω. The capacitor is switched to examine the transient behavior of torn network. With the circuit being in steady state, the capacitor is bypassed (short circuited) in the simulation studies. Fig. 13 shows the current i_l. Note that the reactance of the capacitor is much larger than that of the inductor. Hence the load impedance reduces as the capacitor is bypassed. This results in an increase in the current as is evident from Fig. 13. The experimental waveform is shown in Fig. 14. The transient behaviors are not identical since the dynamics of the switch and the instant of bypass switch closing could not be matched.

Example 3: In this example, the feasibility of power network tearing is extended by testing the interaction of two generators. Fig. 15 shows the network under test in which the network tearing line is also indicated. The supply side network is simulated in the DSP using state equations of (11) and (12) since the supply side remains unchanged from Example 2.

The grid voltage is scaled down using an auto-transformer and used as the voltage source v_2. Synchronization between v_2

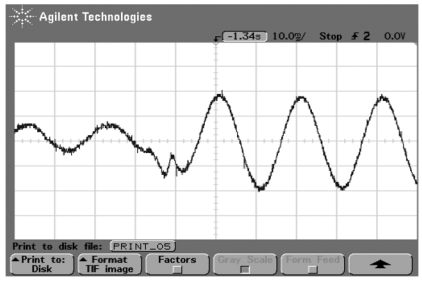


Fig. 14. Experimental result for i_l during capacitor switching.

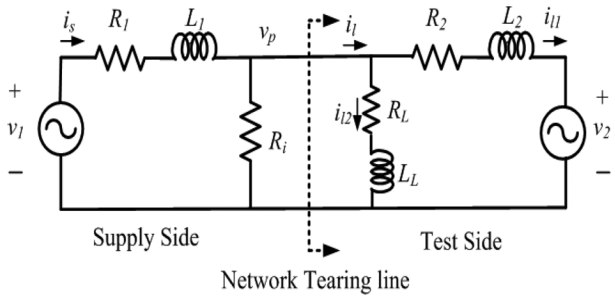


Fig. 15. Circuit under test for two generators interaction.

TABLE I
SYSTEM PARAMETERS FOR EXAMPLE-3

System Quantities	Value
v_1	$32.5\times\sin(\omega t)$
v_2	$10\times\sin(\omega t+\phi)$
R_l	10Ω
L_l	20mH
R_i	5Ω
R_L	200Ω
L_L	54mH
R_2	5Ω
L_2	9mH

and v_1 must be established to avoid a frequency mismatch. Generally, a phase lock loop (PLL) is used to establish synchronization between two sources. To avoid complexity, the grid voltage is scaled down and passed to the DSP through an ADC. We can then set the frequency of the voltage source v_1 to that of the mains. The voltage magnitude and phase difference (Φ) can be created using software program in the DSP by storing one cycle data at a 40 μs sampling rate. The study system parameters are shown in Table I.

For this test, again the PSCAD simulation of the complete network is compared with the experimental results. First the network is tested with zero phase difference between v_1 and v_2. Fig. 16 shows the current at network tearing point (i_l). Fig. 17 shows the comparison between the line currents (i_{l1}). It is clear from these figures that the currents in the torn network are similar to those in the simulated entire network. Fig. 18 shows the phase difference between i_{l1} and v_2, obtained experimentally. The PCC voltage is shown in Fig. 19.

In the next stage of this test, a phase difference of 20° was created between v_1 and v_2 in which the phase of v_1 is advanced by 20° vis-à-vis that of v_2 in the software program.

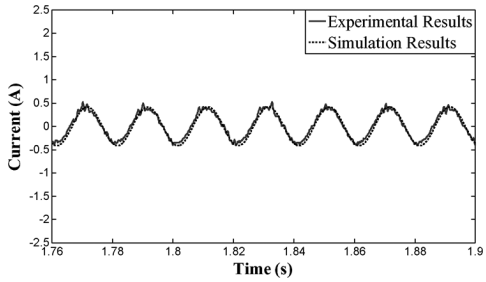


Fig. 16. Current at network tearing point (i_l).

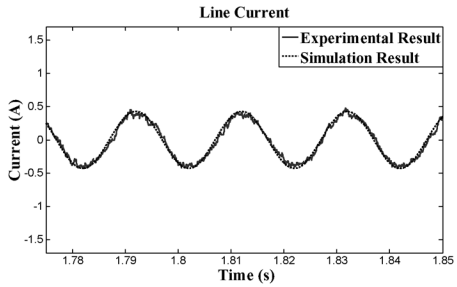


Fig. 17. Line current passing through R_2 (i_{l1}).

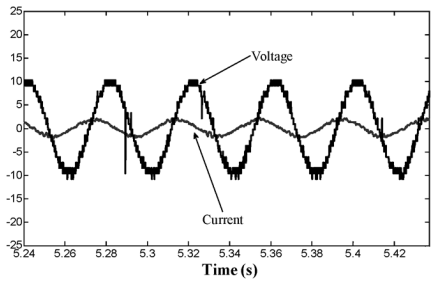


Fig. 18. Phase difference between i_{l1} and v_2.

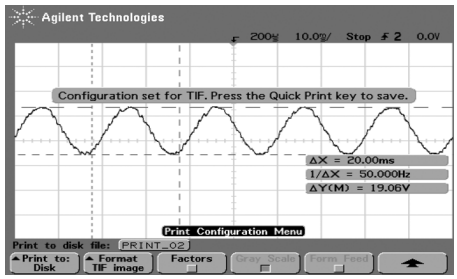


Fig. 19. Tearing point (PCC) voltage v_p.

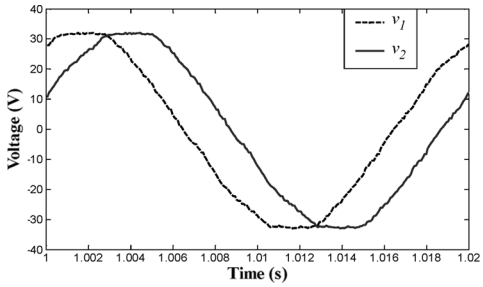


Fig. 20. v_1 and v_2 with 20° phase difference.

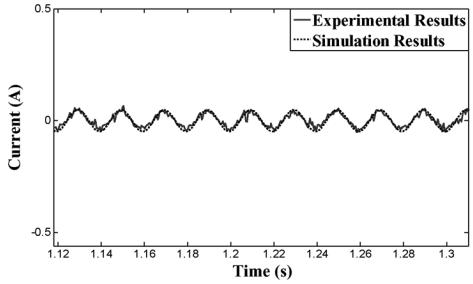


Fig. 21. Current at network tearing point (i_l).

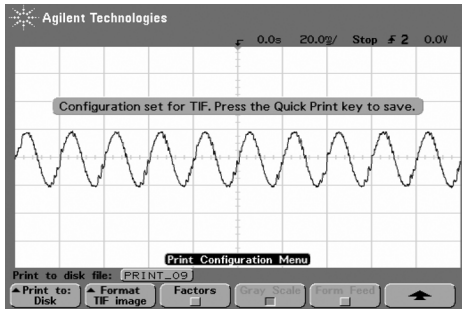


Fig. 22. Tearing point (PCC) voltage v_p.

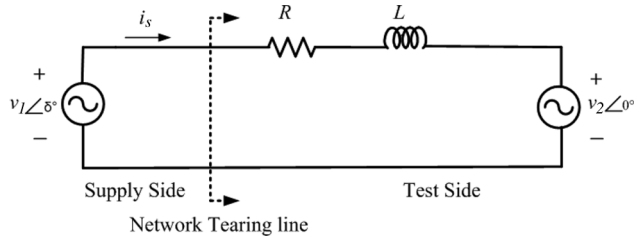


Fig. 23. Circuit under test for Example 4.

Fig. 20 shows the voltage v_1 and v_2. Fig. 21 shows the current at network tearing point (i_l). Since the case magnitude of i_l is very small, the noise to signal ratio of the current sensor is high. Therefore the current i_l is significantly distorted. However, the performance of the system does not get affect due to the small magnitude of the current. This is evident from the PCC voltage shown in Fig. 22.

Example 4: To study the two way interaction of power network in loop, the network shown in Fig. 23 is considered, where the voltage source v_2 is the utility bus. The voltage source v_1 is simulated in the DSP and its angle (δ) is varied according to the swing equation.

The swing equation is solved in discrete time domain at sampling rate of 40 μs. It can be represented as follows:

$$\frac{d}{dt}\begin{bmatrix}\omega\\ \delta\end{bmatrix}=\begin{bmatrix}\frac{-D}{2H} & 0\\ 2\pi f & 0\end{bmatrix}\begin{bmatrix}\omega\\ \delta\end{bmatrix}+\begin{bmatrix}\frac{1}{2H}\\ 0\end{bmatrix}(P_m-P_e). \quad (13)$$

The discrete-time equivalent of the swing equation at the sampling frequency of $1/T_s$ is given by

$$x(k+1)=Fx(k)+Gu_c(k). \quad (14)$$

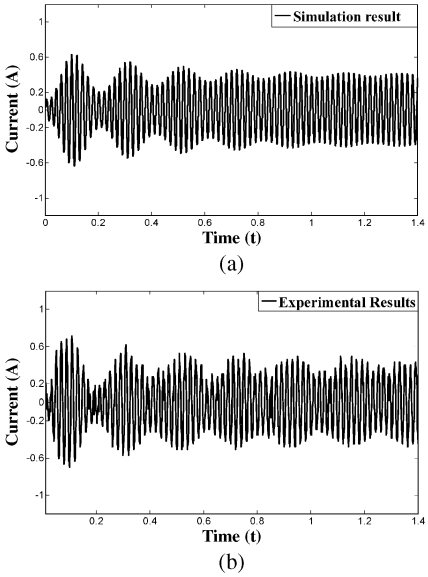


Fig. 24. Initial transients in i_s: (a) simulated waveform and (b) experimental waveform.

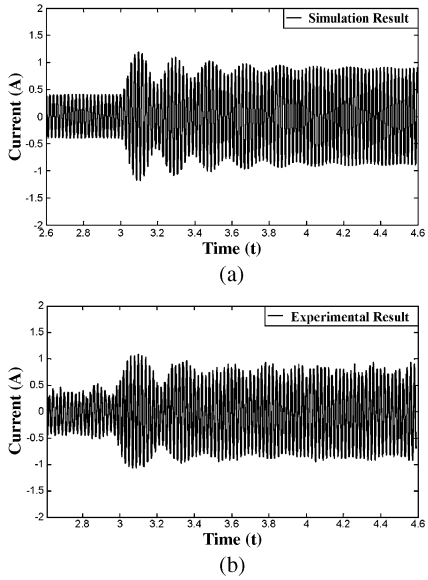


Fig. 25. Transients in i_s during power change. (a) Simulated waveform. (b) Experimental waveform.

The parameters chosen for the study are

$$R = 15\,\Omega,\ L = 20\,\text{mH},\ f = 50\,\text{Hz},\ D = 6 \text{ and } H = 0.5$$
$$v_1 = 12 \times \sin(\omega t + \delta) \text{ and } v_2 = 10 \times \sin(\omega t)$$

To calculate the instantaneous electrical power (P_e), i_s is sensed using the analog-to-digital card and multiplied with v_1. The angle δ is calculated using (14) by the DSP. To overcome the problem of frequency mismatch between v_1 and v_2, mains grid voltage is sensed using an analog-to-digital card and scaled to form the magnitude of v_1, while a phase lead is provided according the calculated value of δ as per (14).

Initially P_m is set to 2 watts. Fig. 24(a) and (b) shows the simulation and experimental results, respectively, of the initial transient in i_s. It is clear from these that the initial transients are similar.

The value of P_m is now suddenly changed from 2 to 5 watts. It is well-known that as P_m increases; both the values of δ and i_s will increase. Fig. 25(a) shows the simulation result of change in P_m, while Fig. 25(b) shows the waveform obtained experimentally. It can be seen that the magnitudes and trends are similar for both these waveforms.

Hence, this experiment proves that the transient study of power system network can be performed using the proposed power network in loop concept. For study of big power network, high speed real time digital simulators are required so that the supply side network can be simulated in lesser time.

VI. Power Network in Loop of a Complex System

So far we have demonstrated the proposed concept of power network in loop for simple systems and have verified it through simulations and experiments. In this section, we shall show that this concept of tearing is valid even in the case of more complex networks. The dynamic interaction will be verified through simulation studies only. The system is considered to be single phase.

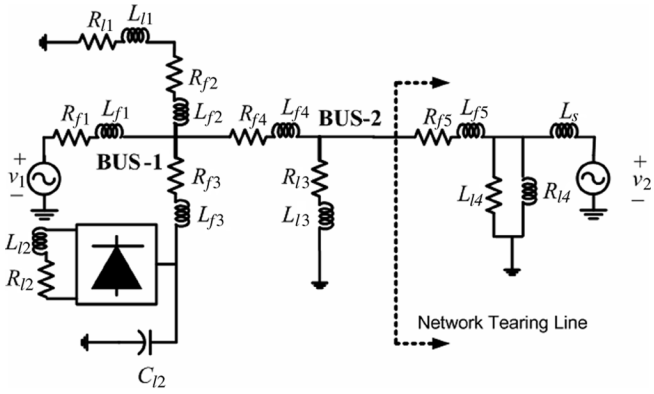


Fig. 26. Complex study system.

Example 5: Let us consider the system as shown in Fig. 26. In this figure, different feeder sections are denoted by the subscript "f," while the loads are denoted the subscript "l," The system parameters for the network are listed in Table II. It is assumed that the circuit on the left of the network tearing line (the supply side) is simulated in a digital simulator, while the circuit on the right (test side) consists of physical systems with the interface driven by an amplifier. Both these systems are simulated in PSCAD. The amplifier is controlled with discontinuous hybrid voltage control. The network tearing line is also indicated in this figure. This network has 2 buses and 5 feeders. Voltage sources v_1 and v_2 are connected to Bus-1 and Bus-2 through feeders one and five, respectively. There is a rectifier load connected to Bus-1 through feeder 3 that injects the harmonics to the system.

The PCC voltage of the complete network without tearing and the torn network with the VSC amplifier are shown in Fig. 27(a), while the error between these two voltages is shown in Fig. 27(b). The average voltage error is 2%. The currents flowing in the test side for the two networks (without tearing and torn) are shown in Fig. 27(c), while the error between these

TABLE II
PARAMETERS OF THE SYSTEM OF Fig. 24

System quantities	Values
System frequency	50 Hz
Voltage Source v_1, v_2	9 sin (ωt)
Feeder (R_{f1}, L_{f1})	0.4032 Ω, 12.8 mH
Feeders (R_{f2}, L_{f2}), (R_{f3}, L_{f3}), (R_{f4}, L_{f4}),	0.2016 Ω, 6.4 mH
Source inductance (L_s)	5 mH
Load (R_{l1}, L_{l1}), (R_{l3}, L_{l3}), (R_{l4}, L_{l4})	50 Ω, 100 mH
Feeders R_{f5}, L_{f5}	1.25 Ω, 6.4 mH
Load (R_{l2}, L_{l2})	10 Ω, 100 mH
Filter capacitance C_{l2}	50 μF

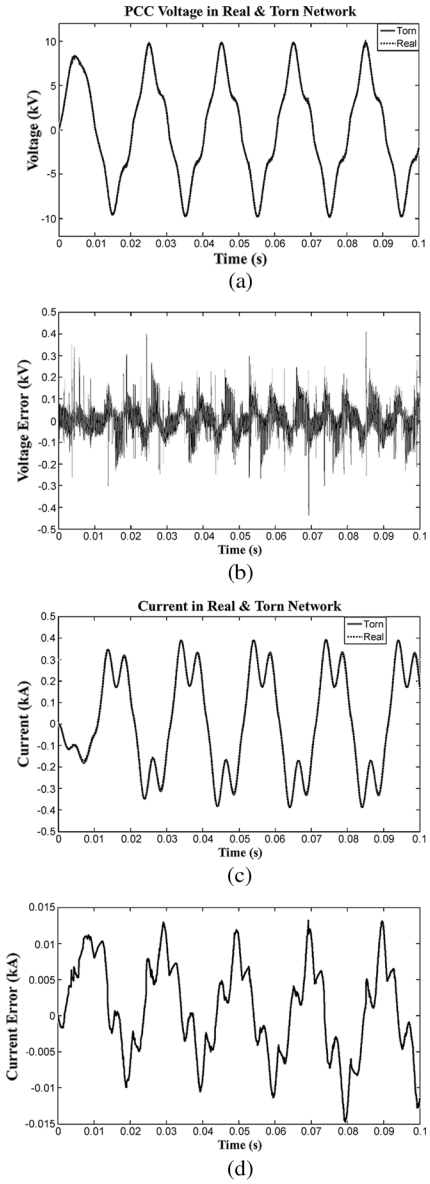


Fig. 27. Voltage, current, and their errors in Example 5.

two quantities is shown Fig. 27(d). The average current error is 3%.

Example 6: In this example, we investigate the behavior due to voltage sag and swell in the source voltage of the supply side of the system of Fig. 26 and Table II. A sag in the source voltage is created at 0.5 s, where the source voltage is decreased to 7 kV

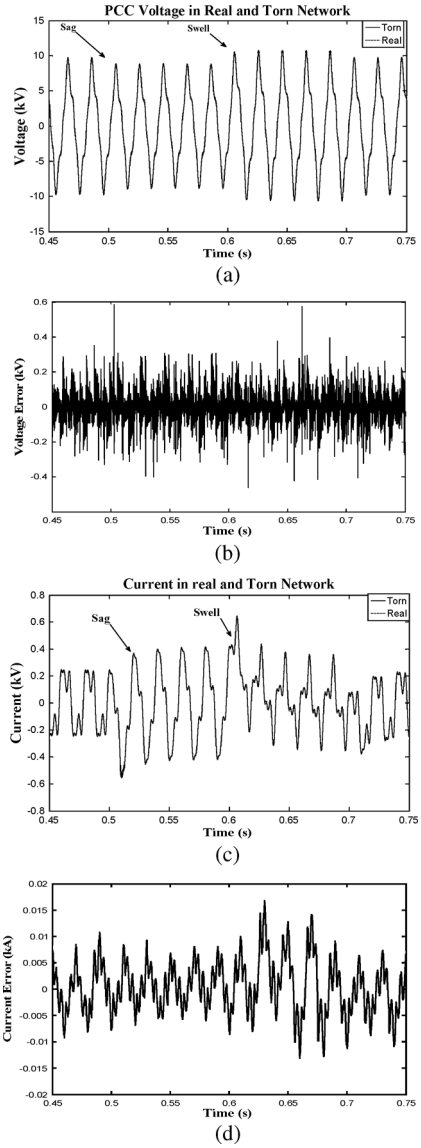


Fig. 28. Voltage, current, and their errors in Example 6.

(L-N Peak). This is followed by a swell in this voltage at 0.6 s, where the voltage becomes 11 kV (L-N peak). The voltage returns to its nominal value (9 kV) at 0.7 s.

Fig. 28(a) shows the PCC voltage of the complete and the torn networks, while the voltage error is shown in Fig. 28(b). The average voltage error is less than 2%. However at the points of the occurrence of voltage transients, the error shoots up to about 3.5%. Fig. 28(c), (d) shows the current in the actual and torn networks and error between these two currents. It is clear from Fig. 28(d) that the current error is less than 5%.

Example 7: In this example effect of line to ground faults at buses 1 and 2 is examined. At $t = 0.5$ s, the fault is created at Bus 1 and it is removed at $t = 0.6$ s. Again at $t = 0.7$ s, a fault is created at Bus 2, which is removed at $t = 0.8$ s. Due to either of these faults, the PCC voltage decreases and test side current increases. Fig. 29(a) shows the PCC voltage in the actual and torn networks. It is clear from figure that the amplifier is able to track the voltage closely even when it reduces due to the faults. Fig. 29(b) shows error in the PCC voltages. It is clear from this

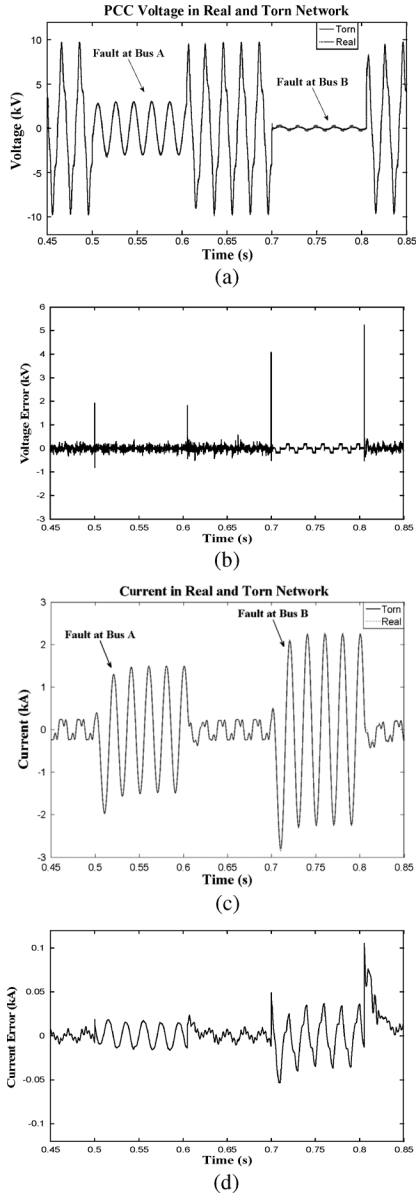


Fig. 29. Voltage tracking of a complex system at the time of faults.

figure that except for the spikes at the instants of voltage change, the error is less than 3.5%. Fig. 29(c) shows the current in the actual and torn networks, while their error is plotted in Fig. 29(d). The average current tracking error is less than 2.5%.

VII. Conclusion

In this paper, a new concept has been proposed. This power network in loop provides a new method for testing of power system components. This paper shows how this can be applied to general power networks through simulation and experimental studies. The research shows that a subsystem of a power network can be interfaced with a real-time simulation using the switching amplifier. The amplifier is capable of amplifying the voltage signal received from the real-time simulation. This can represent the effect of the simulated network, which can be complex. This amplified voltage can then be interfaced with a small physical subsystem. Using this concept, the effect of different faults and

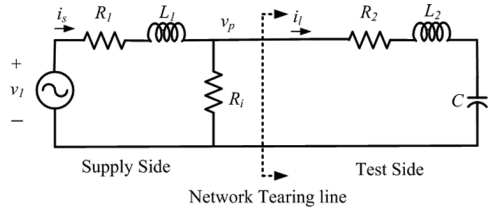


Fig. 30. Network considered for stability studies.

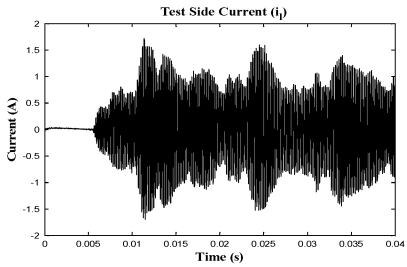


Fig. 31. Test side current containing high frequency ripple components.

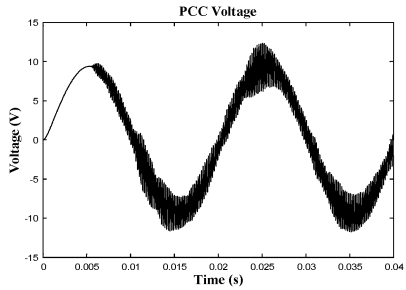


Fig. 32. Distorted PCC voltage.

other conditions in the simulated network can be evaluated on the subsystem under test.

Finally note that given the ready availability of traction converters up to 10 MVA with switch frequency being similar to that considered in this paper, hardware testing at this power level will be feasible. Therefore the method presented in this paper can be used for finite bandwidth testing of medium power sub-systems.

Appendix

This appendix discusses the numerical stability issue and provides a guideline for the remedial action. Consider the network shown in Fig. 30, for which the following parameters are chosen $R_1 = 1\,\Omega, L_1 = 1\,\text{mH}, R_2 = 0.1\,\Omega, L_2 = 0.1\,\text{mH}, C = 10\,\mu\text{F}$ $R_\text{i} = 2\ \Omega$ and $v_1 = \sqrt{2} \times 10\ \sin(\omega t)\text{V}$. The network tearing line is also shown in the figure.

Let us assume that the current i_1 is directly supplied from the test side to the supply side without passing it through the LPF. For the parameters chosen, the complete network without tearing is stable. However, the power network in the loop simulation becomes unstable as shown in Fig. 31. It can be seen from Fig. 7(b) that the voltage error contains the high frequency components, which is then passed to the current i_1. A direct feedback of this current to the supply side will result in the distortion of the PCC voltage as shown in Fig. 32. The distorted PCC voltage further distorts the current, which then distorts the PCC voltage

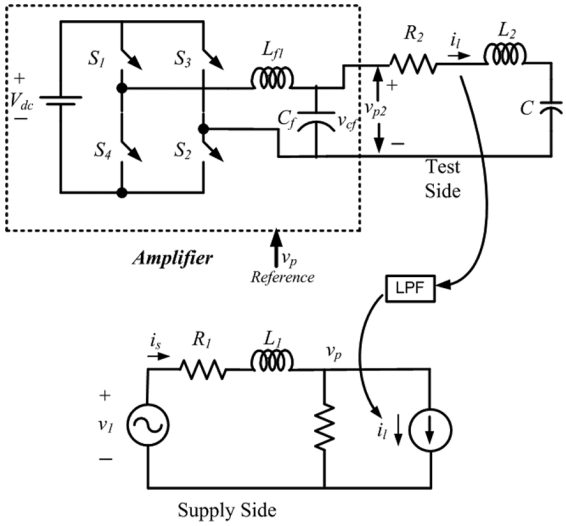


Fig. 33. System structure with LPF.

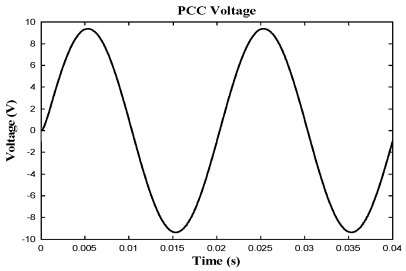


Fig. 34. Stable PCC voltage with LPF.

further. Thus the distortions shown in Figs. 31 and 32 are due to these cumulative effects.

To alleviate the problem, the current i_1 is first passed through a low pass filter (LPF) before passing it to the supply side as shown in Fig. 33. The LPF prevents the injection of the high frequency components of i_1 to the supply side and hence PCC voltage does not get distorted. This results in the stable tracking as shown in Fig. 34. A more formal proof of the effect of the LPF is beyond the scope of this paper.

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