A New Common-mode Voltage Reduction Technique for Multilevel Inverters

Hoda Ghoreishy, Firuz Zare, Senior Member, IEEE, Hamid Hassanpour and Gerard Ledwich, Senior Member, IEEE

Abstract--**In this paper, a novel common-mode voltage reduction technique is proposed for a three-phase multilevel inverter. The technique can be used to control capacitors voltages and load currents with low switching losses. It can be applied to a three-phase three-level inverter with the flying capacitor topology. One of the advantages of this method is that the technique can be applied to more voltage levels without significantly changing the control algorithm. The simulation results of a five-level inverter in this paper indicate that the proposed technique can be used to implement a multilevel inverter.**

Index Terms—**Common-mode voltage (CMV), Multilevel inverters, Pulse width modulation (PWM).**

I. Introduction

CONVENTIONAL two-level pulse width modulated (PWM) inverters have the problem of generating high common-mode voltages (CMV). This problem creates motor shaft voltage through electrostatic couplings between the rotor and the stator windings. It also causes motor shaft voltage among the rotor and the frame. Consequently, the shaft voltage results in excessive bearing currents when it exceeds the dielectric capability of the bearing grease [8].

Currently, there are many CMV reduction techniques in literature [3]-[9]. However, none of these methods consider the switching losses and/or the low frequency harmonics. They may even increase the switching loss [8, 9]. Multilevel voltage source inverters are a new generation of inverters. These are suitable for high power and high voltage applications due to reduced harmonic contents and low voltage stress across the load [1-2, 10]. Multilevel inverters have different voltage levels and switching states. They may reduce and control the CMV which assists the generation of a high quality (low harmonic) voltage and current.

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The CMV is defined as the voltage between the common-point in a three phase Y connected R-L load and the electrical ground. In this paper, a new CMV reduction technique is proposed for the multilevel inverters which controls the capacitors voltages and load currents with low switching losses and low current ripple.

II. Common Mode Voltage Reduction Technique

This paper presents a new pulse pattern for a three-phase multilevel inverter with the flying capacitor topology, minimizing the common mode voltage. This method can be applied to different voltage levels without significantly changing the control algorithm. Multilevel inverters generate different voltage levels. They use capacitors as voltage sources which are placed across the power switches in each leg as shown in Fig.1. This figure shows a three-phase three-level inverter with the flying capacitor topology feeding an inductive-resistive load. The flying capacitors are charged or discharged when the load currents pass through them during operation. In order to operate properly, the controller has to achieve correct switching states to balance the capacitors voltages.

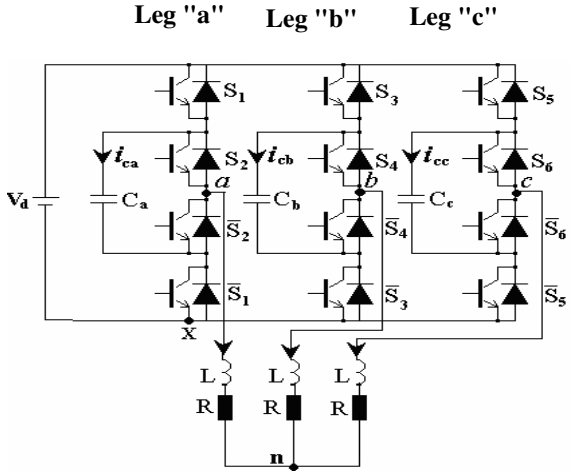

Fig. 1. A three-phase three-level inverter with the flying capacitor topology.

With the capacitors voltages controlled at $V_d/2$, the output voltage of each leg would be a combination of voltages 0, $V_d/2$ and V_d. Table 1 represents different switching states for leg "a". In this table the 0s and 1s indicate the switch is off and on, respectively. As can be seen from the table, there are two switching states (state 01 and state 10) in each leg which

result in output voltage $V_d/2$. In these switching states, depending to the load current direction, the capacitors might be charged or discharged. Fig.2 shows the circuit diagram of switching states $S_1S_2 = 01$ and $S_1S_2 = 10$.

TABLE I
SWITCHING STATES FOR LEG "a" IN FIG. 1.

S_1	S_2	V_{aX}
0	0	0
0	1	$V_d/2$
1	0	$V_d/2$
1	1	V_d

In this figure, the capacitor C_a will be charged in state $S_1S_2 = 10$, and discharged in state $S_1S_2 = 01$ with positive load current; and reversely with negative load current.
Generally, when the switching state is selected to generate $V_d/2$, controlling the capacitor voltage at $V_d/2$ should be considered. Consequently, the controller has to measure the capacitor voltage and compare it to the reference value. Depending to the error voltage and the load current sign, one of the switching states (01 or 10) must be chosen using the adjacent voltage vectors law which minimizes the switching losses.

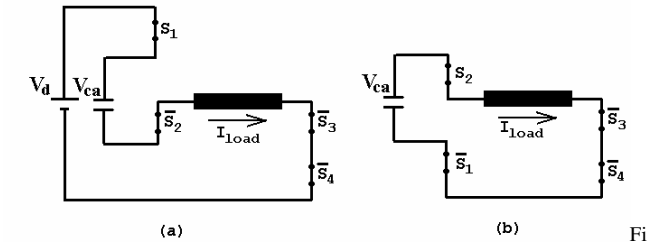

Fig. 2. Circuit diagram when the capacitor in leg "a" is (a) charged (state $S_1S_2 = 10$), (b) discharged (state $S_1S_2 = 01$).

In general, a modulation scheme, such as the space vector modulation, generates the output voltage based on duty cycles corresponding to the average voltage of the sampled reference voltage or current. In a three-level inverter, there are three voltage levels in each switching cycle, so that different PWM schemes can generate the appropriate output voltages. In the proposed method, three pulse positions are defined as shown in Fig.3, where the pulse can be placed at the beginning, center or end of each switching cycle of a phase.
Consequently there are 27 different pulse combinations in each switching cycle of all three phases. Since the CMV is defined as the average voltage of leg voltages ($V_{cm} = (V_{aX} + V_{bX} + V_{cX})/3$), the CMV will also have 27 different voltage shapes in each switching cycle. This average voltage results in a 7- level CMVs: $(\frac{6}{3}\times\frac{V_d}{2})$, $(\frac{5}{3}\times\frac{V_d}{2})$, $(\frac{4}{3}\times\frac{V_d}{2})$, $(\frac{3}{3}\times\frac{V_d}{2})$, $(\frac{2}{3}\times\frac{V_d}{2})$, $(\frac{1}{3}\times\frac{V_d}{2})$ and 0. Since in measuring the common-mode voltages, the midpoint of the dc bus is considered as the reference point, these 7 levels can be rewritten as: $(\frac{3}{3}\times\frac{V_d}{2})$, $(\frac{2}{3}\times\frac{V_d}{2})$, $(\frac{1}{3}\times\frac{V_d}{2})$, (0), $(\frac{-1}{3}\times\frac{V_d}{2})$, $(\frac{-2}{3}\times\frac{V_d}{2})$, $(\frac{-3}{3}\times\frac{V_d}{2})$.

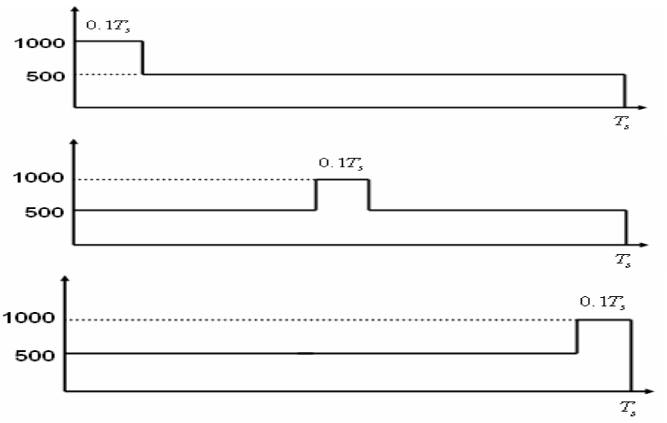

Fig. 3. Three different shapes of a pulse with duty cycle=0.55.

It needs to be noted that more than one combination of the 27 different pulse combinations may have a lower value of CMV in comparison with the other switching states.
In existing CMV reduction methods in multilevel inverters, in the process of generating the output voltage, the CMV is cancelled, but these methods do not consider the switching losses or low order harmonic contents [9]. In the proposed method, the switching states are selected based on the following algorithm to minimize CMV in a three-level three-phase inverter:

- If duty cycle of each leg is in the range of [0.5, 1], the output voltage level is considered between $V_{dc}/2$ and V_{dc}.
- If duty cycle of each leg is in the range of [0, 0.5], the output voltage level is considered between 0 and $V_{dc}/2$.

In the proposed method, three different pulse patterns are used for each leg and the controller achieves the optimum pulse pastern within 27 combinations based on the following criteria:

- low switching losses (using adjacent voltage vector),
- capacitor voltage control (using a correct switching state and based on load current),
- low CMV (shifting the pulse position in such a way to generate low CMV and less zero vectors (00,00,00),(11,11,11)),
- low leakage current and load current ripple (a random selection of the best centering pulse position within the achieved pulses).

Thus, based on the pulse width modulation technique, the controller calculates the duty cycle to generate the output

voltage; the pulse patterns are selected in such a way to minimize the common mode voltage according to Fig.3; the controller achieves the proper switching states in order to control the capacitor voltage based on the adjacent voltage vector and the load current sign; the final pulse pattern is selected based on the best centering pulse position which improves the load current ripple and also minimize dv/dt corresponding to low leakage current. Figure 5 shows steps of this procedure in a flowchart.

This method does not fully cancel the common mode voltage but it reduces the common mode voltage to a minimum level when the other issues like the switching losses and the current ripple are optimized. In fact centering the pulse pattern is the main criteria for improving the load current ripple. The controller analyses all of the above-mentioned pulse combinations to find the optimal case by considering the load current harmonic factor as an important issue. There could be more than one combination among the chosen cases that have a better harmonic spectrum compared to other combinations. These are the cases that have more pulses at the center in their switching cycles, for example see case (b) in Fig.3. Finally, the desired case will be randomly chosen from the above cases to apply the system.

For example, Fig.4 shows three different pulse positions where the case (a) shows the traditional pulse centering which has the lowest current ripple but a higher common mode voltage; while the case (b) has the lower common mode voltage but the pulse pattern is not in such a case to generate a low current ripple. The case (c) shows an optimum case, where the pulse in leg "a" is placed at the beginning of the switching cycle and the pulses in legs "b" and "c" are placed at the center which gives the lower common mode voltage (same as the one in Fig. 3(b)) but generates a better load current.

The controller randomly selects one of the optimum pulse patterns. This is another advantage of the proposed method which spreads the spectrum contents of the output voltage; results in a low electromagnetic interference and mechanical vibration.

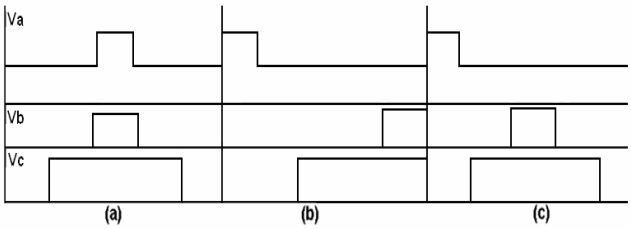

Fig. 4. Pulse pattern for a three phase inverter: (a) the centering pulse pattern, (b) one of the 27 pulse pattern combinations, and (c) optimum pulse pattern with centering and low common mode voltage.

III. SIMULATION RESULTS

To evaluate performance of the proposed technique, it was simulated using the Matlab software. The circuit was simulated using a three-phase three-level flying capacitor inverter with an inductive-resistive load, and the parameters were chosen as below: $R = 1\Omega$, $L = 23mH$, $C_a = C_b = C_c = 1mF$, $V_d = 1000v$.

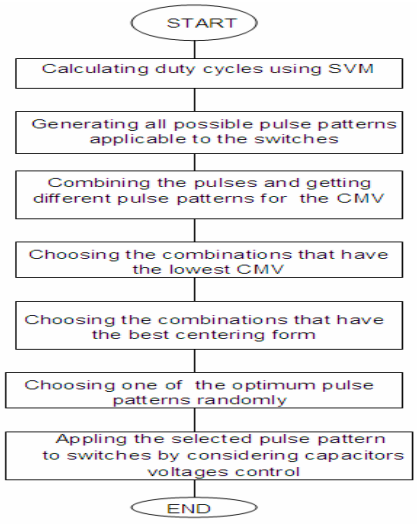

Fig. 5. Figure 5 Algorithm of the novel method

Capacitors in the circuit are assumed to have $V_a = 750v$, $V_b = 250v$ and $V_c = 500v$ initial voltages to find how the controller can control these voltages. The simulation results are shown in Fig. 6. These results are compared to the results of the case that all of the pulses are at the center of the switching cycles shown in Fig.7. In this performance comparison, the simulations have been carried out for three cycles (60 ms in total).

It can be seen from Fig. 6 that the proposed technique has many advantages over the conventional technique in reducing the common-mode voltage. In this method, the common mode voltage is decreased from five levels (in conventional method) down to three levels for the same switching losses while the capacitors voltages are controlled.

The load current and its harmonic spectrum, in both conventional and novel methods, have also been shown for one cycle in Fig.8. As can be seen, there is no considerable difference between the harmonic spectrums of the two methods. It is a trade off between quality of output voltage and reducing common-mode voltage for a same switching frequency. As the voltage vectors are selected randomly to reduce the common-mode voltage, this issue distributes the spectral contents of output voltage which has a impact to reduce the peak of harmonic content at switching frequency and its multiple. In fact, CMV reduction increases the current total harmonic distortion (THD) but the novel method proposed here, keeps the best possible.

As it was mentioned before, the proposed technique can be applied to more than three voltage levels without significantly changing the control circuit. The simulation results on a five-level inverter have also been shown in figures 9-11 to further support this claim. The reduction techniques for three-level and five-level inverters are the same. The only difference is that a five-level inverter with the flying capacitor topology has three capacitors in each leg. On the other hand, there are 9 capacitors in a three-phase five-level inverter that their different charge and discharge states must be considered according to load current. In each leg, the capacitors are charged at their initial values that are 250, 500 and 750 volts.

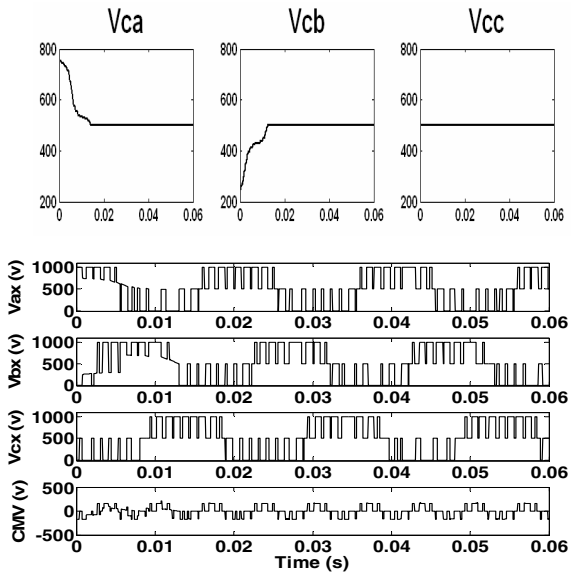

Fig. 6. Capacitors voltages, leg voltages and CMV in the novel method for a three-phase three-level inverter with inductive-resistive load.

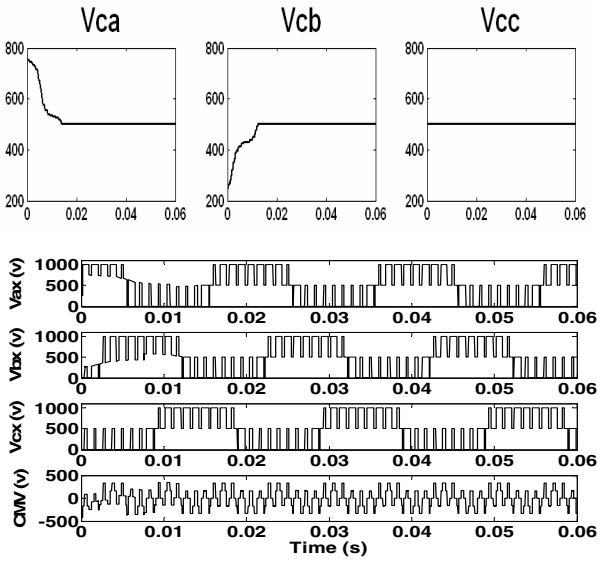

Fig.7. Capacitors voltages, leg voltages and CMV in the conventional method for a three-phase three-level inverter with inductive-resistive load (all of the pulses are centered).

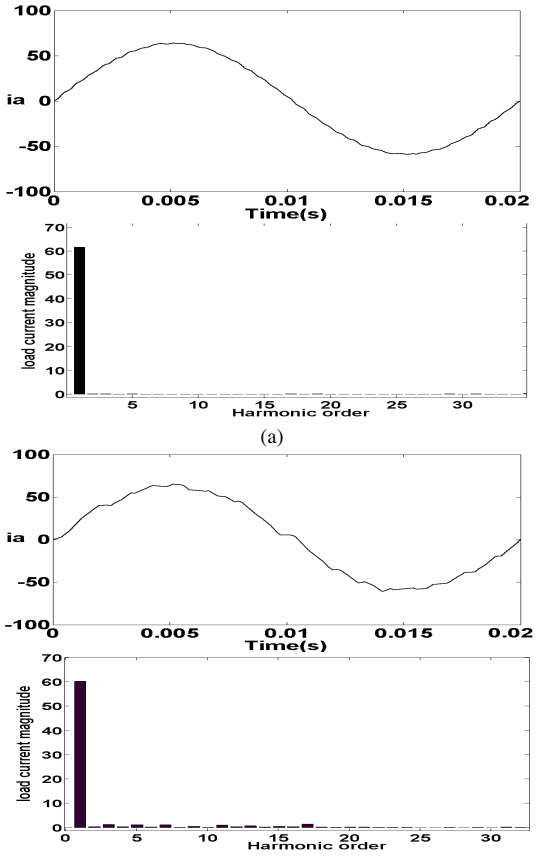

Fig.8. Load current and its harmonic spectrum in a three-phase three-level inverter (a) conventional method, (b) novel method.

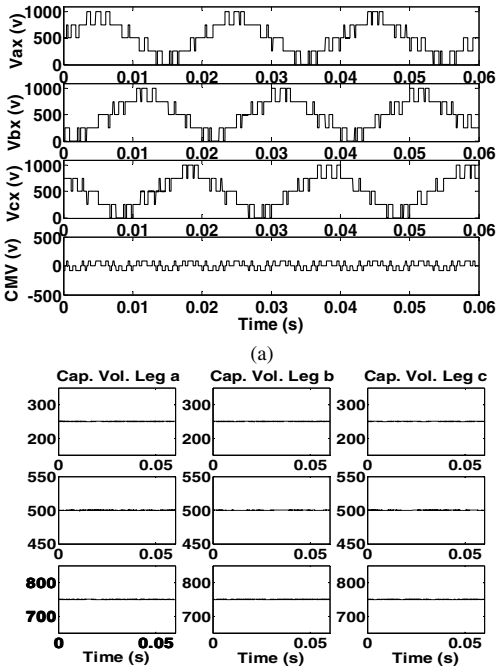

Fig.9. Novel method for a three-phase five-level inverter (a) leg voltages and CMV, (b) capacitors voltage.

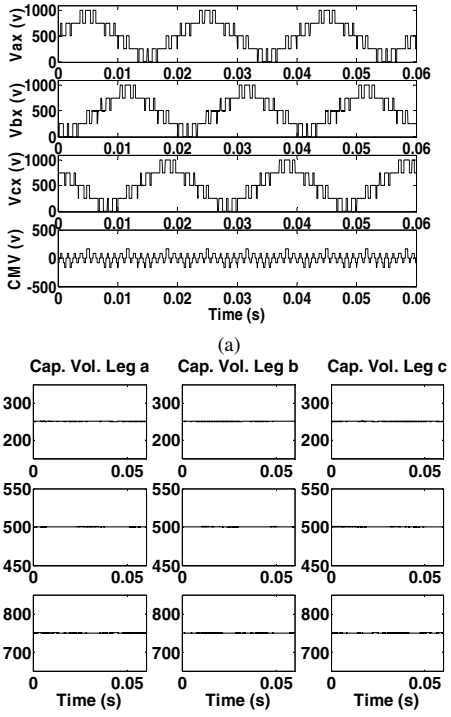

Fig. 10. Conventional method for a three-phase five-level inverter (a) leg voltages and CMV, (b) capacitors voltage.

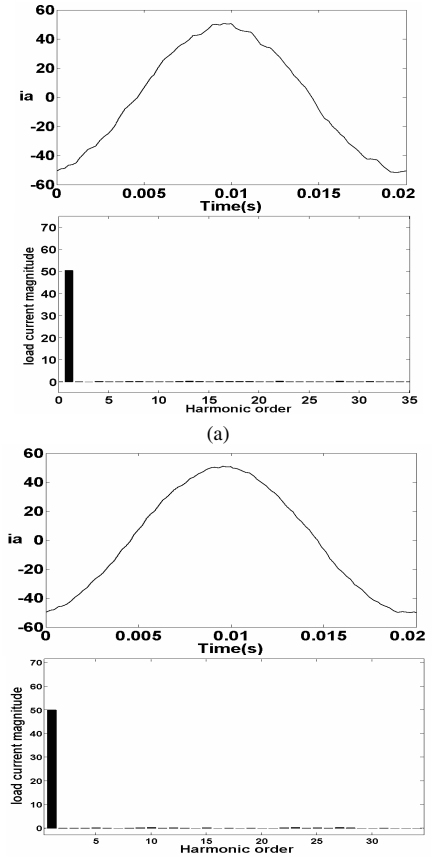

Fig. 11. Load current and its harmonic spectrum in a three-phase five-level inverter (a) novel method, (b) conventional method.

A three-phase five-level inverter has twelve levels of common-mode voltage while it is reduced to 3 levels in the proposed method. The load current and its harmonic spectrum, in both conventional and novel methods, have also been shown for one cycle in Fig 11

IV . CONCLUSION

Multilevel voltage source inverters are a new generation of inverters. They are suitable for high power and high voltage applications due to reduced harmonic contents and low voltage stress**.** In this paper, a novel CMV reduction technique is proposed for a three-phase multilevel inverter which controls the capacitors voltages and load currents with low switching losses. The controller selects one of the optimum pulse patterns (with low CMV) randomly which has another advantage of spreading the spectrum contents of the output voltage for low electromagnetic interferences and mechanical vibration. One of the other advantages of this method is that the technique can be applied to more than three voltage levels without significantly changing the control circuit.

V . REFERENCES

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