Compensation of Distribution System Voltage Using DVR

Arindam Ghosh, *Senior Member, IEEE*, and Gerard Ledwich, *Senior Member, IEEE*

***Abstract*—A dynamic voltage restorer (DVR) is a power-electronic controller that can protect sensitive loads from disturbances in the supply system. In this paper, it is demonstrated that this device can tightly regulate the voltage at the load terminal against imbalance or harmonic in the source side. The behavior of the device is studied through steady-state analysis, and limits to achievable performance are found. This analysis is extended to the study of transient operation where the generation of the reference voltage of the DVR is discussed. Once the reference signals are generated, they are tracked using a switching band scheme. A suitable structure in which the DVR is realized by voltage-source inverters (VSIs) is also discussed. Particular emphasis to the rating of this device is provided. Extensive simulation results are included to illustrate the operating principles of a DVR.**

***Index Terms*—Power distribution, control, DVR, converter, power electronics.**

I. Introduction

A DYNAMIC voltage restorer (DVR) is a power-electronic-converter-based device that has been designed to protect critical loads from all supply-side disturbances other than outages. It is connected in series with a distribution feeder and is capable of generating or absorbing real and reactive power at its ac terminals. The basic principle of a DVR is simple: by inserting a voltage of required magnitude and frequency, the DVR can restore the load-side voltage to the desired amplitude and waveform even when the source voltage is unbalanced or distorted. Usually a DVR is connected to protect sensitive loads during faults in the supply system.

The first DVR was installed in North Carolina, for the rug manufacturing industry [1]. Another was installed to provide service to a large dairy food processing plant in Australia [2]. A DVR is usually built round a dc–ac power converter that is connected in series with a distribution line through three single-phase transformers. The dc side of the converter is connected to a dc energy-storage device. The energy state of the device is regulated by taking power from the feeder.

The field of series compensation in distribution system is relatively new. Peng *et al.* have proposed the use of series active filters in conjunction with shunt passive filters [3]. By integrating shunt and series active filters, Fujita and Akagi [4] have proposed a unified power-quality conditioner that is capable of eliminating voltage flicker, negative sequence current, and harmonics. Campos *et al.* have proposed a series compensator for the correction of supply-side unbalance and voltage regulation [5]. Weissbach *et al.* have proposed a series compensator that is supplied by a flywheel energy-storage unit to ride over any transient that may occur [6].

This paper discusses the use of series reactive injection as a voltage regulator. The approach taken is to develop analytical aspects and to illustrate these by examples of a simplified distribution system. The steady-state capabilities are examined initially and limits to the achievable correction are discussed. Potential modes for transient operation of the DVR are compared and a control strategy is developed. This strategy combines the method of instantaneous symmetrical components and complex Fourier transform relations. The proposed method, based on half-cycle averaging, can eliminate supply-side unbalance and distortion. A modification to the algorithm when the theoretical limit of achievable load voltage is reached is also suggested.

So far, the analysis deals with an ideal voltage injection. The practical implementation of the DVR using inverters raises additional issues of switch-frequency injection. The practical aspects of the control of the necessary resonant filter draw upon switching-control theory. The resulting transient control shows that for many circumstances, balancing, harmonic rejection, and voltage restoration can be implemented without the injection of real power.

II. DVR Characteristics

In this section, we shall present the fundamental, positive-sequence, steady-state analysis of a DVR-connected power system. The proposed voltage regulation scheme is shown in Fig. 1. This consists of the following:

- *DVR:* represented voltage sources v_{fa}, v_{fb}, and v_{fc};
- *Supply voltage:* represented by sources v_{sa}, v_{sb}, and v_{sc}.

The DVR is connected between a terminal bus on the left and a load bus on the right. The voltage sources are connected to the DVR terminals by a feeder with an impedance of $R + jX$. In this study, we assume that the loads are balanced and the load impedance is given by $Z_l = R_l + jX_l$. It is to be noted that the phase angle ϕ_l between the load terminal voltage v_l and the line current i_s, depends on the load impedance and is independent of the line impedance or the DVR voltage.

In the analysis to be presented, we assume that the source voltage is 1 p.u. and we want to regulate the load voltage to 1 p.u. by injecting a voltage from the DVR. We stipulate the following condition on the DVR:

- The DVR does not supply any real power in the steady state. This implies that the phase-angle difference between DVR

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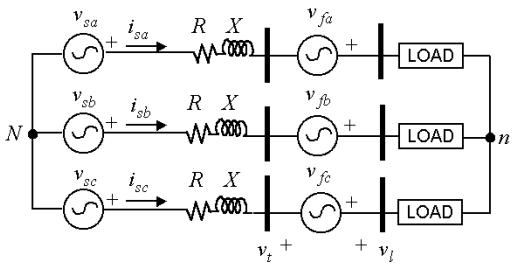

Fig. 1. Schematic diagram of a DVR-connected power system.

voltage phasor and line-current phasor must be $\pi/2$ in the steady state.

Case 1: When the Line Resistance Is Negligible.

The only way the load and source-voltage magnitudes can be equal in this case is when the DVR completely compensates for the reactive drop in the feeder. This will force the source and load voltages to be in phase.

Case 2: The Load Is Resistive (i.e., $X_l = 0$).

The phasor diagram for this case is shown in Fig. 2. It can be seen that in this case, the magnitude of the source and load voltages will never be equal unless the condition that the DVR must not supply (or absorb) real power is relaxed.

Case 3: The General Case.

The common case is where the load current lags, the load voltage and the feeder resistance are not neglected. To draw a phasor diagram, we assume that the load voltage is fixed at V p.u. and the source voltage is allowed to vary. Since the primary target is to make the magnitudes of V_l and V_s equal, the locus of desirable V_s is the semicircle as shown in Figs. 3 and 4.

Fig. 3 shows the limiting behavior. Let us assume that the resistive (RI_s) drop in the feeder is greater than the length SP. Since the DVR must inject voltage in quadrature with the load current, it will not be possible to get the source voltage to be equal to V p.u. Even though the source voltage can be fixed anywhere along the line NM, the maximum of $|V_l|/|V_s|$ is obtained when the source voltage is equal to OM. On the other hand, if the RI_s drop is exactly equal to SP, the load-source voltages can be made equal by aligning the source voltage with the line current. The magnitude of the source voltage is then equal to OQ.

Let us consider the limiting case shown in Fig. 3, where we assume that the magnitude of the source voltage (OM) is equal to 1 p.u. and that of the load voltage is V p.u. We then have the distance $OT = V\cos\phi_l$. Hence, the distance MT will be equal to $1 - V\cos\phi_l$; thus, $RI_s = 1 - V\cos\phi_l$.

Now, suppose the RI_s drop is less than the limiting value. The DVR must then compensate the entire reactive drop in the feeder and provide additional injection so that the source voltage becomes V p.u. It can be seen from Fig. 4 that there are two possible intersection points with the semicircle—one at A and the other at B. This implies that two possible values of DVR voltage can be obtained for this case. In the first case, the source voltage will be along OA, while in the other case, it will be along OB. Needless to say, the best choice is the A intersection, requiring much smaller voltage injection from the DVR.

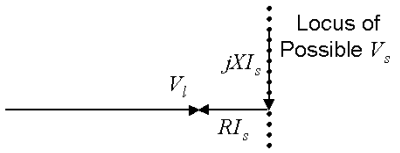

Fig. 2. Phasor diagram for case two.

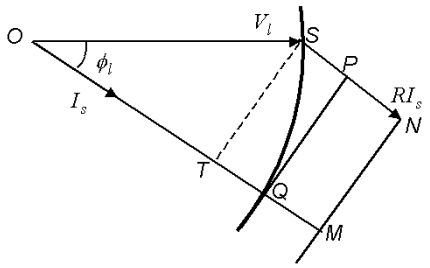

Fig. 3. Phasor diagram of the limiting case.

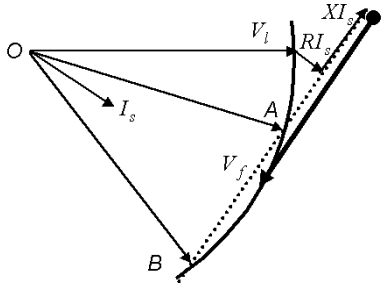

Fig. 4. Phasor diagram showing multiple solutions.

To obtain a valid solution we require that

$$RI_s \le 1 - V\cos\phi_l \;\Rightarrow\; I_s \le \frac{1 - V\cos\phi_l}{R}. \qquad (1)$$

The changes in the source current with changes in the load power factor angle are shown in Fig. 5 for different values of the line resistance and $V = 1.0$ p.u. From this, it can be seen that as the line resistance increases, the current drawing capacity of load decreases. This implies that if the load requires more current than is permissible, the DVR will not be able to regulate the load voltage to 1 p.u.

Alternatively, we can also regulate the load voltage to a value that is other than 1 p.u. Fig. 6 shows the system-load current characteristics for different values of V. It can be seen that as the requested load voltage V decreases, the maximum current drawing capacity of the load increases. At the same time, a restriction is also put on the minimum current that can be drawn by the load. Similarly, as V increases, the current drawing capacity of the load decreases. Clearly, even for zero-load current, a voltage of 1.05 cannot be achieved for low-power-factor angles.

Example 1: In this example, we illustrate the procedure for the steady-state computation of DVR voltage. Let the feeder and load impedances be, respectively, $0.05 + j0.3$ and $2 + j1.5$ p.u.

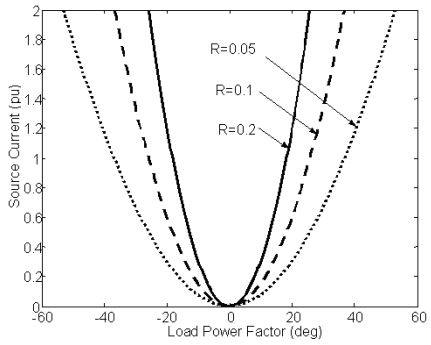

Fig. 5. Compensatable source current versus power factor, source and load voltages equal: a range of feeder resistance.

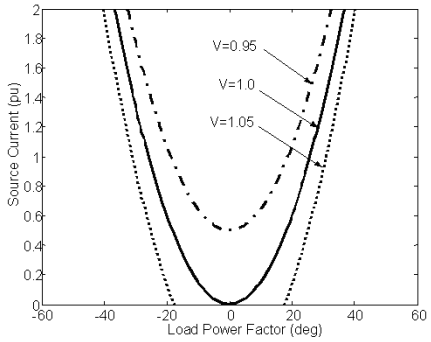

Fig. 6. Compensatable source current versus load power factor: a range of target voltages.

We now connect a DVR aiming to regulate the load voltage to 1 p.u. Let us assume that $V_l = 1\angle 0^\circ$ p.u. The line current is then

$$I_s = \frac{1\angle 0^\circ}{R_l + jX_l} = 0.4\angle -36.87^\circ \text{ p.u.}$$

For zero DVR power, its voltage must be in quadrature to the line current. We then have

$$V_f = |V_f| e^{j(\angle I_s + 90^\circ)} = |V_f| \angle 53.13^\circ = |V_f|(a_1 + jb_1) \quad (2)$$

where $a_1 + jb_1$ is a unit phasor at 90° to I_s. Again, from Fig. 1 we get

$$V_s + V_f = V_l + (R + jX)I_s = V_l + a_2 + jb_2 \quad (3)$$

where $a_2 + jb_2$ represents the feeder drop.

Substituting (2) in (3) and rearranging, we get

$$V_s = V_l + a_2 + jb_2 - |V_f|(a_1 + jb_1). \quad (4)$$

Assuming that the magnitude of the source voltage $|V_s|$ is known, we get the following quadratic equation from the magnitude condition:

$$|V_f|^2 - 2\{a_1(1+a_2) + b_1 b_2\}|V_f| + (1+a_2)^2 + b_2^2 - |V_s|^2 = 0. \quad (5)$$

Let us assume that the magnitude of the source voltage is 1 p.u. Then solving (5), we get

$$|V_f| = 0.1476 \quad \& \quad 1.2924.$$

It was mentioned before that these two values of $|V_f|$ correspond to two operating points (A and B) in Fig. 4. We shall obviously choose the lower of the two values.

III. Transient Operation of DVR

The example mentioned before demonstrates how a DVR can be controlled. However, the equations derived from before assume sinusoidal steady-state operation and full system knowledge. It is thus important to derive the steady quantities using half-cycle averaging.

To extract the sinusoidal steady-state quantities, we shall use the instantaneous symmetrical components [7]. This theory has already been used in DSTATCOM application [8]. Let i_a, i_b, and i_c be three-phase instantaneous currents. The power invariant instantaneous symmetrical components are then defined by [7]

$$i_{a012} = \begin{bmatrix} i_{a0} \\ i_{a1} \\ i_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (6)$$

where $a = e^{j120^\circ}$. Similar expression can also be written for voltages.

Let us now denote the zero, positive, and negative sequence phasors as I_{a0}, I_{a1} and I_{a2}, respectively. Defining a vector as $I_{a012}^T = [I_{a0} \;\; I_{a1} \;\; I_{a2}]$, we can use the complex Fourier transform relation [9] to obtain the symmetrical component phasors from

$$I_{a012} = \frac{\sqrt{2}}{T} \int_{t_1}^{t_1+T} i_{a012} e^{-j(\omega t - 90^\circ)}\, dt. \quad (7)$$

Note that the factor $\sqrt{2}$ is used to change from power invariant description to the magnitude invariant description. Furthermore, time interval T is chosen as half a cycle for a low-delay rejection of harmonics and negative phase-sequence effects. This averaging can be between any two points and need not be synchronized with the zero crossing of the current (or voltage) waveform.

Example 2: Let us consider the same system as given in Example 1 except that it is assumed that the peak of the source voltage 1 p.u., and we want to regulate the load voltage so that its peak is also 1 p.u. The system frequency is chosen as 50 Hz. Based on the averaging process discussed in (6), we now use (5) to obtain the DVR voltage. It is assumed that the DVR is realized by three ideal voltage sources and, thus, any change in the DVR voltage is reflected in the load voltage instantaneously. This, however, is not feasible in practical cases when a voltage-source inverter is used to implement the DVR.

The algorithm is implemented in the following steps. The system quantities are phase-locked to a reference point. The half-cycle-averaged positive sequence of the line current is then extracted with respect to the phase lock. The magnitude of DVR voltage is calculated based on (5). The DVR voltage is then synthesized with this magnitude and an angle that leads the line current angle by 90°. We shall call this type-1 control.

In the control technique presented before, it is assumed that entire circuit parameters are known as well as the source voltage. This, however, may not be feasible. Alternatively, the DVR voltage must be synthesized based on local measurements

only. To accomplish that, we note from Fig. 1 that $v_t + v_f = v_l$. We then get

$$V_t = V_l - |V_f|(a_1 + jb_1). \tag{8}$$

Note that as in (2), the term $a_1 + jb_1$ refers to the phasor that is 90° from the line current. Assuming that $V_l = |V_l|\angle 0°$, the equation shown before leads to the following quadratic:

$$|V_f|^2 - 2a_1|V_l|\,|V_f| + |V_l|^2 - |V_t|^2 = 0. \tag{9}$$

This algorithm will be referred to as type-2 control. It requires the measurement of the local quantities only. To implement this algorithm, we need the fundamental of the DVR terminal voltage (v_t) along with the line current.

The system response with these two algorithms is shown in Fig. 7. The DVR is connected to the system after half a cycle (10 ms). The load voltages with type-1 control are shown in Fig. 7(a). It can be seen that the peak of the load voltages becomes equal to 1.0 p.u. as soon as the DVR is pressed into action. The DVR voltages are shown in Fig. 7(b). The real power consumed the DVR with type-1 control and is shown in Fig. 7(c) while type-2 control is shown in Fig. 7(d). It can be seen that the DVR needs a small amount of real power as soon as it is activated. The real power requirement, however, vanishes within half a cycle as the system reaches steady state.

The example shown before illustrates the advantage of using a DVR when the supply is balanced. However, one of the main reasons for the use of DVR is to produce clean, balanced sinusoidal load voltages even when the supply is unbalanced or distorted. We thus have to modify the algorithm just shown to accommodate this.

To extend the algorithm, we stipulate that the positive sequence DVR power must remain zero in the steady state. In the presence of unbalance or harmonics, this means that the instantaneous DVR power will have a zero mean, but will also contain a periodic term. We now divide the DVR terminal voltage as

$$v_t = v_{t1} + v_{t\_rest} \tag{10}$$

where v_{t1} is the positive-sequence component of v_t and v_{t_rest} is the remaining portion containing the influence of unbalance and harmonics. We then modify (9) to obtain the magnitude of the fundamental frequency component of DVR voltage from the quadratic

$$|V_{f1}|^2 - 2a_1|V_l|\,|V_{f1}| + |V_l|^2 - |V_{t1}|^2 = 0. \tag{11}$$

The instantaneous DVR voltage is then obtained by solving the following equation after phase-locking the fundamental component with the reference point

$$v_f = v_{f1} - v_{t\_rest}. \tag{12}$$

This will provide the desired correction of the positive sequence term and will cancel all negative- or zero-sequence components as well as harmonics.

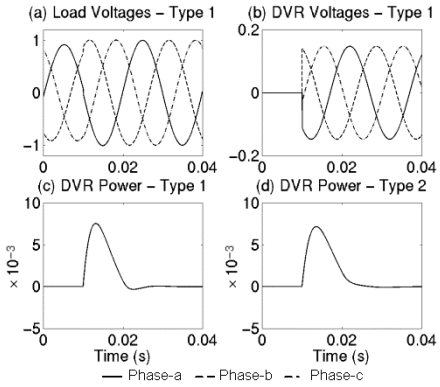

Fig. 7. Performance of DVR under a balanced supply condition.

Example 3: Let us consider the same system as shown in examples one and two. Let the supply voltages be unbalanced so that the voltage peaks of phase a, b, and c are 1.0, 0.9, and 1.2 p.u., respectively. In addition to the unbalance, we have also added fifth and seventh harmonics to the source voltage with their magnitudes being inversely proportional to their harmonic number. The source voltages are shown in Fig. 8(a). The DVR is connected at the end of the first half cycle when the fundamental quantities are extracted. The load voltages are shown in Fig. 8(b). It can be seen that these voltages become balanced and harmonic free with a peak of 1.0 p.u. as soon as the DVR is pressed in service. The magnitude of the source voltage is maximum in the phase c. Thus, the DVR voltage correction for this phase is also maximum. This voltage is shown in Fig. 8(c). It can be seen that peak voltage requirement is approximately 0.5 p.u. The instantaneous DVR power is shown in Fig. 8(d). This oscillating power has a zero mean once the initial transients die off at approximately 0.02 s.

IV. DVR Structure

The examples in the previous section assume that the DVR is realized by ideal voltage sources. In this section, we discuss the compensator structure in which the voltage sources are realized by three voltage-source inverters (VSIs). One phase of the compensator structure is shown in Fig. 9. Three of these VSIs are connected to a common dc storage capacitor. In this figure, each switch represents a power semiconductor device and an antiparallel diode combination. Each VSI is connected to the network through a transformer, and an ac capacitor is connected in parallel to each transformer. The transformers not only reduce the voltage requirement of the inverters, but also provide isolation between the inverters. This prevents the dc-storage capacitor from being shorted through switches in different inverters.

The single-phase equivalent circuit of the DVR is shown in Fig. 10. Here, V_{inv} denotes the switched voltage generated at the inverter output terminals, the inductance L_T represents the leakage inductance of each transformer. The switching losses of the inverter and the copper loss of the connecting transformer are modeled by a resistance R_T. The VSIs operate in a switching band voltage control mode to track the reference voltages generated.

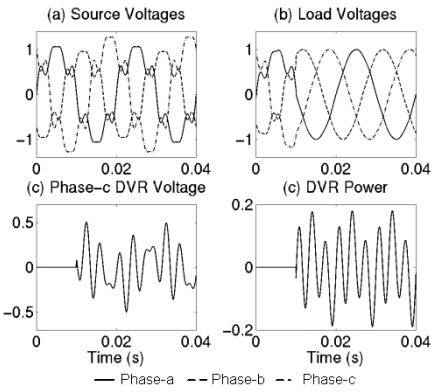

Fig. 8. Performance of DVR under an unbalanced supply condition.

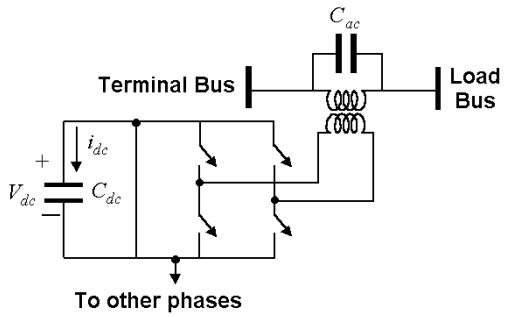

Fig. 9. DVR realization using VSIs and a dc capacitor.

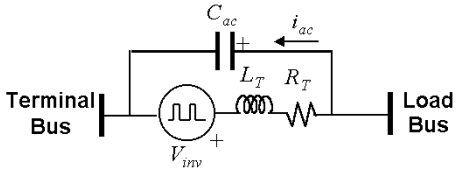

Fig. 10. Single-phase equivalent circuit of DVR.

Let v_f^* be the reference voltage of a phase that has to be tracked and h is a constant. The upper and lower levels of the switching band are then generated from

$$V_{up} = v_f^* + \alpha i_{ac} + h$$
$$V_{dn} = v_f^* + \alpha i_{ac} - h \tag{13}$$

where α is a proportional gain introduced to stabilize the inverter. The switching line is a simplified version of the linear-quadratic-based design in [10]. These near-minimum time controllers have a high-chatter frequency at the target. The hysteresis band (h) has been included to constrain the switching frequency. This combination of switching line with a tolerance band is referred to in this paper as a switching band control.

The inverter in Fig. 9 is capable of supplying V_{dc}, 0, $-V_{dc}$ across the transformer. We refer to these as switch states $+1$, 0, -1, respectively. This three-level switching control is selected according to Table I. For the section where the desired DVR voltage v_f^* is positive, the inverter is switched between 0 and $+1$, while it is switched between 0 and -1 when v_f^* is negative.

TABLE I
THREE-LEVEL SWITCHING SELECTION

Conditions		Switch Value
$v_f^* \geq 0$	$v_f > V_{up}$	0
$v_f^* \geq 0$	$v_f < V_{dn}$	+1
$v_f^* < 0$	$v_f > V_{up}$	-1
$v_f^* < 0$	$v_f < V_{dn}$	0

In addition to the switching band control loop, an additional loop is required to correct the voltage in the dc-storage capacitor against the losses in the inverter and transformer. Furthermore, as evident from Fig. 7(c) and (d), the DVR also has to supply real power during transients. All of this may cause the capacitor voltage to fall. To correct these deviations, a small amount of real power must be drawn from the source to replenish the losses. To accomplish this, we introduce a simple proportional-plus-integral (PI) controller of the form

$$u_c = K_P e + K_I \int e\, dt \tag{14}$$

where $e = V_{ref} - V_{dc}^{av}$, V_{dc}^{av} being the average voltage of the capacitor over a complete cycle. The unit of u_c is radians and steady state is indicative of the losses in the converter. We now modify (2) and (11) such that

$$V_{f1} = |V_{f1}| e^{j(\angle I_s + 90^\circ - u_c)} = |V_{f1}| \left(\tilde{a}_1 + j\tilde{b}_1\right) \tag{15}$$

and the quadratic (11) is modified to

$$|V_{f1}|^2 - 2\tilde{a}_1 |V_l|\, |V_{f1}| + |V_l|^2 - |V_{t1}|^2 = 0. \tag{16}$$

Under this condition, the phase difference between the line current and DVR voltage differs slightly from 90°.

The aim of the DVR is to supply tightly regulated balanced harmonic-free voltage to sensitive loads. There are, however, limits to how much a DVR can achieve. One of these limits is theoretical and the other practical. We shall discuss them next.

A. Theoretical Limit on Achievable Load Voltage

There is a direct relationship between the terminal voltage, power factor of the load, and the maximum possible achievable load voltage. Refer to the quadratic given in (16). Given a value of $|V_{t1}|$ and a target $|V_l|$, (16) will produce two real values of $|V_{f1}|$, provided that the target is feasible. Otherwise, it will produce two complex conjugate roots indicating a lack of a feasible solution. We can then surmise that the maximum achievable value of $|V_l|$ is that for which (16) yields a single solution, that is

$$|V_l| = \frac{|V_{t1}|}{\sqrt{1 - \tilde{a}_1^2}} \tag{17}$$

and the DVR voltage is then given by

$$|V_{f1}| = \tilde{a}_1 |V_l|. \tag{18}$$

With no losses ($u_c = 0$), (17) becomes $|V_l| = |V_{t1}|/\cos\phi_l$.

Example 4: The load and feeder impedances are the same as discussed before. They are supplied by a set of balanced voltages with a peak value of 1 p.u. It is assumed that all system parameters are referred to the feeder side of the transformers. The system parameters, given in per unit, are:

$$X_T = \omega L_T = 0.025, \quad R_T = 0.001\,25,$$
$$Y_{ac} = \omega C_{ac} = 0.25, \quad \text{and} \quad Y_{dc} = \omega C_{dc} = 30.16.$$

The switching band and control parameters are

$$V_{ref} = 0.5 \text{ p.u.}, \quad \alpha = -0.35, \quad h = 0.05$$
$$K_P = 0.5, \quad \text{and} \quad K_I = 5.$$

With these parameters, the switching speed of the VSIs is approximately 4 kHz.

The system operates in steady state for one cycle (20 ms) when the peak of the source voltages is suddenly reduced to 0.6 p.u. As a result, the terminal voltage drops to a level so that it is impossible to regulate the load voltage at 1.0 p.u. To operate the DVR under this condition, the magnitude of maximum possible value of the load voltage is determined from (17) and the DVR voltage is determined from (18).

The system response is shown in Fig. 11 where the terminal voltage and the load voltage are shown in (a) and (b), respectively. The maximum possible load voltage is calculated based on the Fourier extraction of the line current and terminal voltage. As mentioned before, this extraction depends on the half–cycle averaging and this averaging process is continuously running. The load voltage limit, shown in Fig. 11(c), thus varies continuously until the system oscillations die out. It has a value of 1 p.u. before the transient. The dc capacitor response voltage is shown in Fig. 11(d).

B. Practical Limit on Achievable Load Voltage

The practical limit on the target load voltage is usually placed by the storage device. This is best illustrated by the following example.

Example 5: The system parameters are the same as in Example 4. With the system in steady state, the peak of the phase-c of the source voltage suddenly sags to 0.2 p.u. at the end of the first cycle. It, however, is restored to 1.0 p.u. at the end of the third cycle. The system response is shown in Fig. 12. The terminal and load voltages are shown in Fig. 12(a) and (b), respectively. It can be seen that the DVR fails to maintain the load voltage at 1.0 p.u. during the transient. There are two reasons behind this behavior. The first one is due to the reduction in the target load voltage as per (17). The second one is the saturation of the inverter voltage due to the inability of the dc-storage capacitor to supply the required voltage. This is shown in Fig. 12(c), where the desired DVR voltage of phase-c is given by the dashed line and the actual DVR voltage is shown by the solid line. The dc capacitor behavior is shown in Fig. 12(d). It can be seen that capacitor charges momentarily, before discharging, supplying the drop in the faulted phase. If the drop is maintained, the capacitor voltage will be restored to its nominal value with a time constant of 0.15 s.

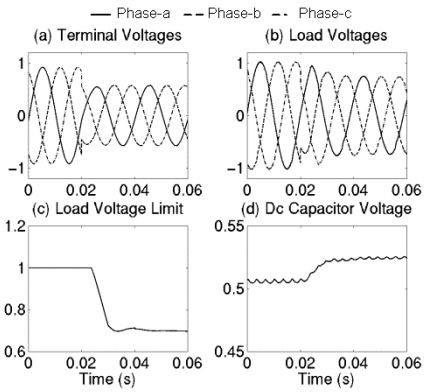

Fig. 11. Performance of DVR when all phases dip.

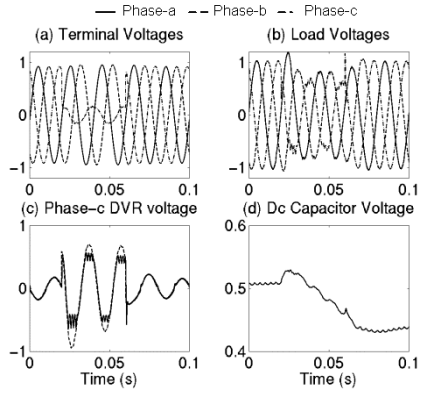

Fig. 12. Performance of DVR when one phase sags.

V. Conclusions

This paper presents a systematic study of a dynamic voltage restorer that can tightly regulate voltage at the load terminals against any variation in the supply-side voltage while consuming no real power in the steady state. The paper demonstrates the capability of the device through steady-state analysis. A number of options to obtain the time-varying DVR reference voltages are proposed. Also, a structure to realize the DVR by VSIs is also discussed. All discussions are supplemented by simulation results using MATLAB. From the studies presented in the paper, it can be safely concluded that a DVR is a voltage regulator, voltage restorer, and voltage conditioner—all in one.

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