Hysteresis Current Control Operation of Flying Capacitor Multilevel Inverter and Its Application in Shunt Compensation of Distribution Systems

Anshuman Shukla, *Student Member, IEEE*, Arindam Ghosh, *Fellow, IEEE*, and Avinash Joshi

***Abstract*—Flying capacitor multilevel inverter (FCMLI) is a multiple voltage level inverter topology intended for high voltage and power operations with low distortion. It uses capacitors, called flying capacitors for clamping the voltage across the power semiconductor devices. In this paper, the implementation of a distribution static compensator (DSTATCOM) using an FCMLI is presented. A hysteresis current control technique for controlling the injected current by the FCMLI-based DSTATCOM is discussed. A new method for controlling the flying capacitor voltages is proposed which ensures that their voltages remain constant and at the same time maintain the desired current profile under the hysteresis current control operation. Simulation studies are performed using PSCAD/EMTDC to validate the efficacy of the control scheme and the FCMLI-based DSTATCOM.**

***Index Terms*—Distribution static compensator (DSTATCOM), flying capacitor multilevel inverter (FCMLI), hysteresis, voltage-source converter (VSC).**

I. Introduction

TO COMPENSATE distribution systems, various power electronics-based devices called custom power devices have been proposed in the literature [1]–[3]. A distribution static compensator (DSTATCOM) is a voltage-source-converter (VSC)-based custom-power device connected in shunt to the distribution network [1]. For high-voltage distribution networks, the conventional DSTATCOM structures are designed on the basis of simple two-level VSC and use transformer to meet the desired voltage profile. In some cases, in order to achieve higher power level, VSCs are connected in parallel to the dc bus [2]. This type of connection requires a transformer with multiple secondary windings, increasing the cost and complexity of the power topology. Further, the transformer adds to the losses in the system and it may saturate once the load draws any dc current [1], [3]. Also, at high power, the long tail current associated with the device characteristics prohibits high switching frequency operation at a high power and the efficiency of the compensator is lower due to significant switching losses. Therefore, the compensator control in high power applications faces difficulties.

Alternatively, the DSTATCOM may be constructed using the multilevel VSC topologies. In a multilevel inverter, the number of possible operating states increases and as a consequence, the flexibility of the inverter improves. As all the devices are individually controlled, better control over voltage magnitude and harmonic suppression can be achieved. Use of a multilevel inverter reduces the required transformer voltage ratio and sometimes even makes possible direct connection of the compensator to the increased voltage supply systems.

The multilevel converter topologies are attractive for continuous control of system dynamic behavior and to reduce power quality problems such as voltage harmonics, voltage imbalance or sag and have better properties under sudden changes of loads. Further, they have similar dynamic properties as two level converters with comparable switching frequencies. Hence, these are suitable for flexible ac transmission system (FACTS), high-voltage custom power applications and for distributed power systems [4]–[6].

Three different multilevel inverter topologies are considered currently. These are 1) diode-clamped multilevel inverter (DCMLI); 2) cascade H-bridge inverter; and 3) flying capacitor multilevel inverter (FCMLI). A number of papers are available in the literature, which compare the three multilevel inverter topologies for FACTS applications [4]–[10]. FCMLI offers many advantages over the DCMLI structure as it does not need clamping diodes, does not suffer from dc-link voltage unbalancing problems, directly clamp the voltage across the switches, etc., unlike DCMLI [4], [6]. For operations above three level, the use of FCMLI becomes more rewarding as compared to that of DCMLI [7]. The cascade inverter topology has been main area of research for the shunt compensator applications in the transmission system [7]–[12]. In the shunt compensator applications, a transformer is necessary to connect the cascade inverter structure to the transmission or distribution systems, once a single dc-link capacitor is used for all the three phases [9]. For distribution systems, the transformer may not be required in some cases as the multilevel inverter itself may be capable of achieving the desired voltage level. Also, for the distribution systems having dc loads, it is not recommended to use interconnecting transformer for the reasons discussed above. Therefore, for such applications, using cascade H-bridge inverter with the said construction is not very well justified. The other method may be to use separate cascade inverter structure with separate dc-link capacitors for each phase without using a transformer. This arrangement however needs a very complex dc-link voltage regulation loop and its complexity will increase

Manuscript received May 25, 2005; revised November 15, 2005. Paper no. TPWRD-00307–2005.

The authors are with the Department of Electrical Engineering, Indian Institute of Technology, Kanpur 208 016, India (e-mail: aghosh@iitk.ac.in).

Digital Object Identifier 10.1109/TPWRD.2006.877100

with the increase in the number of H-bridge modules [5]. Further, connecting separate dc sources between two converters in a back-to-back arrangement (e.g., in UPFC, UPQC) is not possible because a short-circuit will be introduced when two back-to-back converters are not switching synchronously [8]. In addition, for reactive power exchange, the power pulsation at twice the output frequency occurring with the dc-link of each H-bridge inverter necessitates over-sizing of the dc-link capacitors [4]–[11]. On the other hand, an FCMLI requires the simplest dc-link voltage regulation loop as compared to the other multilevel inverters [7]. Further, it does not need a number of isolated power supplies as required in cascade H-bridge arrangements. Its dc-link capacitor control loop is as simple as in the conventional two-level inverter and is independent of the number of output voltage levels [4]–[6]. The main limitations of FCMLI are requirement of large number of capacitors and their efficient control. However, for the DSTATCOM applications, it may be a promising candidate if the flying capacitor voltage control is efficiently achieved because of its simpler dc-link construction. This is also because, it does not need an interconnecting transformer if its output voltage profile is sufficient enough to meet the desired voltage profile at the distribution bus. In this paper, the FCMLI topology has been investigated for DSTATCOM applications. Few methods such as one in [6] have been proposed to efficiently control the flying capacitor voltages in the context of output voltage control of the inverter. However, almost no focus has been given on the current control aspect and corresponding flying capacitor voltage control techniques in FCMLI except the one in [14] which, however, suffers from few limitations discussed in Section II.

A VSC needs to be current controlled for the DSTATCOM applications. Modulation control of a multilevel inverter is usually achieved using open loop PWM strategies, which are well established with the merits of various alternatives well reported. These strategies can be readily used with a synchronous frame PI regulator or a deadbeat regulation strategy to create a current regulated multilevel system in much the same way that a two-level inverter can be current regulated [15]. An alternative way to regulate current through a multilevel inverter is to use hysteresis comparison to determine the switching instants. As with all hysteresis systems, this approach would be expected to have a fast dynamic response and a continuously spread harmonic spectrum. This control has been widely used to control the conventional two-level VSC, showing its robustness and simplicity in a lot of applications [15], [16].

This paper proposes the design of a five-level FCMLI-based DSTATCOM in the hysteresis current control mode. A hysteresis current control operation has been derived for the FCMLI, which ensures that the flying capacitor voltages remain constant and at the same time the controlled line current follows its reference value. The DSTATCOM is applied to a three-phase four-wire distribution network to compensate for the harmonics caused by unbalance and nonlinearity in the load.

II. Hysteresis Current Control of Flying Capacitor Multilevel Inverter

Hysteresis current control technique of a two-level inverter is well established. For multilevel inverters, as n-levels of output

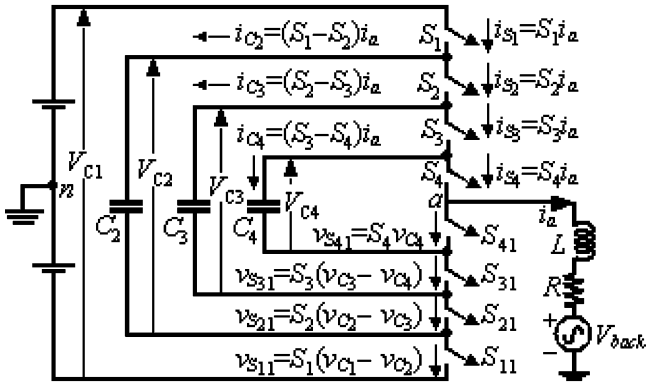

Fig. 1. One phase leg of a five-level flying capacitor inverter.

voltage are available, the task is to select a particular voltage level output to force the current error to zero once it exceeds certain limits. The hysteresis control techniques available in the literature for multilevel inverters have focused mainly on DCMLI and cascaded inverters [15]–[19]. Further, these techniques mainly discuss only three-level inverter structures. For the transformerless shunt compensator application considered here, higher-level inverter structure may be required to meet the desired voltage profile at the distribution bus. There are many other advantages of applying higher-level inverter also, however, at the cost of increase in complexity [4]–[10]. Therefore, in this paper, a five-level flying capacitor inverter has been considered. Fig. 1 shows the schematic diagram of one leg of a three-phase five-level FCMLI. $V_{\rm C1}$ is the dc link of the inverter and C_2, C_3, and C_4 are flying capacitors, which are regulated using a control scheme at $3V_{\rm dc}/4$, $V_{\rm dc}/2$, and $V_{\rm dc}/4$, respectively, for $V_{\rm C1} = V_{\rm dc}$. These capacitors clamp the voltage stresses across the power semiconductor devices (e.g., S_1, S_2, etc.) at $V_{\rm dc}/4$. The expressions for the currents i_{S1} through i_{S4} and i_{C2} through i_{C4} and the device voltages (v_{S11}, etc.) in Fig. 1 use the binary variables S_1 through S_4. These will attain the value 1, if the corresponding switch is closed and 0 otherwise. Table I lists the switch combinations used to synthesize the output phase voltage V_{an} with respect to n. The states "1" and "0" indicate the corresponding switch is ON and OFF, respectively. Table I also indicates the states of the flying capacitors corresponding to the switch combinations chosen. Charging of a capacitor is indicated by $+$, discharging by $-$, while "NC" indicates neither charging nor discharging. The switch states given are for the positive direction of the current waveform (indicated as outgoing current i_a in Fig. 1). The capacitor states ($+$ and $-$) will reverse for the negative current. The detailed operation and structure details of the FCMLI can be found in [4], [6]–[8].

A. Current Control

The output voltage of the inverter V_{an} can be related to the parameters of simple $R-L$ load components (Fig. 1) as follows:

$$V_{an} = Ri_a + L\frac{di_a}{dt} + V_{\rm back} \tag{1}$$

where $V_{an} = nV_{\rm dc}$ ($n = 1/2$, 1/4, 0, $-1/4$ and $-1/2$, as a five-level inverter may select between voltage levels $V_{\rm dc}/2$, $V_{\rm dc}/4$, 0, $-V_{\rm dc}/4$ and $-V_{\rm dc}/2$ for $V_{\rm C1} = V_{\rm dc}$), i_a is the load

TABLE I
SWITCHING SCHEME FOR ONE-PHASE LEG OF A FIVE-LEVEL FCMLI

S_1	S_2	S_3	S_4	S_{41}	S_{31}	S_{21}	S_{11}	C_2	C_3	C_4	V_{an}
1	1	1	1	0	0	0	0	NC	NC	NC	$+V_{dc}/2$
1	1	1	0	1	0	0	0	NC	NC	+	$+V_{dc}/4$
1	1	0	1	0	1	0	0	NC	+	–	
1	0	1	1	0	0	1	0	+	–	NC	
0	1	1	1	0	0	0	1	–	NC	NC	
0	0	1	1	0	0	1	1	NC	–	NC	0
0	1	0	1	0	1	0	1	–	+	–	
0	1	1	0	1	0	0	1	–	NC	+	
1	0	0	1	0	1	1	0	+	NC	–	
1	0	1	0	1	0	1	0	+	–	+	
1	1	0	0	1	1	0	0	NC	+	NC	
1	0	0	0	1	1	1	0	+	NC	NC	$-V_{dc}/4$
0	1	0	0	1	1	0	1	–	+	NC	
0	0	1	0	1	0	1	1	NC	–	+	
0	0	0	1	0	1	1	1	NC	NC	–	
0	0	0	0	1	1	1	1	NC	NC	NC	$-V_{dc}/2$

current, L and R are the load inductance and resistance, respectively, and $V_{\rm back}$ is the back emf voltage. As V_{back} increases or as larger reference slopes are required, larger average values of V_{an} need to be used. Since the voltage across the load resistance is often small, this value can often be neglected. Introducing a term $di_{\rm ref}/dt$, (where $i_{\rm ref}$ is the reference current to be tracked using the hysteresis current control)(1) becomes

$$\frac{d(i_a - i_{\rm ref})}{dt} \approx \frac{V_{an} - V_{\rm back}}{L} - \frac{di_{\rm ref}}{dt}. \tag{2}$$

There are few hysteresis current control methods available in the literature for multilevel inverters [17]–[19]. A method discussed in [17], requires $n-1$ number of offset bands for an n-level inverter. The current error is compared with the bands and the output voltage level is changed one after another each time the error crosses the bands. The main limitation of this scheme is that a positive or negative tracking error is introduced into the average output current [18].

A time-based approach has been proposed in [18] to control the current error of a three-level inverter with the advantage that, no dc-tracking error is introduced in the average output current. It was proposed that the current error could be controlled in a single band ("B") in general, by selecting the output voltage levels one after another. An outer hysteresis band ("B_1") was introduced optionally to allow switching to the extreme voltage levels for rapid current error detection during transient conditions. However, this proposition is true only for a three-level inverter and it needs to be modified for higher level inverters. To verify this, we refer to Fig. 2, which represents the current error control using this method for a five-level inverter.

For a three-level inverter, at the innermost band limit, (say at "L" in Fig. 2), if the output voltage is "0" and if it is insufficient to force the current error in the opposite direction, then at "M," the extreme voltage level output $+V_{\rm dc}/2$ will be selected, which is the maximum this inverter can do to change the current error direction. In this way, the current error is confined within the band "B." However, this is not the case for a five-level inverter, which can be seen from Fig. 2. At "M," the output voltage level is "0" and suppose it is insufficient to reverse the current error

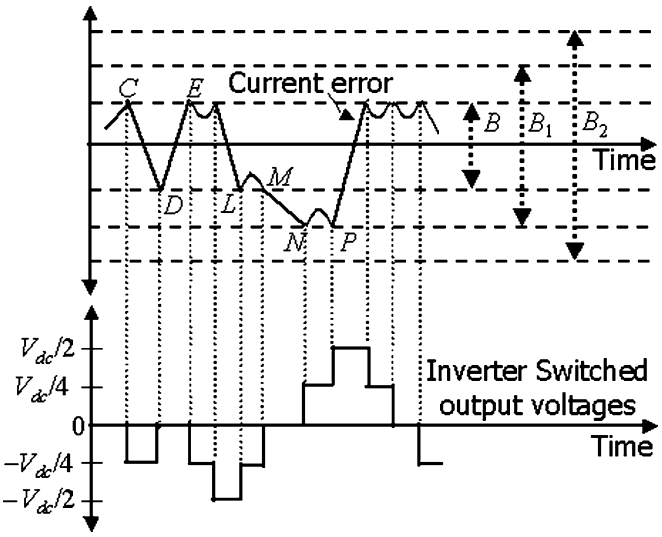

Fig. 2. Hysteresis current control of a five-level inverter.

direction. Then, it will cross "B" with a different slope, as the voltage level acting on it is now "0." In case of only one band "B," the extreme output voltage level $+V_{\rm dc}/2$ will be applied at "N." The transition of the voltage level in this case will be from 0 to $+V_{\rm dc}/2$ (i.e., by two levels). This will deteriorate the output voltage waveform and the advantages of the multilevel inverters will be lost. Now, after introducing an extra band, the voltage level transition is like that as shown in Fig. 2, where at "N," the next voltage level $+V_{\rm dc}/4$ is applied and since it is insufficient to force the current error in opposite direction, the next voltage level $+V_{\rm dc}/2$ is applied at "P." As can be seen, by introducing an extra band, the uniformity in change in output voltage states occurs. Therefore, two bands are required to track the current using this method for a five-level inverter and this number will increase with output voltage levels. An extra band B_2 may be introduced optionally for the purpose, discussed earlier. The size of the main band "B" is largely determined by the permitted level of current distortion. The other determining factors are load value, input voltage, and desired switching frequency. The second set of switching bands (B_1, B_2) has different zones in order to provide a reliable and robust control for an n-level inverter. The time error as discussed in [18] can also be applied to this hysteresis current control to optimize the level change of the current controller.

B. Flying Capacitor Voltage Control

Flying capacitor voltage balancing under the hysteresis current control operation can be achieved using the redundant switch combinations available for different voltage level outputs (Table I). A flying capacitor voltage balancing scheme for only one flying capacitor and having two-switch pairs per leg in hysteresis control application was discussed in [14]. This control measures the capacitor voltage states and the current error to select a proper switch combination each time the controlled current crosses any of the defined bands. However, in this scheme, the capacitor voltage variations depend on the hysteresis bands and load parameters, as detailed in the next section. In the present paper, a five-level inverter (Fig. 1) having

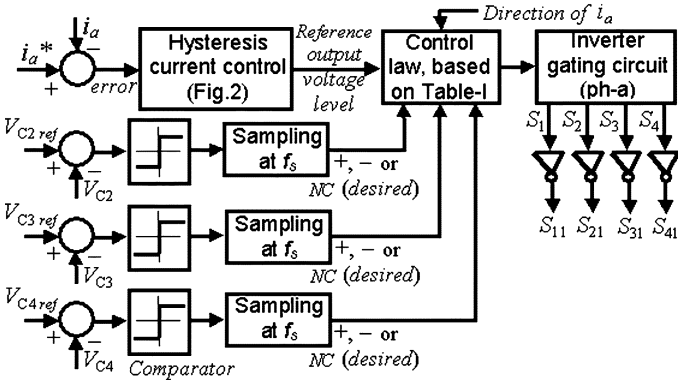

Fig. 3 Control block diagram for one phase of a five-level FCMLI.

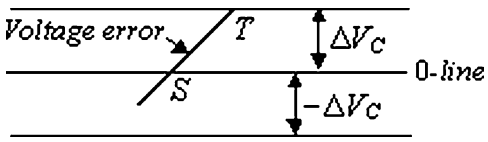

Fig. 4. Flying capacitor voltage error tolerance prediction.

three flying capacitors per phase has been considered. Therefore, the control task is more complex as at each switching instant the decision should be made such that all the three flying capacitor voltages remain balanced and at the same time the output current tracks the reference.

1) Proposed Control Strategy: A flying capacitor voltage balancing technique is proposed in this paper, which offers better operating performances as compared to those available in the literature. Fig. 3 is the block diagram representation of the proposed technique for one phase of the inverter. Similar control actions are needed for the other phases.

In the proposed approach, the current error is passed through hysteresis comparators to decide which output voltage level is required at a particular instant (Fig. 2). Also, each error between the actual flying capacitor voltages (V_{C2}, V_{C3}, and V_{C4}) and their corresponding reference values (denoted as $V_{\rm C2ref}$, $V_{\rm C3ref}$, and $V_{\rm C4ref}$ in Fig. 3) are passed through a zero-band comparator, individually. (Note that $V_{\rm C2ref} = 3V_{C1}/4$, $V_{\rm C3ref} = V_{C1}/2$, and $V_{\rm C4ref} = V_{C1}/4$, with reference to Fig. 1). The output of each comparator is judged at a constant sampling frequency (f_s, in Fig. 3). At a particular sampling instant if the flying capacitor voltage error is positive, then that particular capacitor is required to be discharged, if it is negative, then charging is required and if the error is zero, then no change in the flying capacitor voltage is required. Therefore, the desired operation for each flying capacitor is set. Now, based on the desired output voltage level, the direction of the current and the desired flying capacitor voltage operations at a particular instant, a particular switch combination is chosen from Table I so that it could result in the desired output current and flying capacitor voltages. As for example, suppose the current error lies between points D and E (Fig. 2) and the required output voltage level is 0, which has six switch states (Table I). If the time taken by the current error to go from D to E is larger than $2\times(1/f_s)$, then multiple samplings can be made between D and E at the rate of f_s. In between theses points, if at a particular sampling instant, the situation is such that C_2 is charging, C_3 is discharging, and C_4 is charging, then the switch combination chosen will be S_1-OFF, S_2-ON, S_3-OFF and S_4-ON. This action will lead to discharge C_2 and C_4 and will charge C_3 (Table I). The next switch combination at the next switching instant will be accordingly chosen so that it leads to the most favorable situation with balanced flying capacitor voltages. In similar manners, for the output voltage levels $\pm V_{\rm dc}/4$, there are four switch combinations each as given in Table I, which can be accordingly chosen for these output voltage levels to force the capacitor voltage error to zero. As each flying capacitor has an equal number of charging and discharging operations for the output voltage levels 0 and $\pm V_{\rm dc}/4$, balancing their voltages can be achieved. There may be the case when not all the capacitors are involved in a particular switch combination, as is evident from Table I (denoted as NC). In that case, that particular combination will be chosen which offers most favorable situation for the flying capacitors. For example, suppose for the output voltage level "0," the requirements are to discharge C_2 and C_3 and charge C_4. As Table I does not suggest any such switch combination that can perform all of these operations, the most favorable switch combination is selected. The most favorable switch combination is S_1-OFF, S_2-ON, S_3-ON and S_4-OFF, as it involves desired operation involving two flying capacitors, while the switch combination S_1-OFF, S_2-OFF, S_3-ON and S_4-ON, involves only one. In this manner, by using this strategy the flying capacitor voltages are regulated around their reference values.

2) Choice of the Sampling Frequency: As is shown in Fig. 3, the capacitor voltage errors are compared in a zero band comparator and are sampled at a sampling frequency of f_s. By defining a fixed f_s, the maximum tolerance in the capacitor voltages can be defined, which can be understood from the following discussion. Fig. 4 shows a flying capacitor voltage error variation. Suppose at a particular instant, the flying capacitor C is in the discharging mode and so its voltage error is increasing in the positive direction (along the path $S-T$ in Fig. 4). Before the point S, the voltage error was below the zero line and therefore, the desired capacitor operation was "discharging." After point S, since the error is positive, the capacitor is required to be charged. Suppose the last sampling instant was at S or just before it. Now, after time $T_s = 1/f_s$, the sampling is done at T. Suppose the current, which is flowing through the capacitor, has a peak value of i. This current is the same, which is flowing at the output of the inverter (i_a in Fig. 1). Therefore, we can take the peak of i_a as i. The voltage of the capacitor is V_C at S and has decreased down to $V_C - \Delta V_C$ at T. Let the time instants at S be 0 and at T, it is T_s. Therefore, for the peak current i, we have the following relations:

$$i\int_0^t dt = -C\int_{V_C}^{V_C-\Delta V_C} dV_C, \quad \Delta V_C = \frac{iT_s}{C}, \quad T_s = \frac{1}{f_s}. \tag{3}$$

In (3), as we know i, C and have set T_s, we can predict ΔV_C. Since i is taken as the peak of the output current, ΔV_C is the maximum voltage tolerance. Therefore, we can design the control for a maximum capacitor voltage variation by setting T_s

TABLE II
FIVE-LEVEL INVERTER PARAMETERS

Number of main switches	24
Device ON resistance	0.01 Ω
Device OFF resistance	1.0E6 Ω
Forward voltage drop	0.0 kV
Forward breakover voltage	1.0 kV
Reverse withstand voltage	1.0 kV
Snubber resistance	500.0 Ω
Snubber capacitance	25 μF

and knowing the values of C and i. i can be determined from the rating of the inverter or the compensator.

In the proposed approach, as a fixed f_s is defined, even if the load or dc-link parameters are such that the current error remains in a particular band for a longer time, the control action keeps on changing the switching states as and when required depending on the capacitor voltage states. Therefore, by using this approach, the flying capacitor voltage variations can be made almost independent of the load parameters and the dc-link voltage. This approach also offers full utilization of the redundant switching states available. The lower values of T_s and C may result in a higher switching frequency. However, it can be reduced by taking a larger value of either of T_s or C or of both. Another way of reducing the switching frequency is by introducing a hysteresis comparator in place of the zero-band comparator (Fig. 3). Therefore, the allowed switching frequency can be set by optimally setting the capacitance of the flying capacitors, the sampling frequency, and the band comparator. The detailed description about the switching frequency reduction will be given in the next section.

III. HYSTERESIS CURRENT-CONTROLLED FCMLI SIMULATION RESULTS

A five-level FCMLI is simulated using the PSCAD/EMTDC simulation package. The inverter is supplying a balanced three-phase star-connected RL-load with $R = 0.5\ \Omega$ and $L = 0.1$ H. The back emf voltage [$V_{\rm back}$, (1)] is taken to be zero here. The five-level inverter parameters are given in Table II. The inverter devices are taken nearly ideal in this simulation. The capacitances of the flying capacitors are taken as $C_4 = 300\ \mu$F, $C_3 = 150\ \mu$F, and $C_2 = 100\ \mu$F (Fig. 1), in each phase. The dc-link voltage is 4000 V. Phase-a, b, and c currents are controlled to follow the sinusoidal references having peak-to-peak values of ±50 A, ±60 A, and ±40 A, respectively. The hysteresis current control method discussed earlier in Section II-A has been applied here to the three-phase five-level FCMLI under consideration. As mentioned earlier, three boundaries are taken each above and below the zero crossing for checking the current error. Same widths of the hysteresis bands are taken for the three line currents to be tracked. The width of the outermost hysteresis band (B_2 in Fig. 2) is taken as 2% of the peak of the phase-b reference current (i.e., 2% of 60 A). For simplicity, the bands are taken equidistant from each other. However, the widths of the hysteresis bands may be set using the design considerations discussed earlier in Section II-A.

Figs. 5–7 show the inverter performances operating under the considered conditions. Fig. 5 shows the phase-a current error

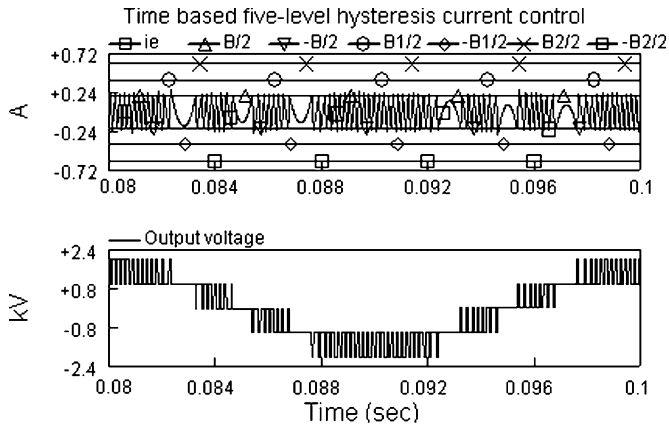

Fig. 5. Five-level FCMLI hysteresis current control.

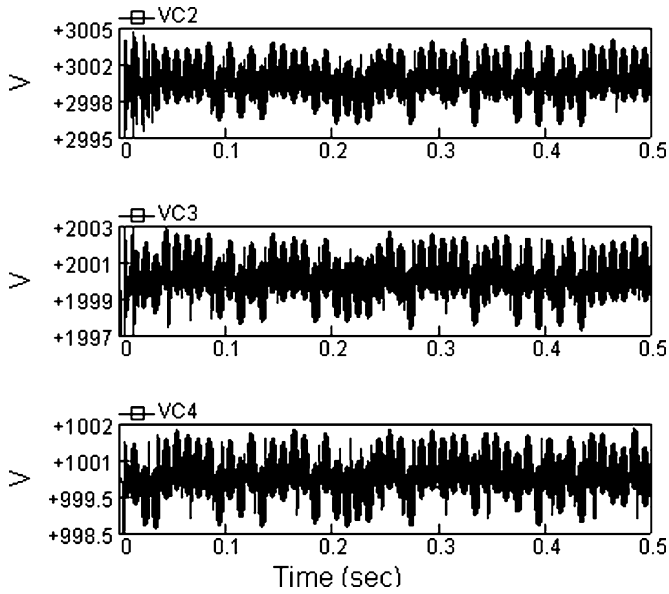

Fig. 6. Phase-a flying capacitor voltages.

variation across the allotted bands and phase-a output voltage. The THDs of the resulting line-a, b, and c currents are 0.11%, 0.06%, and 0.16%, respectively, and of the output phase-a, b, and c voltages are 2.0%, 0.94%, and 3.2%, respectively. For larger widths of the hysteresis bands, the THDs of the currents and voltages will be higher. As can be seen, the current error is contained within the defined bands as described earlier and each current error direction or slope change produces a new output voltage level, different from the previous one. In this way, a five-level output voltage waveform composed of voltage levels $V_{\rm dc}/2$, $V_{\rm dc}/4$, 0, $-V_{\rm dc}/4$, and $-V_{\rm dc}/2$ is obtained for a sinusoidal reference current. This implies that the control algorithm is able to keep the requested discrete voltage levels.

The performance of the flying capacitor voltage control scheme proposed above is evident from Figs. 6 and 7. It can be seen that the clamping leg voltages have been tightly regulated around their reference values [i.e., 1000 V ($V_{\rm dc}/4$), 2000 V ($V_{\rm dc}/2$), and 3000 V ($3V_{\rm dc}/4$)] as expected. The errors between the reference and actual capacitor voltages are compared in a zero-band comparator (Fig. 3) and are sampled at a constant rate of 10 μs ($1/f_s$, Fig. 3). For this sampling frequency and for the inverter parameters given, we can calculate the maximum

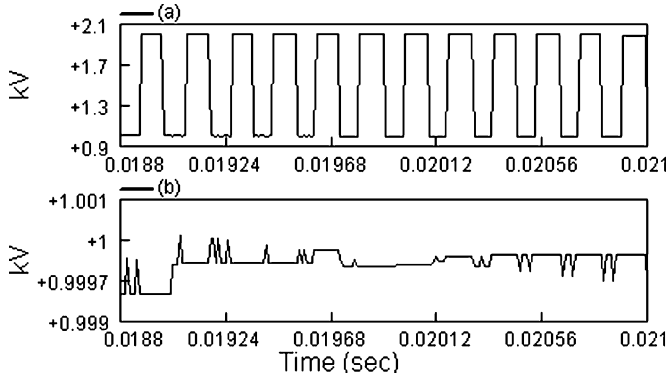

Fig. 7. Phase-a output voltage and innermost flying capacitor voltage. (a) Output voltage; (b) VC4.

voltage tolerance for each of the flying capacitors by using (3). For example, for C_4 in phase-a (Fig. 1), the maximum voltage tolerance is calculated to be 1.667 V, which is 0.1167% of its reference voltage. Similarly, for C_3 and C_2, the maximum voltage tolerances are 3.333 V and 5 V, respectively. These tolerances and the performance of the voltage control method can be justified from Fig. 6, which shows the flying capacitor voltages of phase-a.

Fig. 7 show the output phase-a voltage and one of the flying capacitor's (C_4) corresponding voltage variations for a small time duration. It is evident that for a particular time duration in which the output voltage level is $V_{\rm dc}/4$, multiple charging or discharging operations of C_4 occur, corresponding to whether its voltage is less or more than the reference. This is for the cases in which the duration of the output voltage level $V_{\rm dc}/4$ is equal to or more than 2×10 μs (Section II-B). The charging, discharging, or no change of the capacitor is done by selecting the most favorable switch combination from Table I, each time at the interval of 10 μs for a particular output voltage level. It is also seen from Fig. 7 that for the output voltage level $V_{\rm dc}/2$, V_{C4} remains constant, as this output voltage level does not consist of change in any flying capacitor voltages (Table I). The same phenomenon, such as that shown in Fig. 6(b), occurs with all of the flying capacitors in each phase and, in this way, flying capacitor voltages are controlled.

Here, in the simulation study, small capacitances of the flying capacitors have been taken, the flying capacitor voltage errors have been regulated around zero band and, also, T_s has been taken too small resulting in a maximum switching frequency of around 11.5 kHz. We also kept the flying capacitor voltage variations too low (less than 0.2%). For $T_s = 50$ μs and having other system conditions the same as above, another simulation study is performed. The switching frequency in this case has been reduced down to around 5.2 kHz, without almost unaffecting the quality of inverter output currents and voltages (as these are mostly affected by hysteresis bands, which are the same here as used previously). However, the flying capacitor voltage variations are now less than or around 0.8%, which can also be justified from (3). For $T_s = 100$ μs, the flying capacitor voltage variations are less than or around 1.5%, while the switching frequency is now 2.7 kHz. Since at these higher values of T_s the capacitor voltage tolerance is not very large and also the switching frequency is achievable, realization of this control structure is possible. The switching frequency can be further reduced by increasing the capacitances of the flying capacitors, for a particular i, T_s and ΔV_C (3). In the case considered above, at most of the sampling instants of the flying capacitor voltage errors, the switching decisions have to be made, as the error is compared with zero, resulting in higher switching frequency. However, the switching frequency can be further reduced by adding a certain allowable non-zero band in the comparators (Fig. 3).

In the case of the proposed approach, the controlled current is of best quality as compared to that in other cases such as in [16]–[18], for same total widths of the hysteresis bands. This is because the current error is forced to remain in the minimum width (Fig. 2). For the same hysteresis bands, however, it seems that the switching frequency is more in the present case. This however is not true for the FCMLI using the proposed flying capacitor voltage balancing scheme. This is because, in the proposed scheme, the switching frequency is almost totally determined by the f_s signal, indicated in Fig. 3. Due to the current error variation in a smaller band, the "apparent" switching frequency is increased for the case in Fig. 2 and hence, its output voltage quality is best as compared to that of others. In this way, the method corresponding to Fig. 2 is best as compared to the other methods for the FCMLI.

In applying the hysteresis current control operation to the FCMLI, few things should be taken into consideration. If the sampling time ($1/f_s$, Fig. 3) is taken too large or if the capacitances are small, then the flying capacitor voltage variation may exceed the allowable limit and it may deteriorate the output voltage waveform. This phenomenon can be understood from Fig. 8, where the hysteresis current control method discussed earlier has been studied. The difference here is that now, the capacitor voltage error measurements are done only at the instants when the current error crosses the allotted boundaries. This practically means that the sampler blocks in Fig. 3 are absent. The rest of the operating conditions are same as considered earlier. We refer to Fig. 2 for discussing the effect. The flying capacitors voltages are checked at the points L, M, N, P, etc. Let us consider the current error variation from M to N. The output voltage during this instant is '0', which has six possible switching states (Table I). Suppose at M, when a particular flying capacitor voltage is measured, it is required to be charged to follow its reference value. To do so, the controller selects a particular switch combination, which does this desired operation and also performs the desired charging, discharging or NC (Table I)of the other two flying capacitors in that particular phase. Considering the flying capacitor state from M to N, it will keep on charging in this interval. If this interval is too large, it will deteriorate the output voltage waveform. This is because, the combined flying capacitor voltages will significantly add or subtract to the dc-link voltage depending on the current path and will therefore affect the output voltage waveform. Fig. 8 shows the effect, where only V_{C4} is shown under the considered case. Its large variations, in addition to the variations in the voltages of other flying capacitors greatly reduce the quality of the output voltage waveform. The charging or discharging of flying capacitors for long time also changes V_{an} in (1) and (2) for a particular voltage level output and depending on the number of flying capacitors involved in generation of this

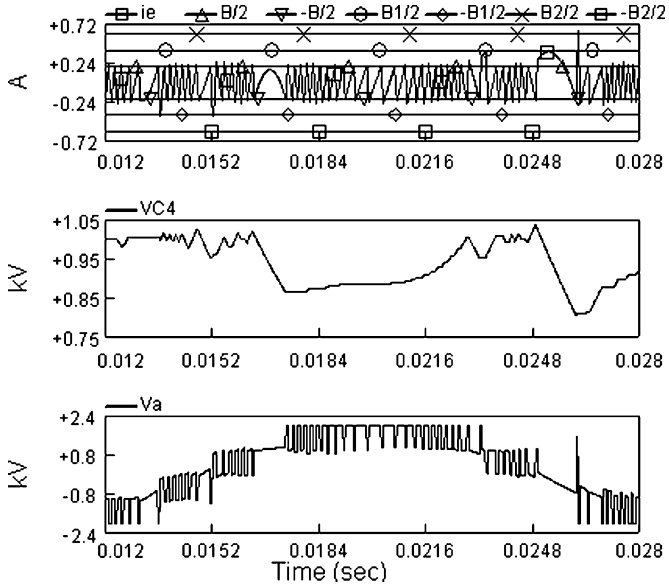

Fig. 8. Five-level hysteresis current control with sampler block absent.

voltage level. This also results in bad quality of controlled current, which can be judged from Figs. 5 and 8, where current error variations have been shown. In Fig. 5, since the flying capacitor voltages are closely held at their corresponding reference values, output voltage waveform is as desired. However, since in Fig. 8, the resulting output voltage gets distorted due to very large variations in the flying capacitor voltages, the current error variations are also accordingly affected [(1), (2)].

Based on the observations made above, it is concluded that T_s should be small enough and capacitance of the flying capacitors should be large enough to have an allowable maximum voltage variations and hence better qualities of the output voltage and current at an allowable switching frequency.

IV. FCMLI-Based DSTATCOM

The DSTATCOM is a shunt compensator, usually operated to balance the source current i_s, by injecting a current i_f to cancel the harmonic component in the load current i_l. For this we assume that the source voltages are balanced sinusoids in this paper. The detailed structure and operation of the DSTATCOM can be found in [1], [3]. The schematic diagram of the DSTATCOM compensated three-phase, four-wire (3p4w) distribution system under consideration is shown in Fig. 9. The dc link of the DSTATCOM contains two capacitors, whose midpoint is connected to the load neutral. It is assumed that the inverter provides sufficient voltage level to eliminate the need of connecting transformers. In Fig. 9, the voltage source, the load, and the DSTATCOM are connected at the point of common coupling (PCC) of the supply and the load. The reference current generation algorithm for the DSTATCOM given in [16] has been used here to achieve the following tasks.

- The load current harmonics do not appear in the source side (active filtering).
- The source current is in phase with the terminal voltage (upf operation).
- The source currents are balanced even when the load is not (load balancing).

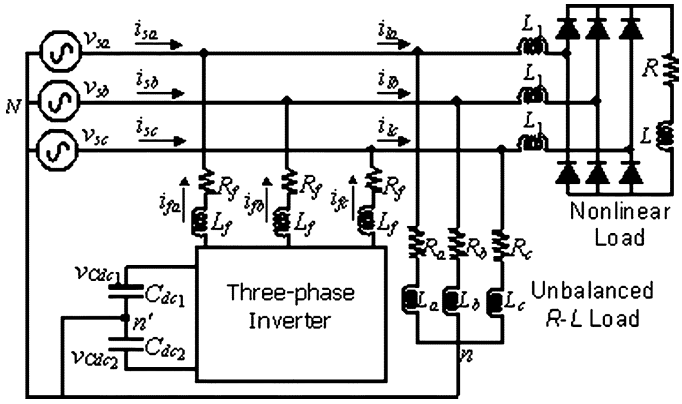

Fig. 9. Single-line diagram of a DSTATCOM connected to a 3p4w system.

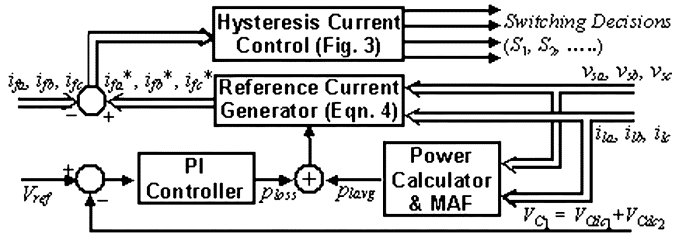

Fig. 10. Control scheme for the FCMLI operating as a DSTATCOM.

The control scheme for the FCMLI operating as a current source is shown in Fig. 10. The inverter is operated in the hysteresis band current control (Fig. 2) to track the reference currents i^*_{fa}, i^*_{fb}, i^*_{fc} in phases a, b, and c, respectively. The reference currents are generated on the basis of theory of instantaneous symmetrical components and are given by [16]

$$\begin{aligned} i^*_{fa} &= i_{la} - \frac{v_{sa} + \beta(v_{sb} - v_{sc})}{\sum_{i=a,b,c} v^2_{si}}(p_{\text{lavg}} + p_{\text{loss}}) \\ i^*_{fb} &= i_{lb} - \frac{v_{sb} + \beta(v_{sc} - v_{sa})}{\sum_{i=a,b,c} v^2_{si}}(p_{\text{lavg}} + p_{\text{loss}}) \\ i^*_{fc} &= i_{lc} - \frac{v_{sc} + \beta(v_{sa} - v_{sb})}{\sum_{i=a,b,c} v^2_{si}}(p_{\text{lavg}} + p_{\text{loss}}). \end{aligned} \tag{4}$$

In (4), $\beta = tan\varphi/\sqrt{3}$, where φ is the desired phase angle between the source voltage and current. Note that, for upf, $\varphi = 0$ and, therefore, $\beta = 0$. The term p_{lavg} is the average power consumed by the load and is computed using a moving average filter (MAF) that has an averaging time of half a cycle. The term p_{loss} accounts for the losses in the inverter and is the power drawn from the ac system to hold the dc bus voltage constant. To generate p_{loss}, a feedback loop is used (Fig. 10), which regulates the dc bus voltage using a PI controller as

$$p_{\text{loss}} = K_p e + K_I \int e dt. \tag{5}$$

In (5), $e = V_{\text{ref}} - V^{cyc}_{\text{dc}}$, where V^{cyc}_{dc} is the cycle-by-cycle average of $v_{Cdc1} + v_{Cdc2}$.

Now the simulation study of a DSTATCOM based on a 5-level FCMLI is presented. For the system under considera-

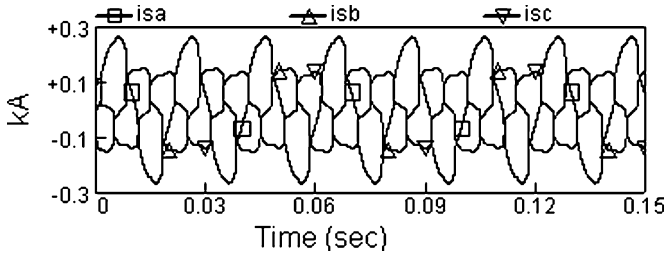

Fig. 11. Source currents in the uncompensated mode.

tion, the term V_{back} as given in (1), will be the PCC voltage, which is the same as the source voltage. The system under study has a balanced 3-phase source having line-to-line rms voltage of 11.0 kV with a fundamental system frequency of 50 Hz. It supplies an unbalanced RL load of $R_a = 50\ \Omega$, $L_a = 0.07$ H in phase-a, $R_b = 170.0\ \Omega$, $L_b = 0.1$ H in phase-b and $R_c = 220.0\ \Omega$, $L_c = 0.4$ H in phase-c. In addition, a three-phase uncontrolled rectifier is also connected to the load bus through an inductance of 0.5 mH in each phase, causing the nonlinearity in the load (Fig. 9). With reference to Fig. 9, $R = 150\ \Omega$, $L = 0.04$ H, $L_f = 0.05$ H, $R_f = 0.5\ \Omega$ and $C_{\rm dc1}$, $C_{\rm dc2} = 500\ \mu$F. The capacitances of the flying capacitors are $C_4 = 90\ \mu$F, $C_3 = 45\ \mu$F and $C_2 = 30\ \mu$F, in each phase. The forward breakover and reverse withstand voltages of the power semiconductor devices are taken as 7.0 kV, while other parameters of the inverter are the same as given in Table II. The dc-link voltage is regulated at the reference value of 24 kV. The hysteresis current method discussed earlier in Section II has been used here to track the referece currents. Again for simplicity, the bands are taken equidistant from each other with $B_2 = 12$ A (Fig. 2). The sampling time step step T_s ($= 1/f_s$ in Fig. 3) has been taken 20 μs here, as opposed to 10 μs taken earlier in Section III. The PI controller parameters (as disscussed in (5)) are $K_p = 0.2$ and $K_I = 0.1$. The system is operated without the DSTATCOM connected to it till 0.5 s. The system performances under this condition can be viewed from Figs. 11 and 12 showing that the source currents, which are the same as the load currents, are unbalanced and distorted and are not in phase with the source voltages. The DSTATCOM is brought into action at 0.5 s and is operated to achieve the tasks, listed earlier. At 1.0 s, the $R - L$ loads connected at the load bus are disconnected, resulting in sudden load change as now, the source supplies only to the rectifier. It can be seen from Fig. 12(a) that once the DSTATCOM is set into operation at 0.50 s, the source voltage and current align in phase and the source currents become balanced within one-cycle. The phase-voltage has been scaled down to 0.05 times in Fig. 12(a). Both unity power factor and balanced operation is evident from the figure. Similar results are achieved in all the three phases. Fig. 12(b) shows the DSTATCOM injected current and its reference current for phase-a. Once the DSTATCOM is connected at 0.5 s, it can be seen that the injected current equals the reference within about a half-cycle. This confirms the robust tracking performance of the proposed hysteresis current control strategy.

Fig. 13(a) shows the compensated source currents and Fig. 13(b) shows the phase-c injected and its reference current

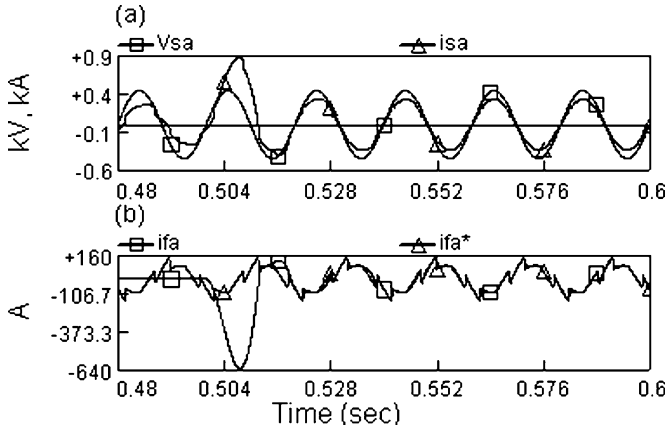

Fig. 12. DSTATCOM performance. (a) Source voltage and current of phase-a. (b) DSTATCOM-injected current and reference current.

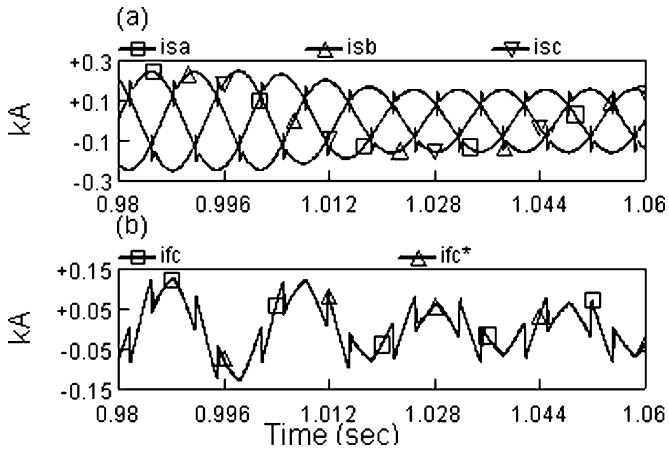

Fig. 13. System currents under compensated condition. (a) Source currents; (b) phase-c injected and its reference currents.

of the DSTATCOM to cancel out the unbalance and distortions caused by the loads. It can be seen that the source currents are balanced and free from distortions. The notches visible in the source currents are due to sudden changes in the rectifier currents. Any sudden changes in the compensator currents are precluded due to the presence of the inductors in its path. Thus, the sudden changes in the load currents are momentarily supplied by the source. The resulting THDs of the source currents are about 3.01%, which can be further reduced by reducing the width of the hysteresis bands. At 1.0 s, when the loads change, the reference currents to be injected by the DSTATCOM also change [(4)], which is evident from Fig. 13(b). It can be seen that the DSTATCOM-injected current follows the new reference current without any transient or delay. After 1.0 s, the source currents settle to new values due to change in the load, while maintaining the balanced and sinusoidal operation without any transient. This confirms the robust and reliable performance of the proposed DSTATCOM.

The losses in the inverter may force the dc capacitors to discharge, resulting in a loss of tracking. It is therefore imperative that the dc-link voltage ($V_{\rm dc}$) stored in the storage capacitors ($C_{\rm dc1}, C_{\rm dc2}$) is maintained around a prespecified set value. This is only possible by drawing additional power to overcome the losses due to R_f. The PI control strategy discussed earlier in

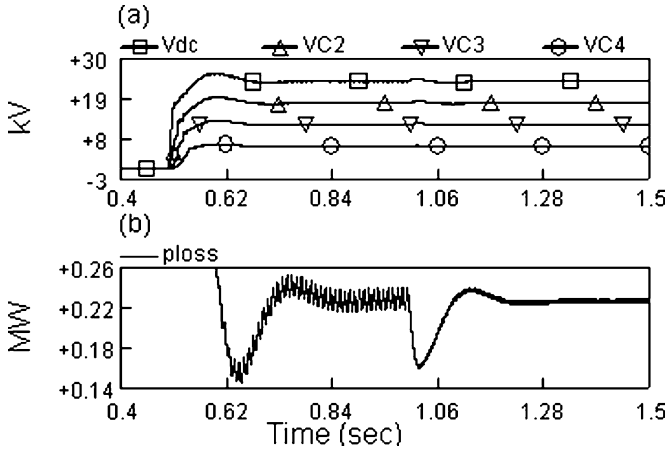

Fig. 14. Capacitor voltages and ploss. (a) DC-link and flying capacitor voltages. (b) Ploss.

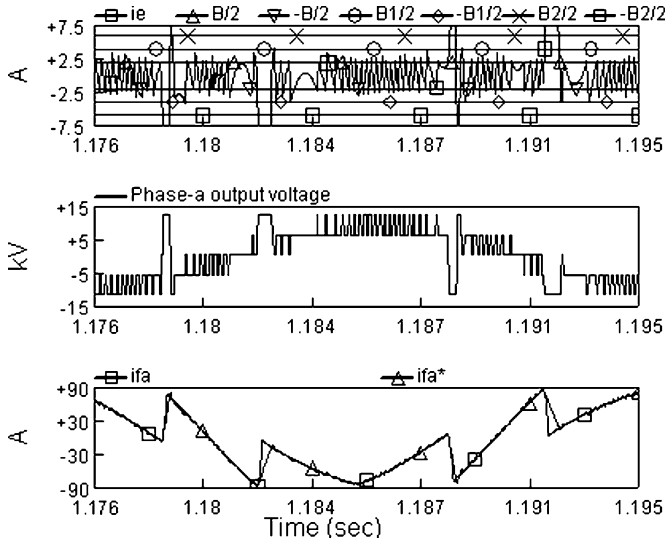

Fig. 15. Tracking performance of the inverter.

Fig. 10 is used to control the dc-link capacitor voltage. Once the DSTATCOM is switched on at 0.5 s, both the controller output and the dc-link capacitor voltage settle to the desired values within a cycle, as can be seen from Fig. 14. The phase-a flying capacitor voltages can also be seen to be balanced. The other phase's capacitor voltages show similar results. At 1.0 s, when the loads change, the p_{loss} curve remains settled with minimum transient and, hence, the capacitor voltages remain balanced throughout. The results verify the proposed control scheme and its objectives discussed earlier.

Fig. 15 shows the tracking performance of the FCMLI-based DSTATCOM under applied conditions. As the reference injected current (i_{fa}^{*}) changes suddenly, the current error accordingly changes. Following a step change, the control scheme clearly implements the minimum switched voltage state changes required to maintain the current error within the hysteresis band. Hence, the advantages of the multilevel topology are fully exploited by the scheme. It can therefore be seen that the characteristic fast dynamic response of hysteresis-based current controllers has been maintained. Following a step change in demanded current, the controller outputs the desired voltage required to follow the reference as closely as possible until the current error reaches the new hysteresis band. The fast recovery after transient and good accuracy can be appreciated. The switching frequency under the present condition is about 5.2 kHz, which is acceptable, if we compare it with those available in the literatures [1]–[3], [20]. As discussed earlier, the switching frequency and hence the losses occurring in the compensator can be further reduced by increasing T_s, capacitances of the flying capacitors and by introducing a finite band in the comparators (Fig. 3). Further, the dynamic performance of the proposed DSTATCOM can be seen to be better as compared to those in [13], [15].

The simulation results confirm the operation of the flying capacitor voltage balancing mechanism for the FCMLI and at the same time supplying the desired output currents. The proposed DSTATCOM based on the FCMLI also show satisfactory results. Time response in all cases is about or less than one cycle, which is adequate for the distribution systems.

V. Conclusions

In this paper, a proposal has been made for a DSTATCOM based on a five-level flying capacitor inverter. The basic concepts and structure of the DSTATCOM are discussed. A hysteresis current control approach has been derived in the perspective of a five-level FCMLI. A new flying capacitor voltage balancing scheme has been proposed for the FCMLI which uses the preferential charging or discharging of the flying capacitors to balance their voltages and at the same time producing the desired output line currents using hysteresis control. The simulation results verify the control scheme proposed. The performance of the compensator has been tested by simulation on a distribution network, having loads causing unbalance and distortions on the source side. The simulation results confirm that the proposed DSTATCOM offers satisfactory performance.

References

[1] A. Ghosh and G. Ledwich, *Power Quality Enhancement Using Custom Power Devices*. Norwell, MA: Kluwer, 2002.

[2] M. Saeedifard, A. R. Bakhshai, and P. Jain, "An active power filter implemented with a 3-level NPC converter in conjunction with the classification technique," in *Proc. IEEE CCECE*, 2003, vol. 1, pp. 503–507.

[3] M. K. Mishra, A. Joshi, and A. Ghosh, "Control schemes for equalization of capacitor voltages in neutral clamped shunt compensator," *IEEE Trans. Power Del.*, vol. 18, no. 2, pp. 538–544, Apr. 2003.

[4] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[5] F. Z. Peng, J. W. McKeever, and D. J. Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," *IEEE Trans. Ind. Appl.*, vol. 34, no. 6, pp. 1293–1298, Nov./Dec. 1998.

[6] A. Shukla, A. Ghosh, and A. Joshi, "Static shunt and series compensations of an SMIB system using flying capacitor multilevel inverter," *IEEE Trans. Power Del.*, vol. 20, no. 4, pp. 2613–2622, Oct. 2005.

[7] D. Soto and T. C. Green, "A comparison of high-power converter topologies for the implementation of FACTS controllers," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1072–1080, Oct. 2002.

[8] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[9] E. Bircenas, S. Ramirez, V. Cardenas, and R. Echavarria, "Cascade multilevel inverter with only one dc source," in *Proc. VIII IEEE Int. Power Elect. Congr. Tech.*, 2002, pp. 171–176.

[10] C. K. Lee, S. K. Leung, S. Y. R. Hui, and H. S. H. Chung, "Circuit level comparison of STATCOM technologies," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 1084–1092, Jul. 2003.

[11] J. D. Ainsworth, M. Davies, P. J. Fitz, K. E. Owen, and D. R. Trainer, "Static var compensator (STATCOM) based on single-phase chain circuit converters," *Proc. Inst. Elct. Eng.*, vol. 145, no. 4, pp. 381–386, 1998.
[12] D. Hanson, "A transmission SVC for national grid PLC incorporating a ±55 MVAr STATCOM," in *Inst. Elect. Eng. Colloq.: Flexible AC Transmission Systems-The FACTS*, 1998, pp. 5/1–5/8.
[13] Y. Liang and C. O. Nwankpa, "A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1118–1123, Sep./Oct. 1999.
[14] F. Zare and G. Ledwich, "A hysteresis current control for single phase multilevel voltage source inverters: PLD implementation," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 731–738, Sep. 2002.
[15] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 691–703, Oct. 1998.
[16] A. Ghosh and A. Joshi, "A new approach to load balancing and power factor correction in power distribution system," *IEEE Trans. Power Del.*, vol. 15, no. 1, pp. 417–422, Jan. 2000.
[17] G. H. Bode and D. G. Holmes, "Implementation of three level hysteresis current control for a single phase voltage source inverter," in *Proc. IEEE PESC Conf.*, 2000, vol. 1, pp. 33–38.
[18] P. C. Loh, G. H. Bode, D. G. Holmes, and T. A. Lipo, "A time-based double band hysteresis current regulation strategy for single phase multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 883–892, May/Jun. 2003.
[19] K. A. Corzine, "A hysteresis current regulated control for multilevel drives," *IEEE Trans. Energy Convers.*, vol. 15, no. 2, pp. 169–175, Jun. 2000.
[20] S. Y. Jung, T. H. Kim, S. Moon, and B. M. Han, "Analysis and control of DSTATCOM for line voltage regulation," in *Proc. IEEE Power Eng. Soc. Winter Meeting*, 2002, vol. 2, pp. 729–734.

Anshuman Shukla (S'04) received the B.Sc. engineering degree from B. R. A. Bihar University, Muzaffarpur, India, in 2001 and the M.Tech. degree in 2003 from the Indian Institute of Technology (IIT), Kanpur, where he is currently pursuing the Ph.D. degree.

His interests include power electronics and power systems dynamics and control.

Arindam Ghosh (S'80–M'83–SM'93–F'06) received the Ph.D. degree in electrical engineering from the University of Calgary, Calgary, AB, Canada, in 1983.

He is a Professor of electrical engineering at the Indian Institute of Technology (IIT), Kanpur. He has held visiting positions in Nanyang Technological University, Singapore; University of Queensland, and Queensland University of Technology, Brisbane, Australia. His interests are the control of power systems and power-electronic devices.

Avinash Joshi received the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 1979.

Currently, he is a Professor of Electrical Engineering at the Indian Institute of Technology (IIT), Kanpur, India. He was with the G.E.C. of India Ltd., Calcutta, from 1970 to 1973. His interests include power electronics, circuits, digital electronics, and microprocessor systems.