Cascaded Multilevel Control of DSTATCOM Using Multiband Hysteresis Modulation

Rajesh Gupta, *Student Member*, *IEEE*, Arindam Ghosh, *Fellow*, *IEEE*, and Avinash Joshi

Abstract—**In this paper a cascaded H-bridge inverter topology is used in a distribution static compensator (DSTATCOM). A new multiband hysteresis algorithm is used to control the switches of the cascaded *H*-bridges leading to multilevel output of the inverter. The algorithm requires hierarchal switching of each *H*-bridge. Sequential change in the hierarchy facilitates equal charging and discharging of each capacitor. This leads to self-balancing of voltage across the capacitors. The multiband hysteresis algorithm is robust even under unequal capacitor voltages due to the dissimilarity in the *H*-bridge and capacitor units. The use of a resonant controller provides good tracking of the fundamental component of reference current. Discrete sampling of the switching function limits the switching frequency of the semiconductor devices. A 7-level cascaded inverter topology is considered for shunt compensation of an 11-kV distribution system. The results are validated through PSCAD/EMTDC simulation software.**

***Index Terms*—Cascaded topology, DSTATCOM, multiband, multilevel.**

I. Introduction

SHUNT compensation for medium voltage distribution systems requires higher rating for voltage source converters (VSCs). Ratings of the semiconductor devices in a VSC are always limited; therefore for higher rated converters it is desirable to distribute the stress among the number of devices using multilevel topology [1]. Cascaded multilevel configuration of inverter has the advantage of its simplicity and modularity over the configurations of diode-clamped and flying-capacitor multilevel inverters. Application of cascaded multilevel converters for shunt compensation of distribution systems has been described in [2]-[3].

There are various current control methods for two-level converters [4]. Hysteresis control of power converters, based on instantaneous current errors, is widely used for the compensation of the distribution system as it has good dynamic characteristics and robustness against parameter variations and load non-linearties [5].

A distribution static compensator (DSTATCOM) is a voltage source converter (VSC) based device. When operated in a current control mode, it can improve the quality of power by mitigating poor load power factor, eliminating harmonic content of load and balancing source currents for unbalanced loads [5]-[7].

In this paper a cascaded seven-level inverter based DSTATCOM control is proposed. The method of three-level hysteresis control given in [8] is extended for the multilevel inverter using a multiband hysteresis control algorithm. The algorithm requires hierarchal switching of each cascaded *H*-bridge leading to unique switching scheme for multilevel output voltage. Sequential change in the hierarchy in every cycle of fundamental frequency provides equal average switching for each *H*-bridge. Therefore the charging and discharging cycle of each capacitor is the same and this leads to the self-balancing of capacitors. The dissimilarity in the cascaded units and dc link capacitors provides unequal voltage convergence in the steady state. The multiband hysteresis algorithm is robust enough to provide multilevel output even under unequal dc link voltage. However the use of multiband hysteresis leads to tracking error at the fundamental frequency that is proportional to the hysteresis band. The error is minimized using proportional plus resonant controller tuned close to the fundamental frequency [9]-[10]. The switching frequency of the semiconductor devices is limited by increasing the hysteresis band and discrete sampling of the error function [11]. The 7-level cascaded topology based DSTATCOM balances the source currents and reduces THD while improving the load power factor.

The authors are with the Department of Electrical Engineering, Indian Institute of Technology, Kanpur- 208 016, INDIA.

II. Cascaded Multilevel Converter Modulation

The block diagram of the complete modulation process of the multilevel converter is shown in Fig. 1. The current error e is sampled at discrete sampling instants and fed to the proportional (P) + Resonant controller. The output of the controller, i.e. the switching function s_e, is modulated by the multiband hysteresis to produce the control signal u. This signal provides the switching commands to the individual switches of the cascaded *H*-bridges to yield the multilevel output v_o.

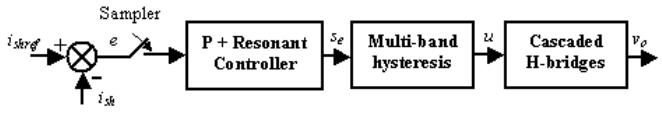

Fig. 1 Block diagram of the cascaded multilevel converter modulation.

A. Multiband Hysteresis Modulation

(1) Three-level hysteresis modulation: The three-level hysteresis modulation proposed in [8] is briefly discussed as below. Fig. 2 shows the input-output characteristics of the modulator. The parameter h is the hysteresis band and δ is a small dead-zone introduced to avoid any overlapping while s_e approaches zero. The possibility of overlapping exists due to the discrete sampling of error function in which between two sampling instants, the switching function s_e might cross the surface $s_e = 0$.

The following algorithm describes the three-level modulation.

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Condition 1: $s_e > 0$ then (1)

$u = +1$ for $s_e > +h$

$u = 0$ for $s_e < +\delta$

Condition 2: $s_e < 0$ then

$u = -1$ for $s_e < -h$

$u = 0$ for $s_e > -\delta$

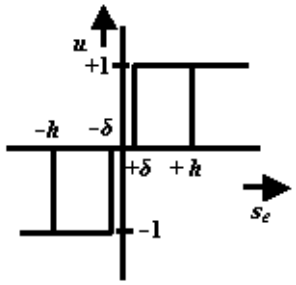

Fig. 2 Three-level hysteresis modulation.

(2) Seven-level hysteresis modulation: The algorithm of three-level hysteresis modulation may be extended to multilevel using the multiband hysteresis modulation. The input-output characteristic of the multilevel modulator is shown in Fig. 3.

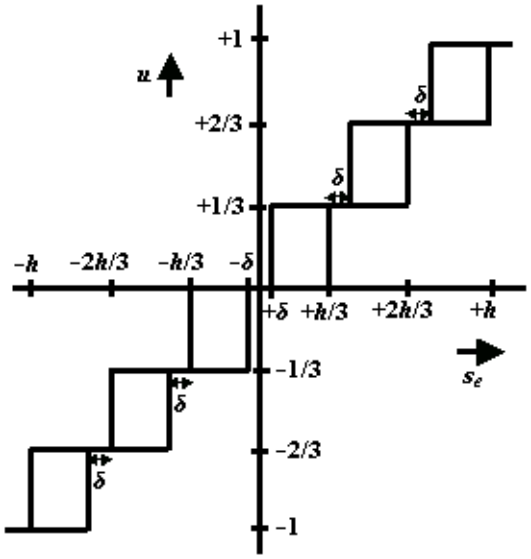

Fig. 3 Seven-level hysteresis modulation.

The following algorithm describes the seven-level modulation.

Condition 1: $s_e > 0$ then (2)

Condition 1.1: $s_e > +\delta$ then

$u = +1/3$ for $s_e > +h/3$ & $s_e < +(h/3+\delta)$

$u = 0$ for $s_e < +\delta$

Condition 1.2: $s_e > +(h/3+\delta)$ then

$u = +2/3$ for $s_e > +2h/3$ & $s_e < +(2h/3+\delta)$

$u = +1/3$ for $s_e < +(h/3+\delta)$

Condition 1.3: $s_e > +(2h/3+\delta)$ then

$u = +1$ for $s_e > +h$

$u = +2/3$ for $s_e < +(2h/3+\delta)$

Condition 2: $s_e < 0$ then

Condition 2.1: $s_e < -\delta$ then

$u = -1/3$ for $s_e < -h/3$ & $s_e > -(h/3+\delta)$

$u = 0$ for $s_e > -\delta$

Condition 2.2: $s_e < -(h/3+\delta)$ then

$u = -2/3$ for $s_e < -2h/3$ & $s_e > -(2h/3+\delta)$

$u = -1/3$ for $s_e > -(h/3+\delta)$

Condition 2.3: $s_e < -(2h/3+\delta)$ then

$u = -1$ for $s_e < -h$

$u = -2/3$ for $s_e > -(2h/3+\delta)$

The algorithm can be extended to any number of levels of hysteresis modulation.

B. Three-Phase Converter Topology

In the multiband hysteresis algorithm for an n-level inverter (n = 3, 5, 7, …), the voltage stress of the semiconductor switches and dc-link capacitor is $2/(n-1)$ times the net dc link voltage required. The total number of power semiconductor devices required per-phase is $2\times(n-1)$. The output voltage levels are added through the $(n-1)/2 = N$ number of cascaded H-bridges. Therefore for obtaining seven switched dc levels proposed in this paper, 3 H-bridges are required for each phase as shown in Fig. 4. VSC-A, VSC-B and VSC-C represent the voltage source converters for phases-a, b and c respectively. Each of the switches in the figure consists of a power semiconductor device (e.g., IGBT) and an anti-parallel diode. The voltages V_{dca1}, V_{dca2} and V_{dca3} are the dc link voltages across the capacitors C_{dca1}, C_{dca2} and C_{dca3} respectively of the cascaded H-bridges for phase-a. The dc-link voltages and capacitors of phase-b and phase-c may be defined similarly. The common points of the three converters are connected to the system neutral.

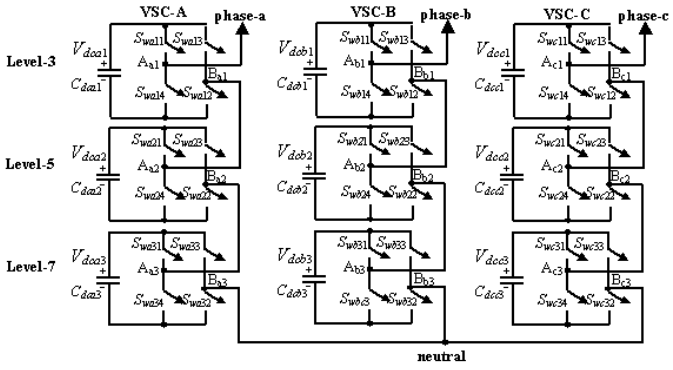

Fig. 4 Cascaded configuration of three-phase seven-level VSC's.

C. Hierarchical Switching Scheme

There are many switching combinations for obtaining the same level of the inverter output voltage [12]. In this section a novel switching scheme is proposed to follow the algorithm given in (2) for the 7-level output. This leads to a unique switching pattern for each levels of the output. In this scheme the switching stress of all the switches are equal. Moreover the average switching stress for each *H*-bridge is also equal. Consider phase-a of the converter of Fig. 4. The following three hierarchies of the *H*-bridges are chosen:

(i) Level-3, (ii) Level-5 and (iii) Level-7 *H*-bridge.

For Condition 1, the left leg switches of all the *H*-bridges of phase-a are kept at low switching frequency, i.e. the switches S_{wa11}, S_{wa14}, S_{wa21}, S_{wa24}, S_{wa31} and S_{wa34} change their states at the fundamental frequency as follows.

Condition 1: $s_{ea} > 0$ Switches S_{wa11}, S_{wa21}, S_{wa31} are ON

Note that the complementary switches will be OFF. Under steady state condition the switching function s_{ea} varies at the fundamental frequency. Therefore the left leg switches operate at this frequency for positive half cycle.

The right leg switches of the *H*-bridges, i.e., S_{wa13}, S_{wa12}, S_{wa23}, S_{wa22}, S_{wa33} and S_{wa32} operate at high switching frequency for the positive half cycle of switching function s_{ea} following the multiband hysteresis modulation. Each hierarchical bridge will operate for that corresponding level of output only. The switch position of other *H*-bridges will remain fixed in this period. Consider the Condition 1, i.e., $s_{ea} > 0$ as

(i) Condition 1.1: $s_{ea} > +\delta$; (Level-3 operation)

Case 1: $s_{ea} > +h/3$ & $s_{ea} < +(h/3+\delta)$ Switch S_{wa12} is ON

Case 2: $s_{ea} < +\delta$ Switch S_{wa13} is ON

switches S_{wa23} and S_{wa33} remain ON for both the above conditions. This leads the inverter output to toggle between $+V_{dc}/3$ and 0.

(ii) Condition 1.2: $s_{ea} > +(h/3+\delta)$; (Level-5 operation)

Case 1: $s_{ea} > +2h/3$ & $s_{ea} < +(2h/3+\delta)$; Switch S_{wa22} is ON

Case 2: $s_{ea} < +(h/3+\delta)$; Switch S_{wa23} is ON

switches S_{wa12} and S_{wa33} remain ON for both the above conditions. This leads the inverter output to toggle between $+2V_{dc}/3$ and $+V_{dc}/3$.

(iii) Condition 1.3: $s_{ea} > +(2h/3+\delta)$;(Level-7 operation)

Case 1: $s_{ea} > +h$ Switch S_{wa32} is ON

Case 2: $s_{ea} < +(2h/3+\delta)$ Switch S_{wa33} is ON

switches S_{wa12} and S_{wa22} remain ON for both the above conditions. This leads the inverter output to toggle between $+V_{dc}$ and $+2V_{dc}/3$.

Now for Condition 2, i.e. $s_{ea} < 0$, the right leg switches of all the *H*-bridges are kept at low switching frequency, i.e., the switches S_{wa13}, S_{wa12}, S_{wa23}, S_{wa22}, S_{wa33} and S_{wa32} change their states at the fundamental frequency for the negative half cycle of s_{ea} as follows

Condition 2: $s_{ea} < 0$ Switches S_{wa13}, S_{wa23}, S_{wa33} are ON

The left leg switches in this case, i.e. S_{wa11}, S_{wa14}, S_{wa21}, S_{wa24}, S_{wa31} and S_{wa34} operate at high switching frequency for the negative half cycle of the switching function s_{ea}. The switch position of these left leg switches may be defined based on the Conditions 2.1, 2.2 and 2.3 of equation (2) to obtain the output levels of 0, $-V_{dc}/3$, $-2V_{dc}/3$ and $-V_{dc}$.

Effectively, level-3 and level-5 *H*-bridge shares the switching for approximately $2/5^{th}$ duration of the fundamental period, while level-7 *H*-bridges share the switching for approximately $1/5^{th}$ duration of the fundamental period. Fig. 5 shows the 7-level inverter output voltage v_{oa} and the switching function s_{ea} following the above switching scheme. The switching function s_{ea} is shown with the amplification factor of 200 for clarity.

With the fixed hierarchy given in Fig. 4, the switching stress for each *H*-bridge will be different. In order to have equal switching stress, the hierarchy of each *H*-bridge is swapped sequentially at the fundamental time period. This is accomplished by running a counter that resets at the fundamental frequency. At every reset, the hierarchy is changed cyclically. This provides equal average switching for all the cascaded *H*-bridges. The charging and discharging cycles will also be equal for all the capacitors and that will provide the self-balancing capability of the dc-link voltage across the capacitors. The average switching frequency of all the switches are approximately ($1/6^{th}$) of the instantaneous switching frequency of the cascaded output voltage. The cascaded inverters of other phases are also modulated similar to phase-a.

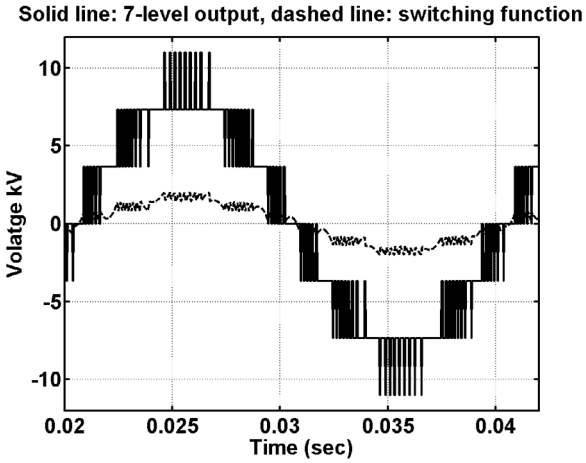

Fig. 5 7-level inverter output voltage v_{oa} and switching function s_{ea}×200.

D. Modulator Gain

The multiband hysteresis modulation proposed above for the multilevel inverter is a nonlinear function on the instantaneous basis. However modulator offers a linear relationship between switching function s_{ea} and the inverter output voltage v_{oa} on the average basis. From (2) it may be noted that the amplitude of the switching function s_{ea} varies between $-h$, $-2h/3$, $-h/3$, 0, $+h/3$, $+2h/3$, $+h$. The variation approximately follows the sinusoidal function with the peak amplitude of h as seen from Fig. 5. The output of the inverter v_o at the same instants varies as $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, 0, $+V_{dc}/3$, $+2V_{dc}/3$, $+V_{dc}$. The variation of v_{oa} also follows the approximate sinusoidal function of the same frequency and phase as that of s_{ea} with the peak amplitude of V_{dc} (see Fig. 5). Therefore the av-

erage gain M obtained between inverter output voltage v_{oa} and the switching function s_{ea} may be written as

$$M = \frac{v_{oa}(t)}{s_{ea}(t)} = \frac{V_{dca}}{h} = \frac{\sum_{i=1}^{N} V_{dcai}}{h} \tag{3}$$

where N is the number of cascaded H-bridges which in this case is equal to 3.

III. DSTATCOM CONTROL

A. System Configuration

Fig. 6 shows a three-phase four-wire distribution system that is compensated by a DSTATCOM. The three-phase load is supplied from the voltage source v_{sk} through the feeder with the impedance of (R_{sk}, L_{sk}), where $k = a,b,c$ for the three-phase respectively. The DSTATCOM is represented by VSCs in the shunt path with the interfacing inductance L_{shk}. The resistance R_{shk} represents the loss equivalent due to the inverter switching. The voltage at the point of common coupling (PCC) is denoted by v_{tk}. The currents flowing through the different branches at the PCC are the source current i_{sk}, the load current i_{lk}, and the current injected in shunt branch i_{shk}. For the 3-phase, 4-wire configuration, the load neutral n_l and the compensator neutral n_{sh} are connected to the source neutral n_s.

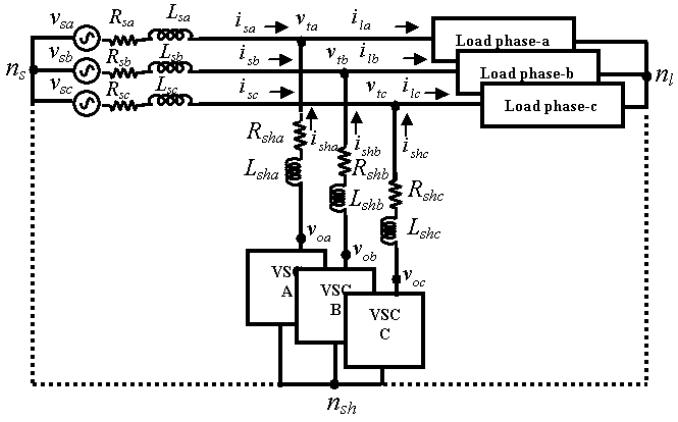

Fig. 6 Shunt compensation of three-phase four-wire distribution system.

B. Compensator Model

The DSTATCOM contains two control loops – one for the current and the other for the dc-link voltage (V_{dc}). These two loops are controlled separately. The current control loop is separated from the dc voltage control loop as the latter is much slower. Therefore the dc voltage is assumed to be constant for the purpose of modeling current control loop. The differential equation for the shunt compensator for phase-a may be written as

$$L_{sha}\frac{di_{sha}}{dt} = -R_{sha}i_{sha} + v_{oa} - v_{ta} \tag{4}$$

Taking Laplace transform on both the sides of (4), the following equation in the s-domain is obtained

$$I_{sha}(s) = \frac{1/L_{sha}}{s + R_{sha}/L_{sha}}V_{oa}(s) - \frac{1/L_{sha}}{s + R_{sha}/L_{sha}}V_{ta}(s) \tag{5}$$

Fig. 7 shows the block diagram of the multilevel current control loop of the DSTATCOM. The reference shunt current for the phase-a is represented by $i_{sh\ refa}$. The controller transfer function is denoted by $G_c(s)$. The block M represents the modulator gain (3) and $G(s)$ is the compensator transfer function obtained from (5) as

$$G(s) = \frac{1/L_{sha}}{s + R_{sha}/L_{sha}} \tag{6}$$

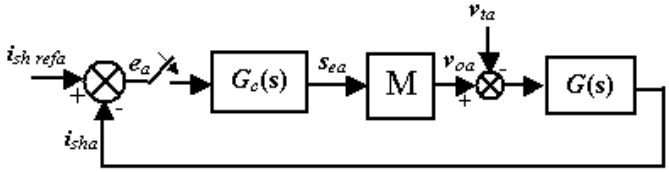

Fig. 7 Current control loop of the DSTATCOM.

C. Proportional plus Resonant Controller

As shown in Section II, the multiband hysteresis control algorithm offers a finite gain at the fundamental frequency ω_o. This leads to error in tracking fundamental component of current reference. It is proposed to pass the error through a proportional plus resonant controller as shown in Fig. 7. The controller is tuned close to the fundamental frequency to minimize the error at this frequency [9]-[10]. The controller structure in the frequency domain is written as

$$G_c(s) = \frac{S_{ea}(s)}{E_a(s)} = K_p + \frac{2K_i s}{s^2 + \omega_o^2} \tag{7}$$

where K_p and K_i are the proportional and integral gains respectively. Fig. 8 shows the Bode plot of the controller (7) for K_p = 1.0, K_i = 10.0 and ω_o = 314 rad/sec (for the fundamental frequency of 50 Hz). The resonant frequency ω_o should be continuously updated using the current estimate of the fundamental frequency. The controller provides high gain at the resonant frequency ω_o to compensate the error component at this frequency. The phase characteristics at the fundamental frequency suffer a 180° shift. This deteriorates the transient performance and makes the convergence sluggish at this frequency. Both magnitude and phase characteristics are governed by the proportional gain K_p at other frequencies.

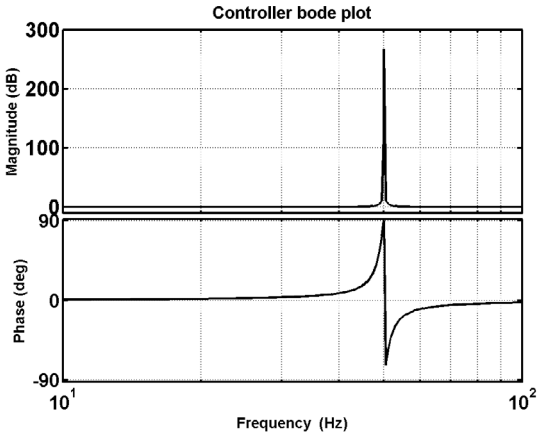

Fig. 8 Bode plot of the proportional plus resonant controller.

Consider a discrete sampling period of T_s sec for the sampling of the error function e_a. The advantage of using the sampler is to restrict the switching frequency of the semiconductor

devices to be less than or equal to ($1/2T_s$). The actual frequency depends upon the width of the hysteresis band h. The larger the band, the lower will be the switching frequency. Consider one sample delay as the switching delay. Then the switching delay is represented by the first order lag transfer function $G_d(s) = 1/(1+ T_s s)$. The closed loop transfer function with respect to reference shunt current for the closed loop system shown in Fig. 7 may then be written as

$$T_{ref}(s) = \left.\frac{I_{sha}(s)}{I_{sh\,refa}(s)}\right|_{V_{ta}=0} = \frac{MG_c(s)G_d(s)G(s)}{1+MG_c(s)G_d(s)G(s)} \tag{8}$$

Similarly the transfer function with respect to the terminal voltage that act as a periodic perturbation for the current control loop, may be written as

$$T_{pert}(s) = \left.\frac{I_{sha}(s)}{V_{ta}(s)}\right|_{I_{tsh\,refa}=0} = \frac{G(s)}{1+MG_c(s)G_d(s)G(s)} \tag{9}$$

Example 1: Consider the system parameters given in Appendix A. The sampling frequency is chosen as 10 kHz such that the instantaneous switching frequency will be less than 5 kHz. The hysteresis band selected as h = 0.01 kA with a δ of 0.002 kA.

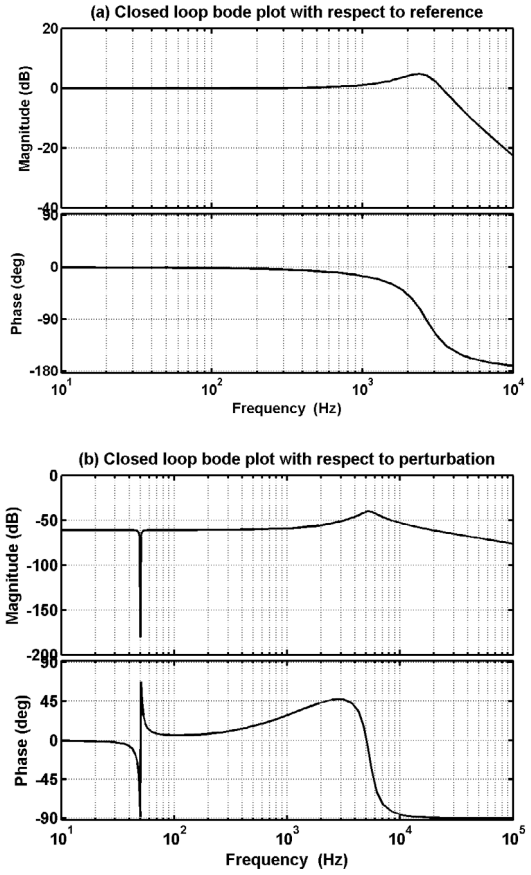

Fig. 9 Closed loop Bode plot (a) with respect to reference shunt current, (b) with respect to the perturbation at PCC.

Fig. 9 (a) shows the closed loop Bode plot of the system shown in Fig. 7 with respect to the reference shunt current, while assuming a constant modulator gain M for all the frequency components. It can be seen from Fig. 9 (a) that the system tracks the reference over a wide range of frequencies. Fig.9 (b) shows the closed loop frequency response with respect to the PCC voltage perturbation v_{ta}. The system offers good attenuation at all frequencies and strong attenuation at the fundamental frequency for the input perturbation v_{ta}. The system gain and phase margins are found be be infinity and 18.2° respectively. This implies the stability of the closed loop system.

IV. Reference Current Generation

The reference current generation in this paper follows the method described in [5]-[6]. Refer to Fig. 7; the current control requires the reference for shunt current $i_{sh\ ref}$ for each phase. For an independent control of the shunt currents in the three-phases, the references for shunt currents are determined on-line using the following equations [6]

$$\left.\begin{aligned} i_{sh\,refa} &= i_{la} - \frac{v_{ta}-v_0}{\Delta}\left(p_{lav}+p_{dc}\right) \\ i_{sh\,refb} &= i_{lb} - \frac{v_{tb}-v_0}{\Delta}\left(p_{lav}+p_{dc}\right) \\ i_{sh\,refc} &= i_{lc} - \frac{v_{tc}-v_0}{\Delta}\left(p_{lav}+p_{dc}\right) \end{aligned}\right\} \tag{10}$$

where i_{shrefk}, i_{lk} and v_{tk}, $k = a,b,c$ respectively are the reference shunt current, load current and PCC terminal voltages for the three phases and

$$v_0 = \frac{1}{3}\sum_{\alpha=a,b,c} v_{t\alpha} \text{ and } \Delta = \left[\sum_{\alpha=a,b,c} {v_{t\alpha}}^2\right] - {v_0}^2$$

In (10), p_{lav} is the average load power that is obtained by a moving average filter using the continuous measurement of instantaneous power given by

$$p_l = v_{ta}i_{la} + v_{tb}i_{lb} + v_{tc}i_{lc} \tag{11}$$

The averaging window is half a fundamental cycle. Note that the PCC terminal voltages v_{tk}, $k = a,b,c$, used in (10), are the fundamental frequency components of the switching frequency contaminated terminal voltages that are extracted on-line from the measurement of the actual voltages [5]-[6].

The variable p_{dc} in (10) is the power drawn from the ac-system to replenish the loss caused by the DSTATCOM circuit. The main objective of p_{dc} is to hold the average dc voltage V_{dcav} constant and equal to V_{dcref} and hence the dc control loop is given by

$$p_{dc} = K_{pdc}e + K_{idc}\int e\,dt \tag{12}$$

where K_{pdc} and K_{idc} are the proportional and integral gains respectively for the dc control loop. The error e between the reference dc voltage and the average dc voltage is given as

$$e = V_{dc\,ref} - V_{dc\,av} \tag{13}$$

where the dc voltage $V_{dc\ av}$ is the average of the dc link voltages across each cascased H-bridge of all the three phases.

V. SIMULATION RESULTS

Consider the shunt compensated distribution system shown in Fig. 6. The DSTATCOM is realized by three 7-level cascaded multilevel inverters that are supplied from seperate dc capacitors as shown in Fig. 4. The following example illustrates the performance of the proposed compensator with the multiband hysteresis algorithm of (2) and using the P+Resonant controller of (7). The reference shunt currents are derived from (10).

Example 2: The parameters of the system are given in Appendix A. The unbalanced linear load is given by

$$R_{la} = 102.0\ \Omega, L_{la} = 350.0\,mH, R_{lb} = 180.0\ \Omega, L_{lb} = 400.0\,mH$$
$$R_{lc} = 80.0\ \Omega, L_{lc} = 300.0\,mH$$

In addition the load contains a 3-phase rectifier bridge supplying a load of 100 Ω and 300 mH. The sampling period and hysteresis band is same as selected in Example 1. There is a 10% variation in the dc link capacitance value. The reference voltage for the dc capacitor is kept at 3.6 kV and PI parameters of dc voltage control loop (12) are chosen as K_{Pdc} = 0.3 and K_{idc} = 0.3 sec^{-1}.

The simulation is performed in the PSCAD/EMTDC simulation package (version 3.0.7). The following parameters of IGBT and anti-parallel diodes are considered: For both the devices on-resistance and off-resistances are 20 mΩ and 1 MΩ respectively. The on-voltage IGBT and diodes considered are 1.5 V and 0.7 V respectively. The complimentary switches of the same arm of the *H*-bridges are gated through the dead-time delay of 5.0 μsec.

The total harmonic distortion (THD) in the source current for uncompensated system is 14.5%. The three-phase currents are unbalanced with the poor power factor. Fig. 10 shows the source currents for the uncompensated system. It is desired to bring down the THD in source current to be within an acceptable limit with good tracking of fundamental component while balancing the three-phase source currents. The steady state performance of the compensator is discussed below.

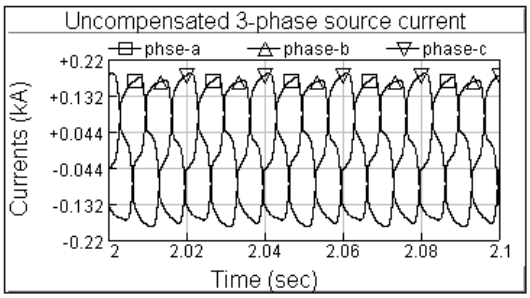

Fig. 10 Three phase source currents for uncompensated distribution system.

Fig. 11 shows the compensated source currents using the proposed modulation and control. The source currents are balanced with the THD improved to 3.5%. The proportional plus resonant controller is tuned near to the fundamental frequency with 1.0% error in frequency estimates. This leads to the maximum error of 3.0 A (rms) for the tracking of the fundamental component of the shunt current.

The source current is in phase with the terminal voltage as shown in the Fig. 12 (for phase-a only). This implies a near unity power factor operation. The shunt current tracking characteristic is shown in Fig. 13. In the absence of the resonant controller, an error of about 10 A (rms) is observed in the tracking of the fundamental component. The 7-level inverter output voltage for the phase-a is shown in Fig. 14. The other two-phases have similar characteristics as those shown in Figs. 12 to 14 for the a-phase. An average switching frequency of 425.0 Hz is observed for all the switches.

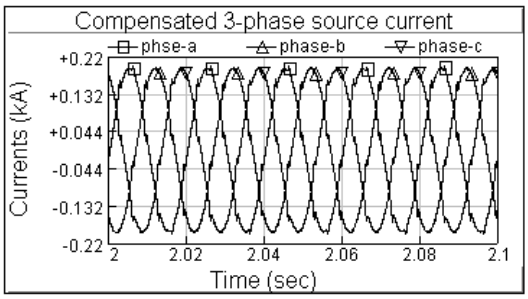

Fig. 11 Three phase source currents for compensated distribution system.

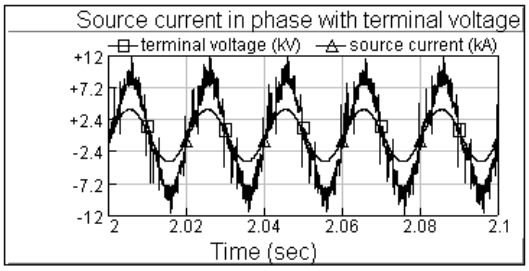

Fig. 12 In-phase source current with terminal voltage for phase-a.

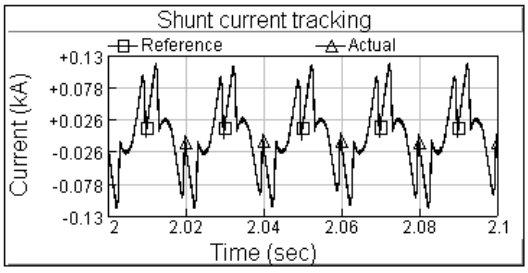

Fig. 13 Shunt current tracking characteristics of phase-a.

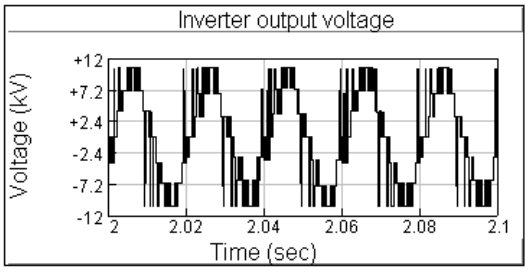

Fig. 14 Inverter output voltage for phase-a.

With the swapping of the hierarchy of each *H*-bridge, equal average switching is obtained for all the *H*-bridges. Fig. 15 shows the convergence of the dc-link voltage of the cascaded *H*-bridges for the phase-a. Unequal dc-link capacitance leads to unequal voltage convergence in the steady state. However the multiband hysteresis algorithm is robust enough to provide multilevel output even under the unequal dc link voltages. Similar voltage convergences are observed for the other

phases. Fig. 16 shows the total power loss occurring in the three-phase inverter circuit (represented by equivalent loss resistance R_{sh}). After initial large power loss during transient, the losses settle to few kilowatts in the steady state. Total three phase compensated load is around 2.5 megawatts.

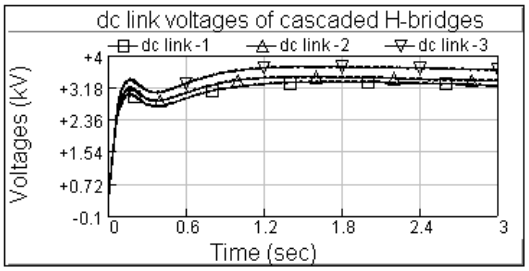

Fig. 15 dc link voltage convergence of the cascaded H-bridges for phase-a.

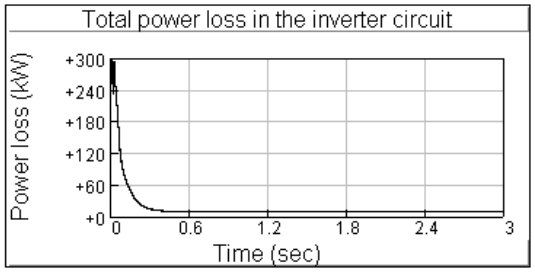

Fig. 16 Total power loss in the three-phase cascaded inverter circuit.

VI. CONCLUSIONS

Cascaded multilevel topology is well suited for current control of higher rated DSTATCOM, as this requires similar multiple modular cells depending upon the device ratings. The proposed multiband hysteresis hierarchical algorithm provides multilevel output even under unequal dc link voltages. The sequential swapping of the hierarchy provides for equal average switching for each *H*-bridge. Hence this leads to the self-balancing capability to the voltage across each dc link capacitor. The use of proportional plus resonant controller gives good tracking performance for the fundamental component of the reference current. Discrete sampling of the error function limits the switching frequency of the inverter. The DSTATCOM control balances the source current with significant improvement in the THD and power factor.

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APPENDIX A: System Parameters

Parameters	Numerical value
Source voltage v_{sk}	11.0 kV (L-L) rms
Feeder impedance R_{sk}, L_{sk}	2.0 Ω, 25.0 mH
Inverter losses R_{shk}	1.0 Ω
Shunt inductance L_{shk}	40.0 mH
DC link capacitor C_{dcki} and Reference voltage V_{dcki} for each *H*-bridge	5000 μF ± 10%, 3.6 kV

Rajesh Gupta (S'05) is a doctoral student in the Department of Electrical Engineering at IIT Kanpur, India on a study leave from National Institute of Technology, Allahabad, India, where he is holding the post of Senior Lecturer. From 1996 to 1999 he served as Lecturer in the Department of Electronics & Electrical of G.B Pant Engg. College, Pauri Garhwal, India. He has obtained his Bachelor of Engineering degree Electrical from MMM Engineering College, Gorakhpur, India, in 1993 and his Master of Engineering degree from BIT, Mesra, Ranchi, India, in 1995. His interests include Control of Power Electronics based Systems, Power Quality and Systems Dynamics.

Arindam Ghosh (S'80, M'83, SM'93, F'06) is a Professor of Electrical Engineering at IIT Kanpur, India. He has received a Ph.D. in EE from University of Calgary, Canada in 1983. His interests are in Control of Power Systems and Power Electronic devices. He is a fellow of Indian National Academy of Engineering (INAE)

Avinash Joshi is a Professor of Electrical Engineering at IIT Kanpur, India. He has worked at the G.E.C. of India Ltd (1970-73), Calcutta, India. He has obtained a Ph.D. (1979) in EE from University of Toronto, Canada. His interests include Power Electronics, Circuits, Digital Electronics, and Microprocessor Systems.