A Hysteresis Current Control for Single-Phase Multilevel Voltage Source Inverters: PLD Implementation

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***Abstract*—In most high-performance applications of voltage source pulse-width modulation inverters, current control is an essential part of the overall control system. In this paper, a hysteresis current control technique for a single-phase five-level inverter with flying-capacitor topology is proposed. Logic controls and a programmable logic device are suitable for handling a large number of switches and implementation of state transitions. This method also considers how to improve unbalanced voltages of capacitors using voltage vectors in order to minimize switching losses. The simulation and experimental results describe and verify the current control technique for the inverter.**

***Index Terms*—Current control, multilevel inverter, PLD, pulse-width modulation.**

I. Introduction

DURING the last decade, multilevel inverters have attracted much attention due to reduced harmonic content and voltage stress, (dv/dt), in high power electronic applications. Switching of power electronic devices is controlled in multilevel inverters to synthesise a desired output waveform using several levels of voltage and a pulse-width modulation (PWM) technique. As the number of voltage levels increases, the output waveform becomes a staircase wave based on the PWM technique, which approaches a sinusoidal waveform with minimum harmonic distortion. The most popular structure proposed as a voltage source multilevel inverter is the diode clamp inverter based on the neutral point converter [1] and the flying-capacitor topology [2] as shown in Fig. 1. Generalized structures and applications of the multilevel inverters have been reported [3], [4].

The performance of the inverter system largely depends on the quality of the control strategy. Different current control techniques for the traditional inverter have been considered by several authors [5]–[9]. The current controlled PWM inverters have some advantages compared to the conventional open-loop voltage source PWM inverters [7], [8] such as: control of instantaneous current waveform with high accuracy, peak current protection, overload rejection, compensation of effects due to load parameter changes, and semiconductor voltage drops of the inverters.

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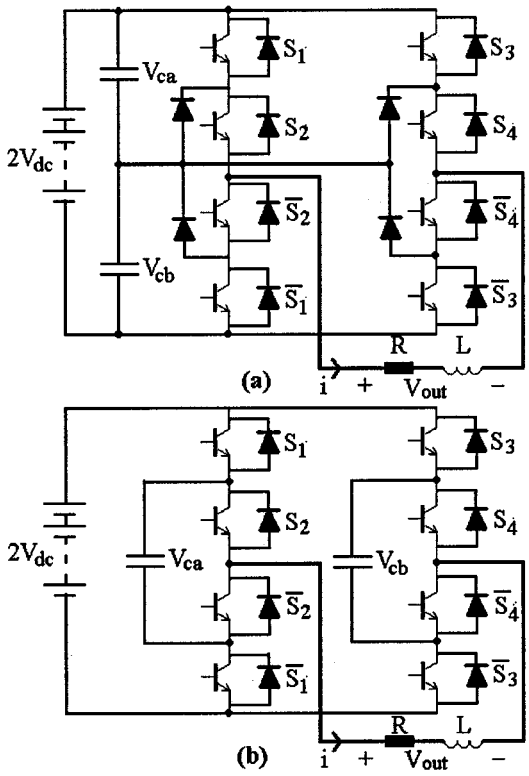

Fig. 1. Single-phase five level inverter topologies:. (a) Diode-clamp. (b) Flying capacitor.

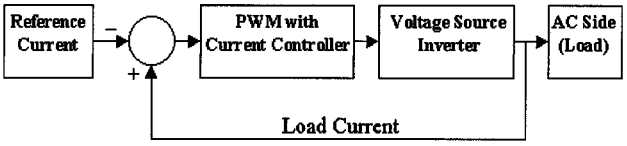

Fig. 2. Basic diagram of a current controller.

By comparing a reference current and a load current, the current controller can generate switching states for the power electronic devices, which decreases the current error and provides the desired current waveform for a load. Fig. 2 shows a basic diagram of a voltage source PWM inverter with a current control loop.

The conventional two-level hysteresis current control technique is one type of nonlinear current control based on the current error, which consists of a comparison between the load cur-

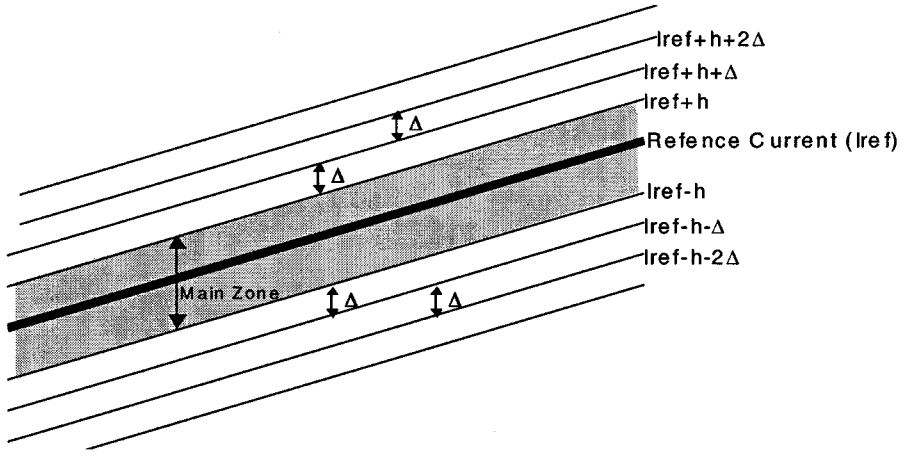

Fig. 3. Tolerance bands for "n" level inverter.

rent and the tolerance band around the reference current. While the load current is between upper and lower bands, no switching occurs and when the load current crosses to pass the upper limit (lower band) the output voltage is decreased (increased).

A three level hysteresis current control technique for a single-phase voltage source inverter has been proposed by Bode and Holmes [9]. To achieve this three-level modulation, two hysteresis comparators with a small offset are used for the control section. This concept cannot be expanded to "n" level. Current control techniques for multilevel inverters based on multiband hysteresis have been reported [11], [12] but do note take state transition losses or capacitor control into account. Inverter states for capacitor voltage control are discussed in [13] and [14], but this is not applied in a current control context. The contribution of this paper is in specific capacitor voltage control, low losses through switch adjacency, and precise current control.

The hysteresis current control technique for the multilevel inverter based on minimum switching losses is more complex than for the traditional inverter due to more voltage levels and also the requirement of balancing the capacitors' voltages. This paper presents a new hysteresis current control technique based on magnitude and time errors for an "n" level single-phase inverter with flying-capacitor topology. In this technique, the switching states are achieved as follows:

- *band change based on time limit*;
- *level change based on hysteresis technique*;
- *switching states based on capacitor voltage balancing*;
- *minimum switching losses based on adjacent voltage vectors*.

Field-programmable logic devices (FPLDs) have been available for a number of years. The role of FPLDs has evolved to the stage where they can implement very complex systems functions, such as microprocessors and microcomputers. Their popularity comes from the high flexibility of individual devices, high circuit densities, as well as the range of design tools [10]. EPM7128S PLD from the MAX7000 family with high-performance and EEPROM structure has been utilized. Simulations and experiments have been carried out to confirm the current control method for a five-level inverter.

II. Current Control Properties

The hysteresis current control based on the magnitude error for an "n" level inverter can be associated with number of bands around the reference current, in such a manner that each band does not belong to a specific voltage level. The tolerance bands for an "n" level inverter are of two different natures. The first band consists of a main zone with $I_{ref} \pm h$ bands and the load current always has to be inside the main zone to minimize the harmonic distortion as shown in Fig. 3. The size of the main band, "h," is largely determined by the permitted level of current distortion; other determining factors are the load value, the input voltage and the desired switching frequency. The second set of switching bands has different zones separated by Δ in order to provide a reliable and a robust control for an "n" level inverter. A key issue is the change of switch voltage when the derivative of the load current is not high enough to follow the reference current. A five-level controller may select between voltage levels $2V$, V, 0, $-V$, and $-2V$. Initially we may be using the pair 0, V to keep the current in the main band. If the current crosses the level $I_{ref}+h$ we select "0" else if the current crosses $I_{ref}-h$ we select "V." However, if this selection fails to keep the current in the main band, it will cross $I_{ref}-h-\Delta$ and we need to change the switch levels to use "V" and "$2V$." Each crossing of the additional bands will trigger a level change.

The output voltage of the inverter, V_{inv}, can be related to the parameters of simple R-L load components as follows:

$$V_{inv} = Ri + L\frac{di}{dt} + V_{back} \tag{1}$$

where

V_{inv}	$nV_{dc}(n = 2, -1, 0,1,2)$;
i	load current;
L, R	load inductance and resistance;
V_{back}	back emf voltage.

Since the voltage across the load resistance is often small, this value can often be neglected. Thus, (1) becomes

$$\frac{d(i-I_{ref})}{dt} \approx \frac{V_{inv}+V_{back}}{L} - \frac{d(I_{ref})}{dt}. \tag{2}$$

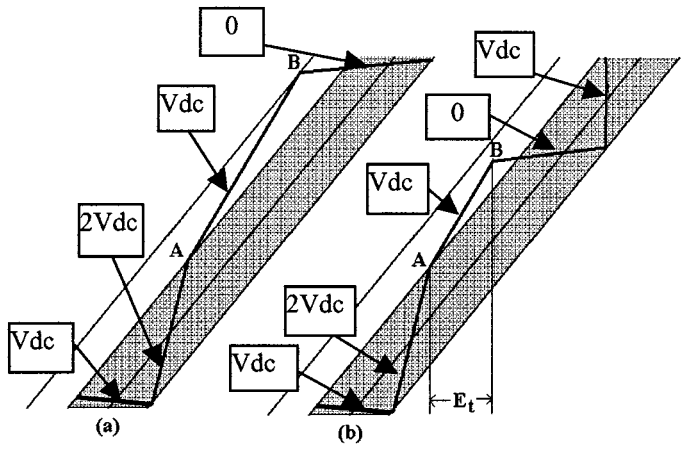

Fig. 4. (a) Load current for hysteresis current control based on magnitude error. (b) Load current for hysteresis current control based on magnitude and time errors.

As V_{back} increases or as larger reference slopes are requires, larger average values of V_{inv} need to be used. Similar to the traditional hysteresis current control, when the load current crosses the first upper ($I_{ref}+h$) or lower band ($I_{ref}-h$), the output voltage is changed by one level in order to increase or decrease the load current to follow I_{ref} based on (2). We start from an inverter voltage of V_{dc}, and switch between V_{dc} and $2V_{dc}$ to keep the current retained in the main band. When the load current exceeds the first upper band at point A, as shown in Fig. 4(a), the inverter voltage is decreased one level as normal ($2V_{dc} \rightarrow V_{dc}$). After "A" however, the load current still is out of the main zone since the derivative of the load current is not high enough to follow the reference current. No further switching occurs until the load current crosses the second upper band at point B. Then, the output voltage is decreased one level more ($V_{dc} \rightarrow 0$) and the load current follows the reference current and moves to the main zone. After the level change, the main zone is now associated with 0 and V_{dc},. Indeed, each band is not associated with a specific voltage level but the voltage level pair is changed in the process of tracking the reference.

Time error can be applied to this hysteresis current control to optimize the level change of the current controller as shown in Fig. 4(b). In this case, when the load current exceeds the first upper band at point A, the output voltage is changed one level ($2V_{dc} \rightarrow V_{dc}$) and then the controller waits for a certain period of time, E_t. If the load current does not move to the main zone after E_t, the controller changes the output voltage one level more at point B ($V_{dc} \rightarrow 0$). The value of E_t can be achieved using (2) in terms of the maximum value of the derivative of the load current. For the same load, the maximum value of the derivative of the load current occurs when the output voltage of the inverter has the maximum value. Thus, for a single phase five level inverter, the maximum value of the current derivative in (2) becomes

$$\frac{di}{dt} \approx \frac{2V_{dc}+V_{back}}{L}. \tag{3}$$

An approximation of (3) during one switching cycle can be defined as

$$\frac{\Delta i}{\Delta t} \approx \frac{2V_{dc}+V_{back}}{L}. \tag{4}$$

Thus, the minimum time for changing the load current from the first band to the second band, "Δ," can be found as

$$\Delta t_{\min} \approx \frac{\Delta L}{(2V_{dc}+V_{back})}. \tag{5}$$

Therefore, the value of the time error period E_t can be achieved from (5), which is based on the maximum derivative of the load current. One aspect of using time error to determine band changes is that large voltage transitions for an "n" level control can take n times the time error to reach the target. This can only be improved if the open loop plant modeling is sufficiently accurate that the desired final state can be accurately computed rather than determined by feedback.

III. Capacitor Voltage Control With Adjacent Voltage Vectors

In contrast to the two level hysteresis current control, the new current controller has to efficiently utilize several voltage levels with adjacency. Adjacency means that moving from one voltage level to another can be achieved by one switch change. In this paper, a multilevel inverter with flying-capacitor has been considered however the concept of the control technique can be applied to the diode-clamp topology. All possible switching states of a five-level single-phase inverter with flying-capacitor topology associated with Fig. 1(b) are given in Table I.

It is required that capacitors' voltages are kept around V_{dc} while they are charged or discharged when the load current passes through the capacitors. Thus, the objective is to balance the capacitors' voltages with minimum switching losses while achieving current tracking during operation.

Fig. 5 shows all voltage vectors of a single-phase five-level inverter with flying-capacitor topology at different voltage levels, associated with Fig. 1(b). Moving from one voltage level to another with one switch change can be achieved such that the capacitor voltage can be balanced. The "on" and "off" switching states of each switch are defined as 1 and 0, respectively. For example, (1100) means that $S_1 = 1$ (on), $S_2 = 1$ (on), $S_3 = 0$ (off), and $S_4 = 0$ (off).

The load current does not pass through the capacitors for the four switching states (1100); (0011); (1111); (0000). Thus, the rest of the switching states are associated with the load current changing the capacitors' voltages. The controller has to determine the adjacent voltage vector to improve the capacitor voltage during the next switching state.

Suppose the output voltage is zero using the switching state (0000) and the load current crosses the lower band. In this case, the output voltage has to be increased one level in order to increase the load current. The switching states with adjacent voltage vectors give two alternative states (0100) and (1000) which are associated with the voltage across the capacitor in phase "a," V_{ca}. If V_{ca} has to be changed and the load current is positive, the switching states (1000) or (0100) will charge or discharge the capacitor of phase "a," respectively, as shown in Fig. 6. Indeed, at three of the voltage levels, V_{dc}, 0, and $-V_{dc}$, the capacitor voltages V_{ca} and V_{cb}, can be changed in any desired direction using the correct switching states. Thus, in addition to the hysteresis current control technique for control of the load current, the controller uses the correct switching state at

TABLE I
SWITCHING STATES OF A FIVE-LEVEL SINGLE-PHASE INVERTER WITH CHARGING AND DISCHARGING STATES OF FLYING-CAPACITORS

S1	S_2	S_3	S_4	V_{out}	V_{ca} for i>0	V_{cb} for i>0
1	1	0	0	$2V_{dc}$	No change	No change
1	1	0	1	V_{dc}	No change	Increase
1	1	1	0	V_{dc}	No change	Decrease
1	0	0	0	V_{dc}	Increase	No change
0	1	0	0	V_{dc}	Decrease	No change
0	1	0	1	0	Decrease	Increase
0	1	1	0	0	Decrease	Decrease
1	0	0	1	0	Increase	Increase
1	0	1	0	0	Increase	Decrease
0	0	0	0	0	No change	No change
1	1	1	1	0	No change	No change
0	0	0	1	$-V_{dc}$	No change	Increase
0	0	1	0	$-V_{dc}$	No change	Decrease
0	1	1	1	$-V_{dc}$	Decrease	No change
1	0	1	1	$-V_{dc}$	Increase	No change
0	0	1	1	$-2V_{dc}$	No change	No change

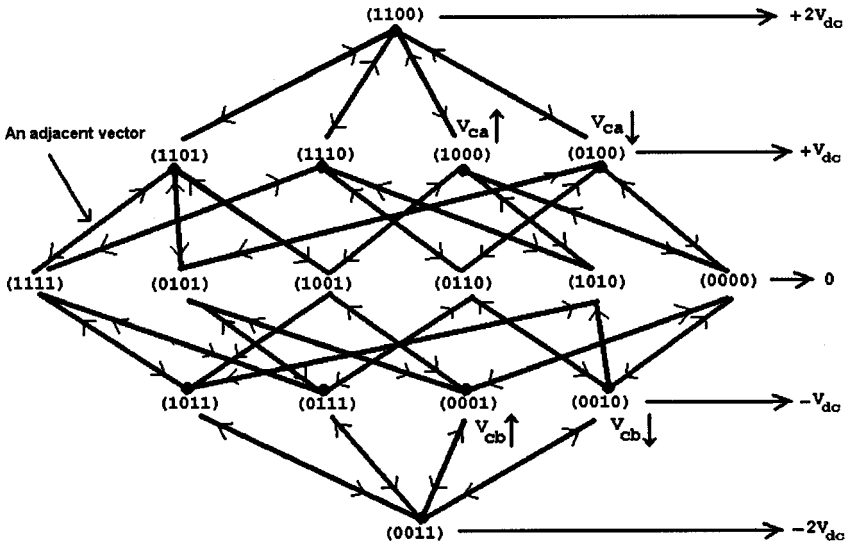

Fig. 5. Switching states of a single-phase five-level inverter with flying-capacitor topology with adjacent voltage vectors.

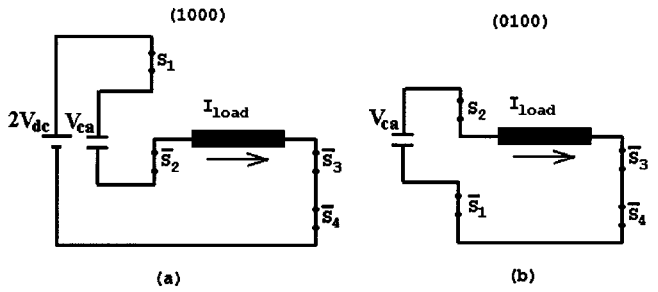

Fig. 6. Capacitor voltage at switching times. (a) Charging state. (b) Discharging state.

each switching time using the state transition technique in order to improve the capacitor voltage with adjacent voltage vectors.

IV. SIMPLE STRUCTURE OF A SINGLE-PHASE MULTILEVEL INVERTER

Fig. 1(b) shows a single-phase five-level inverter with flying capacitor topology which consists of two similar legs with two capacitors. All switching states with the adjacent voltage vectors between each two switching states have been given in Table I and Fig. 5. Another alternative case is to use a simple structure of a single-phase five-level inverter as shown in Fig. 7. This single-phase inverter has a multilevel structure's leg and a traditional structure's leg. This circuit has eight switching states as given in Table II. It is clear that five voltage levels can be generated by this structure and the capacitor voltage can be controlled when the output voltage is V_{dc} or $-V_{dc}$. This is a basic illustration of

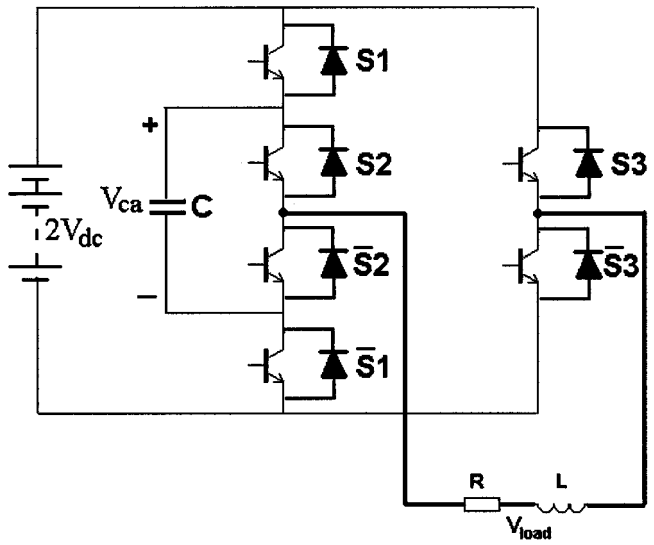

Fig. 7. A simple structure for a single-phase five-level inverter with flying capacitor topology.

TABLE II
SWITCHING STATES ASSOCIATED WITH A SIMPLE STRUCTURE OF A FIVE-LEVEL SINGLE-PHASE INVERTER WITH FLYING-CAPACITORS

S1	S_2	S_3	V_{out}	V_{ca} for i>0
1	1	0	$2V_{dc}$	No change
1	0	0	V_{dc}	Increase
0	1	0	V_{dc}	Decrease
0	0	0	0	No change
1	1	1	0	No change
0	1	1	$-V_{dc}$	Decrease
1	0	1	$-V_{dc}$	Increase
0	0	1	$-2V_{dc}$	No change

the multilevel inverter with the low number of the components and tools extendible to more legs and levels.

A disadvantage of this structure is the lack of adjacency when the switching transitions occurs from zero voltage level toward the negative or the positive voltage levels. Suppose the output voltage is $+2V_{dc}$ using (110) and the controller is required to decrease the output voltage based on the derivative of the load current. The adjacent voltage vectors exist between the positive voltage levels, V_{dc}, (100) and (010). Thus, the capacitor voltage can be controlled at $+V_{dc}$ voltage level based on the load current using adjacent voltage vectors. When the output voltage reaches zero, there is no adjacent voltage vector to approach the negative voltage level $-V_{dc}$. This is a constraint due to the simple structure. The required nonadjacent switching transitions are unidirectional between the following switching states and are shown in Fig. 8 by dash lines:

- (000) to (101);
- (000) to (011).

Each of these transitions requires two switch changes. After the transition occurs from the zero voltage level (000) to $-V_{dc}$ voltage levels (101) or (011), then the controller uses (111) for the modulation between the zero and $-V_{dc}$ voltage levels.

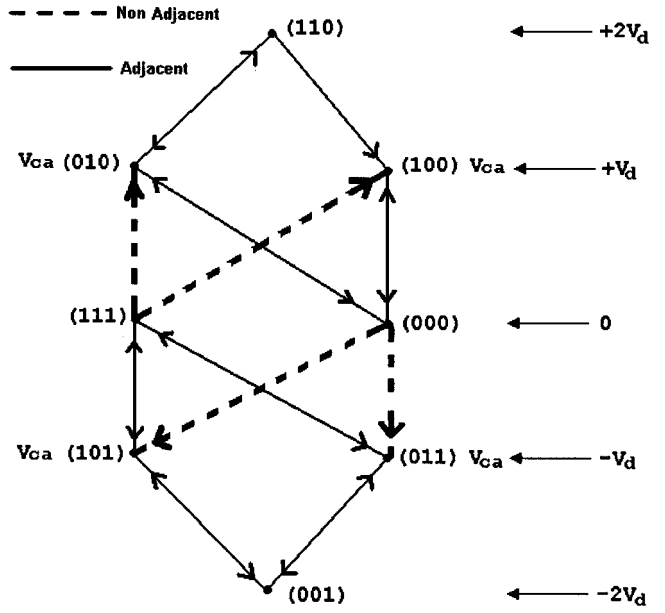

Fig. 8. Switching states of a simple structure of a single-phase five-level inverter with flying-capacitor topology.

The equivalent situation happens when the output voltage is negative and the controller increases the output voltage. For this case, the unidirectional switching transitions areS

- (111) to (010);
- (111) to (100).

These unidirectional switching transitions occur just two times in each cycle, from zero voltage level to negative or positive voltage levels and the switching losses will not be changed significantly.

V. PLD IMPLEMENTATION OF CURRENT CONTROLLER

For this multilevel inverter, the hysteresis current controller is required to generate a sinusoidal current waveform and also control the capacitor voltage using adjacent voltage vectors. The use of adjacent vectors minimizes the number of switchings. Figs. 5 and 6 show a state transition where the next switching state is achieved based on the last switching state, capacitor voltage level, load current and adjacent voltage vectors. The hardware section of the hysteresis current controller based on magnitude and time errors only consists of the main zone with upper and lower bands. The load current can be increased or decreased by changing the output voltage whenever the load current reaches the upper or the lower bands similar to the traditional hysteresis current control. A resetable timer will be activated whenever the load current hits the upper or the lower bands and it will be disabled when the load current moves to the main zone. For example, if the load current reaches the first upper band and moves out of the main zone, the controller decreases the output voltage one level and the timer starts to count. If the load current still is out of the main zone after the time error period, E_t, the output voltage is decreased one level more and the timer is reset and continues to count. Thus, the timer can work to change the

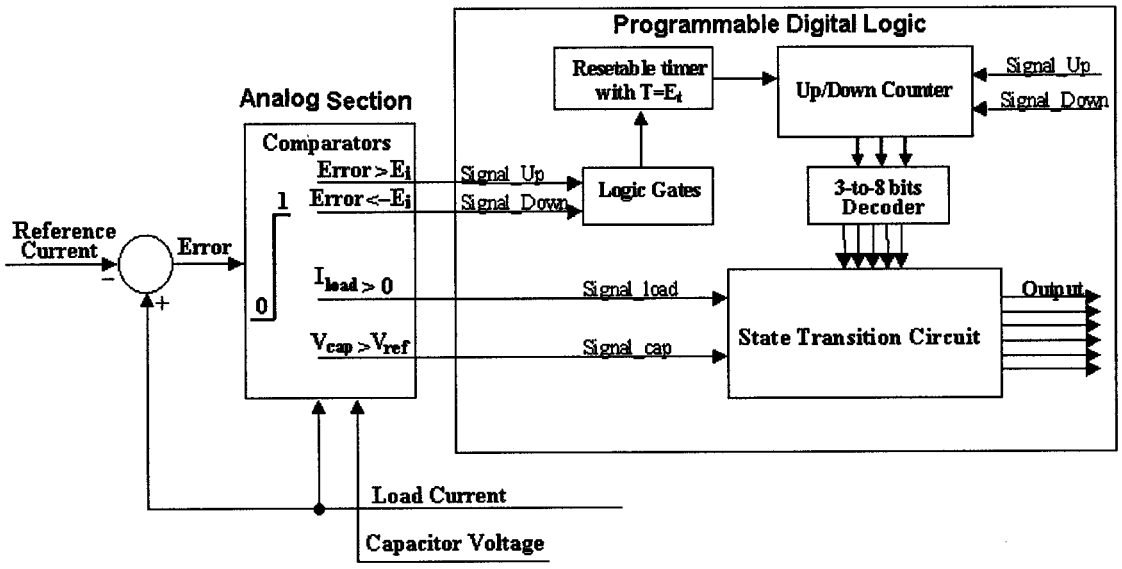

Fig. 9. Circuit diagram of the hysteresis current control for five-level inverter with flying-capacitor topology.

bands when the load current leaves the main zone. The control section of the hysteresis current control does not need several comparators with different reference voltages in order to detect the location of the load current in each band.

Fig. 9 shows a circuit diagram of the current controller for a single-phase five level inverter with flying-capacitor topology. The first block is an analog circuit consisting of four comparators. The current error is compared with two levels, $+E_i$ and $-E_i$, which are associated with the upper and lower bands, respectively. Using Fig. 8, the charging or the discharging states of the capacitor voltage can be selected by signals, which are a function of the capacitor voltage level and the load current direction. Thus, one bit is defined for capacitor voltage based on whether the voltage is above or below the reference value (V_{dc}) and another bit for the load current when the current is positive or negative. These signals are connected to the digital section.

The state transition and the logic circuits can be used for other types of the current controllers such as a predictive current control to balance the capacitor voltage and to map the switching states using adjacent voltage vectors.

EPM7128S PLD from MAX7000 family, with high-performance and EEPROM structure have been used for the hardware section. As shown in Fig. 9, an up/down counter increments or decrements the output voltage whenever the load current hits the bands. Signal_up and signal-down can set the counter in the up-count or the down-count modes, respectively. A resetable timer is activated when the load current leaves the main zone. The clock cycle of the timer is determined by (5) associated with the time error period, E_t. The output of the counter is connected to a decoder to determine the output voltage level after level change. At two voltage levels, $+V_{dc}$, $-V_{dc}$, there are some switching states which are associated with the charging or the discharging of the capacitor voltages based on the load current as shown in Fig. 8. The state transition technique is required to achieve the switching state using adjacent voltage vectors.

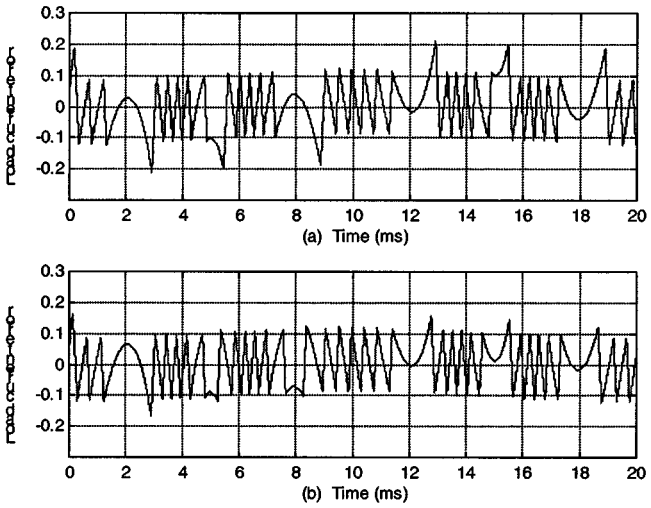

Fig. 10. (a) Magnitude of current error for hysteresis current control based on magnitude error. (b) Magnitude of current error for hysteresis current control based on magnitude and time errors.

The state transition circuit has the following inputs:

- *three signals associated with three-voltage level $+V_{dc}$, 0, $-V_{dc}$;*
- *signal_cap which identifies the capacitor voltage*;
- *signal_load which shows the sign of the load current.*

In the state transition circuit, type D flip-flops can save the switching states for decision at the next switching time.

VI. Simulations and Experimental Results

A comparison between the hysteresis current control based on magnitude error and the hysteresis current control based on magnitude and time errors have been carried out using Matlab as shown in Fig. 10. The results show that the magnitude of the current error is decreased by the hysteresis current control

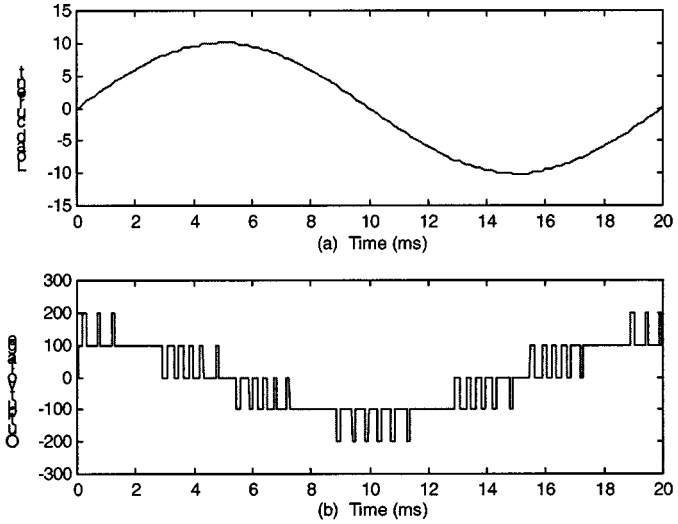

Fig. 11. Simulation results for five level inverter. (a) Load current. (b) Output voltage.

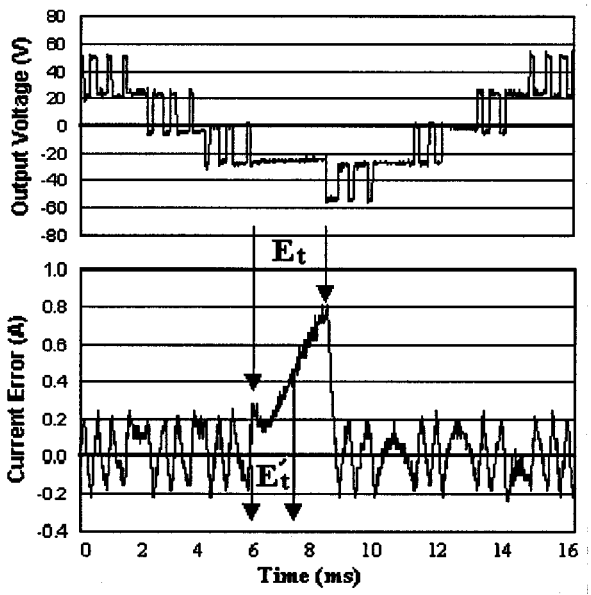

Fig. 12. Experimental result of output voltage and current error for a big value of time error period E_t.

based on magnitude and time errors and also it is more robust for implementation. Increasing the load inductance would slow the current transitions in both directions and hence reduce switch frequency while the presence of back emf would, at one instant of time, tend to make one direction of current transition faster and the other direction slower.

Fig. 11 shows the simulation result of the output voltage and the load current. It is clear that the load current follows the reference current with low distortion.

Experiments have been performed based on the simple structure of the single-phase five-level inverter with an RL load The presence of back emf would serve to create more variation in the switching frequency but without affecting the nature of the error trajectory. To describe the time error technique, $E_t = 2.6$ ms has been achieved with a large time interval value and the result is shown in Fig. 12. The voltage level change occurs whenever the load current tries to pass the bands. As shown in Fig. 12, the load

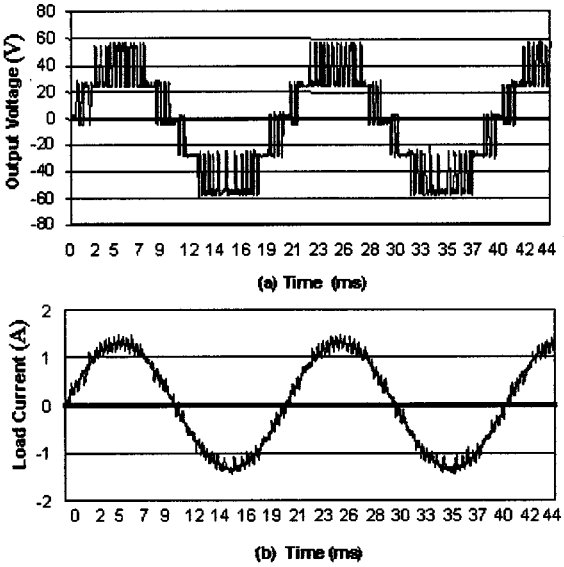

Fig. 13. Experimental results of a single phase five-level inverter. (a) Output voltage. (b) Load currents.

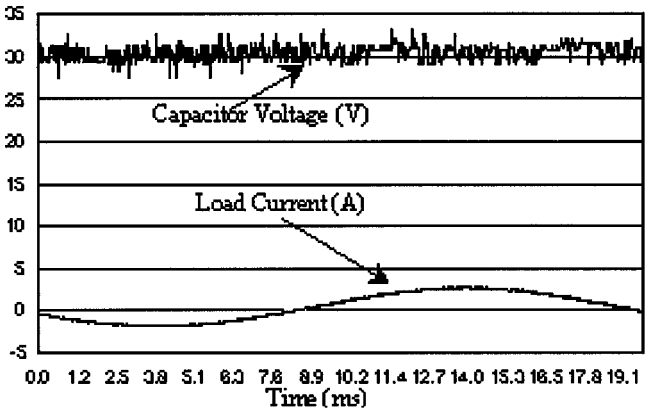

Fig. 14. Experimental result of capacitor voltage during operation.

current reached the upper band and the controller decreased the output voltage from 0 to $-V_{dc}$. The load current still is out of the main zone and the controller waits for the time error period, E_t and then the output voltage is changed one level more from $-V_{dc}$ to $-2V_{dc}$ in order to increase the derivative of the load current. Note: In this example, the time error period, E_t, was achieved with a large time interval value to identify the control technique but for normal operation, the time error period, E_t, has to be based on (5) in order to minimize the current error. For example, if the time error period, E_t' is achieved based on (5), the current error will be much less as shown in Fig. 12.

Fig. 13 shows the output voltage and the load current for normal operation of the controller. The upper and the lower band size achieved is 200 mA and the dc bus voltage is 60 V. The reference current is a sinusoidal waveform with $f = 50$ Hz and $I_{\max} = 1.3$ A.

Another important objective is to control the capacitor voltage during operation. As it was described before, the controller can achieve the correct switching states based on the load current when the output voltage is $+V_{dc}$ or $-V_{dc}$. Fig. 14 shows the voltage across the capacitor and the load current for normal operation. The capacitor was charged and discharged

during operation and the results show that the capacitor voltage level is reliably controlled.

VII. Conclusions

Multilevel inverters provide an attractive solution for power electronics when both reduced harmonic content and high power are required. The hysteresis current control technique for the multilevel inverter is more complex than the traditional inverter control due to more voltage levels. In this paper, a hysteresis current control technique for a single-phase inverter with flying-capacitor topology is proposed. Level, band, and switching state are based on time out, hysteresis, and capacitor voltage balancing, respectively. This method incorporates a technique to improve the performance of the controller using adjacent voltage vectors in order to minimize the switching losses. Thus, this technique can be applied to the multilevel inverter with different current control techniques such as predictive current control to address the balancing of capacitor voltage with minimum switching losses. The simulation and experimental results describe and verify the current control technique for the inverter.

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