Efficient digital single-bit resonator

A.C. Thompson, Z.M. Hussain and P. O'Shea

An all-digital single-bit resonator is presented. The resonator input can be either a single-bit or multi-bit signal and the resonator output is in single-bit format. This resonator structure contains no multi-bit multiplication operations, making the resonator efficient for implementation.

Introduction: Single-bit processing has been attracting interest due to the promise of efficient and simple implementations [1, 2]. One area where little work can be found is in single-bit resonators. Resonators are typically used to filter narrow bandwidth signals. A typical resonator is implemented using a multi-bit architecture and, as such, it produces multi-bit output [3]. In this Letter we propose a resonator structure that produces a single-bit output.

Structure: The structure of the single-bit resonator consists of a standard second-order resonator with a bandpass sigma-delta modulator (ΣΔM) embedded in the loop. The standard second-order resonator has a centre frequency f_c that is equal to one quarter of the sampling frequency f_s. The delay in the standard resonator is replaced with a bandpass ΣΔM. This modulator not only acts as a delay element but also remodulates the input signal to the single-bit format. Essentially this second-order resonator system behaves as if the modulator were two simple delays z^{-2}. The structure of the proposed single-bit resonator is shown in Fig. 1.

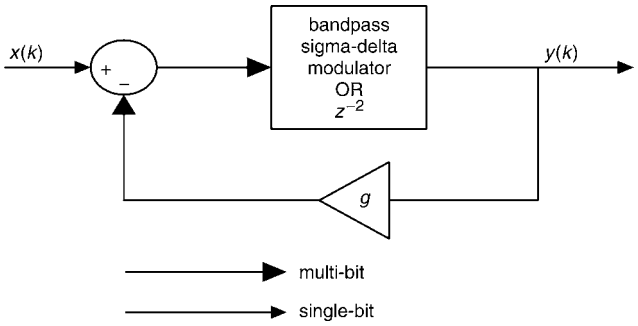

Fig. 1 *Block diagram of proposed second-order single-bit resonator*

As a direct result of remodulation the new resonator contains no multi-bit multiplications. This considerably reduces the implementation complexity as multi-bit multiplication operations require highly clocked circuits and many thousands of gates. The gain factor g in the feedback path, shown in Fig. 1, can be implemented with a simple multiplexer. This reduction in implementation complexity also extends to the input summing node. Given that the input to the resonator is in a single-bit format, the summer can be implemented with a simple four-element lookup table. This further reduces the hardware complexity and also lends itself to efficient field programmable gate arrays (FPGA) implementation.

The choice of bandpass digital ΣΔM used in the single-bit resonator structure in Fig. 1 is limited to those that have only two delay elements in their forward path and a noise shaping centre frequency of $f_s/4$. The bandpass double-loop ΣΔM is such a modulator [4]. The block diagram of this modulator is shown in Fig. 2.

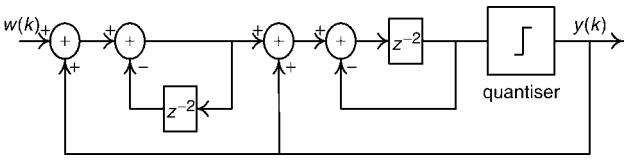

Fig. 2 *Block diagram of double loop bandpass ΣΔM*

The implementation efficiency of this single-bit resonator can be improved further by combining the gain multiplexer and the input summing node multiplexer. The final single-bit resonator system can then be implemented with only a simple two-input lookup table and a bandpass ΣΔM. This enables efficient implementation, particularly in FPGA.

The signal and noise transfer functions (denoted as STF and NTF, respectively) of this single-bit resonator can be described by:

$$STF = \frac{z^{-2}}{1 + gz^{-2}} \tag{1}$$

and

$$NTF = \frac{1 + 2z^{-2} + z^{-4}}{1 + gz^{-2}} \tag{2}$$

where g is the feedback gain shown in Fig. 1.

This gain element has some control over the bandwidth of the single-bit resonator. If we consider the ΣΔM to behave as a double delay, then the system reduces to a simple second-order resonator. The value of the feedback gain controls the pole locations and as such the stopband attenuations and 3 dB bandwidths. We would expect the stopband attenuation to improve as $g \rightarrow 1$ [3].

The stability of the proposed single-bit resonator is an important issue as a ΣΔM is present in the system. The double-loop bandpass ΣΔM is derived from its lowpass counterpart by virtue of the transformation $z \rightarrow -z^{-2}$. The transformation of the lowpass double-loop ΣΔM preserves the modulator's dynamics, and hence stability properties [4]. Since the double-loop ΣΔM is generally considered as stable [4], we can assume that the bandpass double-loop ΣΔM behaves as a stable element in the system. The system stability as an entire unit still requires further investigation. However, we have found that the system stability is similar to that of the second-order multi-bit resonator.

Future work will involve a comprehensive stability analysis, efficient FPGA resonator implementation and an investigation into higher-order single-bit resonator structures.

Simulation results: To illustrate the capabilities of the proposed single-bit resonator, simulations with feedback gain values of $g = 0.99$, 0.999 and 0.9999 are presented. A white Gaussian noise signal was input to the resonator. The resulting data at the resonator output were recorded. A 32768 point fast Fourier transform (FFT) of this output was performed and recorded for every value of the gain g. An estimate of the resonator's frequency response was calculated by taking the average of the FFTs for 1000 realisations. The results are shown in Fig. 3.

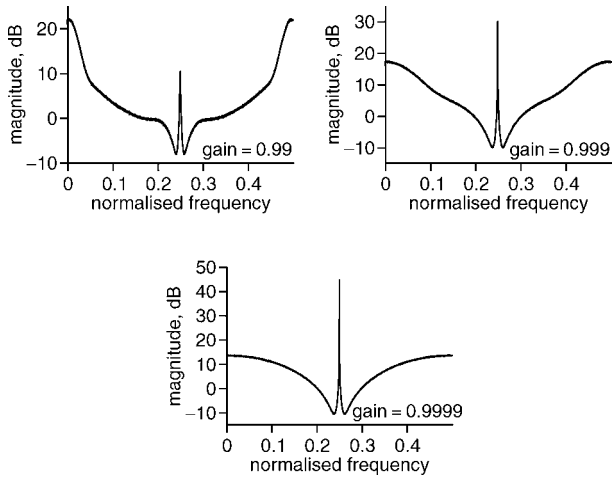

Fig. 3 *Resonator frequency responses with feedback gains of 0.99, 0.999 and 0.9999*

The graphs in Fig. 3 show that the system behaves like a resonator. As expected, increasing the feedback gain improves the bandpass filtering stopband attenuation. However, as the feedback gain increases, the 3 dB bandwidth decreases.

Overall, the simulated system produced stopband attenuations of 18.3, 39.8 and 55 dB with 3 dB bandwidths of 0.0015, 0.00017 and 0.00005 f_s at gains of 0.99, 0.999 and 0.9999, respectively. Gain values of $0.95 < g < 1$ were found to provide stable results. A feedback gain of 1.0 produced oscillation at $f_s/4$, hence, the resonator would behave like

a single-bit oscillator. Feedback gain values greater than 1.0 tended to produce unstable results.

Conclusion: A digital single-bit resonator is proposed. This resonator can accept either multi-bit or single-bit input words and produces a single-bit output. The system is implementation efficient as it contains no multi-bit multiplications. It consists only of a multiplexer and a bandpass ΣΔM. Simulations showed that the feedback gain has some control over the resonator's stopband attenuation and the 3 dB bandwidth.

25 June 2004
Electronics Letters online no: 20045803
doi: 10.1049/el:20045803

A.C. Thompson and Z.M. Hussain (*School of Electrical and Computer Engineering, RMIT University, Melbourne, Victoria 3000, Australia*)

E-mail: zmhussain@ieee.org

P. O'Shea (*School of Electrical and Electronic Systems Engineering, Queensland University of Technology, Brisbane, Queensland 4000, Australia*)

References

1 Fujisaka, H., Kurata, R., Sakamoto, M., and Morisue, M.: 'Bit-stream signal processing and its application to communication systems', *IEE Proc., Circuits Devices Syst.*, 2002, **149**, (3), pp. 159–166
2 Thompson, A.C., O'Shea, P., Hussain, Z.M., and Steele, B.R.: 'Efficient single-bit ternary digital filtering using sigma-delta modulator', *IEEE Signal Process. Lett.*, 2004, **11**, (2), pp. 164–166
3 Proakis, J.G., and Manolakis, D.G.: 'Digital signal processing principles, algorithms, and applications' (Prentice-Hall, Englewood Cliffs, NJ, USA, 1996, 3rd edn.)
4 Norsworthy, S.R., Schreier, R., and Temes, G.C. (Eds.): 'Delta-sigma data converters: theory, design, and simulation' (IEEE Press, New York, USA, 1997)