Enabling large focal plane arrays through mosaic hybridization

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ABSTRACT

We have demonstrated advances in mosaic hybridization that will enable very large format far-infrared detectors. Specifically we have produced electrical detector models via mosaic hybridization yielding superconducting circuit paths by hybridizing separately fabricated sub-units onto a single detector unit. The detector model was made on a 100mm diameter wafer while four model readout quadrant chips were made from a separate 100mm wafer. The individually fabricated parts were hybridized using a Suss FC150 flip chip bonder to assemble the detector-readout stack. Once all of the hybridized readouts were in place, a single, large and thick silicon substrate was placed on the stack and attached with permanent epoxy to provide strength and a Coefficient of Thermal Expansion match to the silicon components underneath. Wirebond pads on the readout chips connect circuits to warm readout electronics; and were used to validate the successful superconducting electrical interconnection of the model mosaic-hybrid detector. This demonstration is directly scalable to 150 mm diameter wafers, enabling pixel areas over ten times the area currently available.

Keywords: Superconducting Indium Hybridization, Large Focal Plane, Mosaic Bolometer Array

1. INTRODUCTION

The next generation of large-scale science experiments studying the universe will require large format detector arrays containing tens of thousands of pixels [1]. These studies will likely include CMB polarization, general evolution of large-scale structure in the universe and other astrophysical phenomena, requiring large focal planes as well as background-limited detector arrays. Currently, there is no existing detector for wavelengths longer than 40μm that can meet these science goals. Recognizing this fact and in preparation for the New Worlds, New Horizons (NWNH) decadal survey in astronomy and astrophysics by the National Research Council, a large community of scientists submitted a white paper with clear recommendations, including the need for novel detector array technologies with an order of magnitude or more increase in the format available today [2].

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2.1 Fabrication

The detector array is made from a 100mm diameter single crystal silicon wafer. The part of the circuit on the detector is comprised of a single layer of d.c. sputtered molybdenum nitride (Mo_2N) and is patterned on the bottom side of the wafer such that it simply acts to short out the circuit from the substrate. This layer is also patterned to receive the indium bumps from the substrate, including the electrically active bumps and those that are purely for mechanical strength and thermal conduction. This material was chosen as the landing-pad-metal primarily because it is a superconductor with a relatively high transition temperature, about 7 Kelvin. Also, molybdenum nitride has a stable surface morphology and is a well-known diffusion barrier [7]. To define the detector geometry we use deep reactive ion etching (DRIE) to transfer a pattern completely through the wafer. This pattern defines the outer frame of the detector as well as each "pixel." A pixel in this sense is a cavity on a pitch of approximately 1 mm, having walls 60 μm wide between pixels. The detector model is an array of 32 x 40 of these pixels with the perimeter frame ranging from slightly more than half a millimeter to slightly more than one millimeter wide. The patterned molybdenum nitride resides on the walls between each pixel as well as all along the frame of the detector.

A full set of readout quadrant chips are fabricated on a single 100 mm diameter single crystal silicon wafer. Prior to any metallization, an insulating layer of 2000Å of SiO2 is grown on the wafers. The circuit traces that run from edge bond pads to pixel locations are the same type of molybdenum nitride used on the detector, and for similar reasons. This single layer also acts as the under-bump-metal. On top of the UBM and patterned to match up with the LPM, 10 μm of indium is deposited in a lift-off process. There is a "forest" of indium bumps that run around the perimeter of the detector footprint whose primary role is mechanical strength and thermal conduction. This forest however prevents a wiring fan-out to all pixels. Consequently only 64 pixels of 1280 are capable of being readout with this model. The completed substrate is then diced and prepared for hybridization.

2.2 Plasma Cleaning

Standard metallization processes often employ in situ cleaning steps under vacuum conditions that enhance the adhesion or electrical contact between metallic layers. We employ this technique when depositing the indium on top of the molybdenum nitride on the substrate or UBM. However, when the substrate is hybridized to the detector, the indium on the substrate essentially cold-welds to the molybdenum nitride on the detector. This process is done in a cleanroom, in air, and it is not possible to do any further processing of the parts while they are on the tool that bonds them together.

When exposed to air at room temperature, indium will readily oxidize, forming a thin "crust" of In_2O_3. This layer of indium oxide can result in two problems, the first being poor adhesion to the LPM. The forces from bonding can rupture a surface film, thereby allowing indium to contact the LPM resulting in good adhesion, however In_2O_3 tends to resist rupturing. The second problem is that In_2O_3 can prevent a barrier to electrical conduction and inhibit a superconducting joint. In fact In_2O_3 has been shown to exhibit a superconductor-insulator-transition effect [8], although being such a thin surface film, will present a very low critical current.

To overcome these limitations we plasma clean each chip just prior to hybridization using a March CS-1701 plasma cleaning system. For the substrates, we apply r.f. power to a nitrogen-rich, reducing gas mixture. The plasma has the effect to reduce the indium-oxide, which is then replaced by indium-nitride in a self-limiting process. The indium nitride ruptures more readily than the In_2O_3 and enables a good electrical joint between the indium and the LPM. If the indium surface is merely reduced, an oxide will re-grow as soon as the chip is removed from vacuum. The indium nitride layer inhibits this growth allowing for time to complete the hybridization process.

To develop our plasma clean on the indium we used ellipsometry to track the surface film on the indium. We did not calculate thickness directly, but merely tracked the Delta for each measurement. Delta is a simple calculation based on the polarization angles specific to a film and its substrate. It is used to make a measurement of thickness or index of refraction in conjunction with other measurements. As it is directly proportional to thickness, it is a good indicator by itself of the film and when measuring native oxide on indium, the lower the value of Delta, the thicker the In_2O_3 film. In Figure 2 we look at a sample of untreated indium alongside a sample of indium that has received the plasma treatment, and track them both over a long period of time. You can see that the untreated sample has a Delta value that is about 128, which corresponds to the native In_2O_3, and stays at this value over time. The plasma treated sample, however, has a large increase in Delta just after plasma treatment indicating that we have removed the native oxide. Initially, the Delta of this sample drops a little due to removing the sample from the vacuum chamber, as oxygen will attach to indium
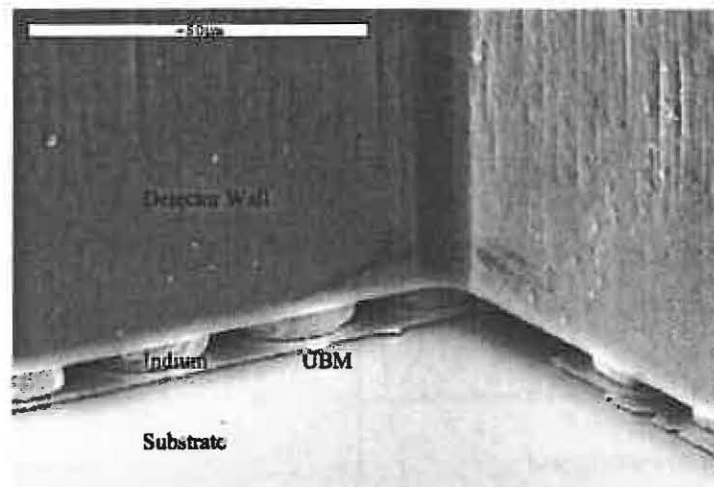
Figure 3. Scanning Electron Microscopy image post hybridization. The view shows a close-up of one corner of a pixel. Visible in the image are the detector wall, substrate with under-bump-metal (UBM) and the indium itself after approximately 50% deformation. Not visible due to the angle, is the landing-pad-metal (LPM).

The hybridization plan for a single completed part is an involved process. Overall, five alignments and thermocompression cycles are needed to make a finished part. The process starts off with aligning the detector array on a custom vacuum plate designed to hold a large array while transmitting the force through the detector walls. This custom part is also designed to handle detector arrays with membranes [10]. The readout quadrants are then hybridized one at a time to build up the mosaic. When all of the quadrants are in place, one more piece of silicon is glued to the stack. This solid piece ties all the quadrants together for rigidity. The FC 150 is used for this step to ensure alignment and control the epoxy gap, as well as to cure the epoxy. The gap between the quadrants after hybridization is equivalent to the width of the dicing saw that cuts the substrate after fabrication, which is about 200μm.

2.4 Cold Testing

After hybridization the parts are mounted and wire-bonded in a package for cold testing. We are able to wire-bond directly to the molybdenum nitride on the substrate. A successful circuit needs to prove superconducting with adequate critical current in order to be useful and considered successful. To get to the needed temperatures, a simple dewar was used that allowed for pumping on a liquid helium bath. The package was lowered directly into the liquid helium. A Linear Research bridge was used to measure the resistance of each channel connected, while temperature was monitored using a Lakeshore bridge. Data was recorded using Labview software. Using a 4-wire measurement configuration each channel was monitored to see that it went to the lowest reading of the bridge, which corresponded to a value of 0.01mΩ, this value was taken to indicate a superconducting circuit.

3. RESULTS

Electrically, we have proven a superconducting path from the under-bump-metal, to the indium bumps, to the landing-pad-metal and back to the substrate via a completely new path. Figure 4 shows representative data for the metal systems comprising the circuit of a mosaic hybrid. The superconducting transition of the molybdenum nitride at 6.8 Kelvin is consistent with Mo_2N [11]. Also shown in Figure 4 is the superconducting transition of the indium at 3.4 Kelvin, which is consistent with bulk indium [12]. The data shown in Figure 4 were taken at a measurement range of 2Ω and an excitation of 2mV indicating a critical current of at least 1mA, sufficient for our PIPER project as well as future missions. This data indicates that we have successfully made a superconducting cold-weld between the indium and the LPM, as well as the indium-molybdenum nitride joint on the substrate or UBM. The plasma cleaning process on large-format-arrays produced from the mosaic build process have yielded a successful pixel rate of 91% of testable channels. The failure rate is confined to the corners of the array, which are thought to be due to non-uniform plasma over large areas. This limitation can easily be overcome with a more uniform reactive ion etching system.
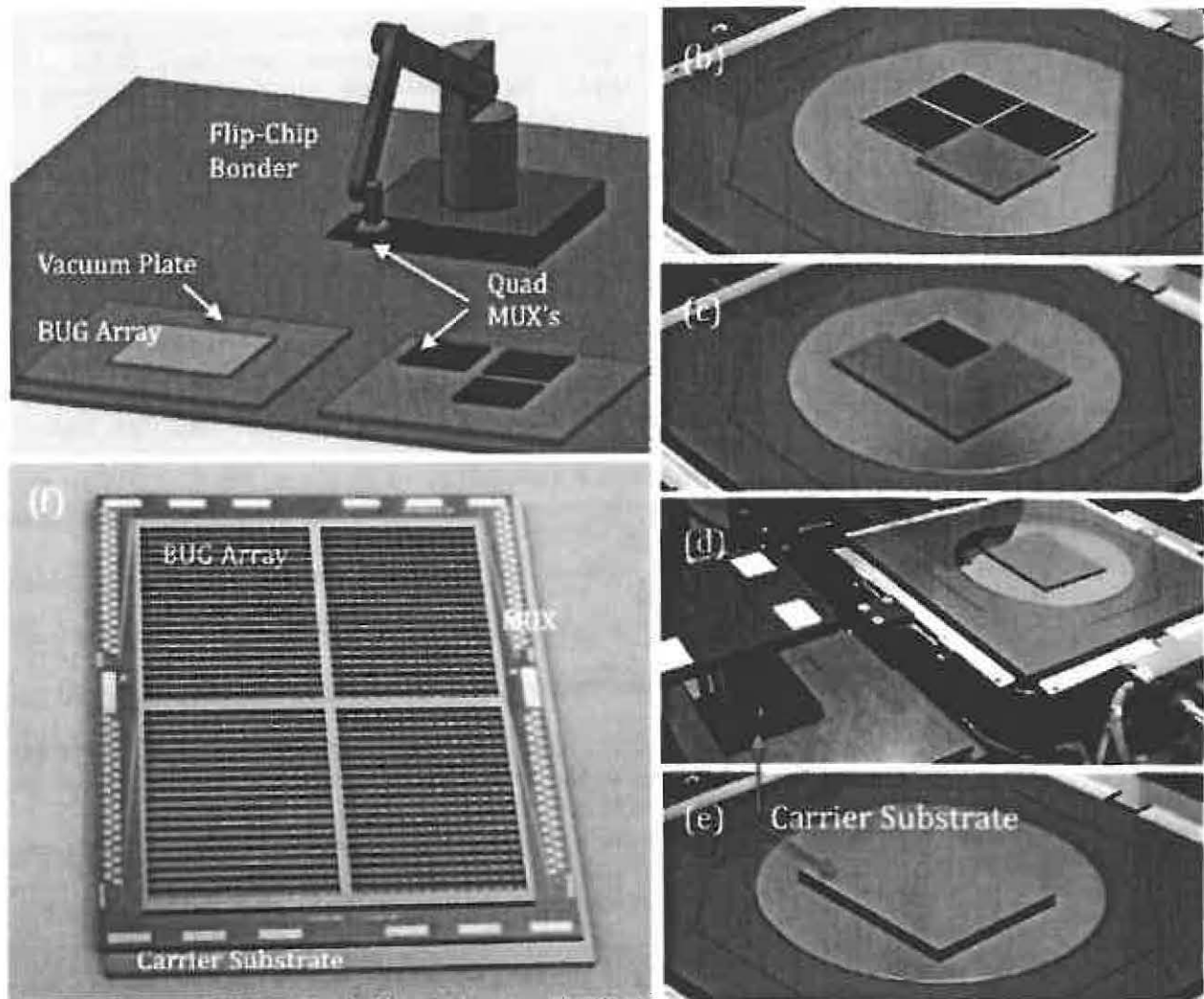
Figure 5. The sequence above illustrates the mosaic build process. (a) is a sketch of the assembly process, showing how the FC150 arm picks and places mosaic quadrants of readout chips onto a single BUG array, oriented facedown, hybridizing with indium bump bonds between each component. Images (b) – (d) are photographs taken of parts on the FC150 vacuum chuck during the assembly process. These show the population of the BUG array with readout quadrants (smaller rectangles). Image (e) shows the final placement of a carrier substrate on top of the readout quadrants, which provides strength to hold the assembly together. At the lower left is a photograph of the front-side of the stack showing the readout quads (with edge wire-bond pads) and the singular detector grid on top. The cross in the grid is solid silicon, one pixel width, used to provide area for indium bumps to hold the quadrants together.

4. SUMMARY

We report a hybridization scheme that will enable large format detectors which utilizes an effective plasma cleaning process for the hybridized parts. The plasma cleaning process has been shown to consistently prepare the indium surface for hybridization. The plasma process also passivates the surface in a way that allows for the indium to sit in air during the hybridization loading and alignment steps, which can take considerable time. This process yielded superconducting circuits with high critical currents, of at least 1mA.

With this mosaic hybridization technology, current detectors can be readily scaled up with only a few design changes. Our demonstration showed that we can tile current sized arrays to build even larger mosaic arrays. We built a mosaic detector and readout quadrants fabricated on 100mm diameter wafers, however this technology is directly scalable to 150mm wafers. In this scenario, the readout quadrants could be the size of the single MUX used for PIPER, while the detector could be produced on a 150mm wafer. The hybridization scheme along with the plasma cleaning is compatible