Fabrication of Silicon Backshorts with Improved Out-of-Band Rejection for Waveguide-Coupled Superconducting Detectors

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Abstract— The Cosmology Large Angular Scale Surveyor (CLASS) is a ground-based instrument that will measure the polarization of the cosmic microwave background to search for gravitational waves from a posited epoch of inflation early in the universe's history. This measurement will require integration of superconducting transition-edge sensors with microwave waveguide inputs with good control of systematic errors, such as unwanted coupling to stray signals at frequencies outside of a precisely defined microwave band. To address these needs we will present work on the fabrication of silicon quarter-wave backshorts for the CLASS 40GHz focal plane. The 40GHz backshort consists of three degeneratively doped silicon wafers. Two spacer wafers are micromachined with through wafer vias to provide a 2.04mm long square waveguide. The third wafer acts as the backshort cap. The three wafers are bonded at the wafer level by Au-Au thermal compression bonding then aligned and flip chip bonded to the CLASS detector at the chip level. The micromachining techniques used have been optimized to create high aspect ratio waveguides, silicon pillars, and relief trenches with the goal of providing improved out of band signal rejection. We will discuss the fabrication of integrated CLASS superconducting detectors with silicon quarter wave backshorts and present current measurement results.

Index Terms—Superconducting microstrip, transition edge sensors, deep reactive ion etching, wafer bonding. surface roughness

I. INTRODUCTION

Gravitational waves produced during inflation create a unique polarization pattern on the cosmic microwave background (CMB). This signature offers an important tool with which to investigate the high-energy physics of the inflationary epoch of the early Universe. The discovery of this signature will provide the first direct evidence for inflation and will rule out most competing explanations for the initial conditions of the Universe. Characterization of this signal offers a way to explore the first 10^{-32} seconds of the Universe. The polarized signal from inflation is anticipated to be 10^{-9} of the 2.725 K isotropic CMB. Thus for an instrument to be successful in measuring this signal it must have (1) the requisite sensitivity, (2) excellent control over systematic errors in measurement, and (3) multiple spectral bands for foreground removal. NASA Goddard Space Flight Center in collaboration with Johns Hopkins University are developing the Cosmology Large Angular Scale Surveyor (CLASS), a ground based telescope designed to search for the polarized divergence free "B-mode" signal in the CMB.

The CLASS instrument takes an innovative approach to address the scientific requirements for measuring the B-mode signal. CLASS will operate at three spectral bands (40, 90 and 150GHz) for foreground removal. Excellent beam control enabled by feedhorns is combined with the sensitivity provided by transition-edge-sensing (TES) bolometers. The sensor integration is enabled via the use of a broad-band planar orthomode transducer (OMT) that symmetrically couples the independent polarizations in the waveguides into separate microstrip lines. The microstrip line for each polarization terminates in a resistor that is thermally coupled to a bolometer. This architecture provides the very powerful advantage of incorporating the band-defining filters into the microstrip circuitry.

A critical enabling component for the CLASS instrument is the detector technology. The CLASS 40GHz detector architecture was described in [1]. The full detector assembly is made up of three parts, a detector chip which consists of planar superconducting microwave antenna and filters along with transition edge sensors which is flip chip bonded to a micromachined silicon quarter wave backshort. This structure is bonded to a silicon interface plate that mates the detector assembly to the focal plane. In a previous paper(REF) we described the fabrication process for the 40GHz CLASS detectors. These fabrication processes are reviewed in section II. In section III we describe the fabrication of the quarter wave backshort. Section IV reviews recent measurements of device performance.

II. FABRICATION

A. Detector chip fabrication

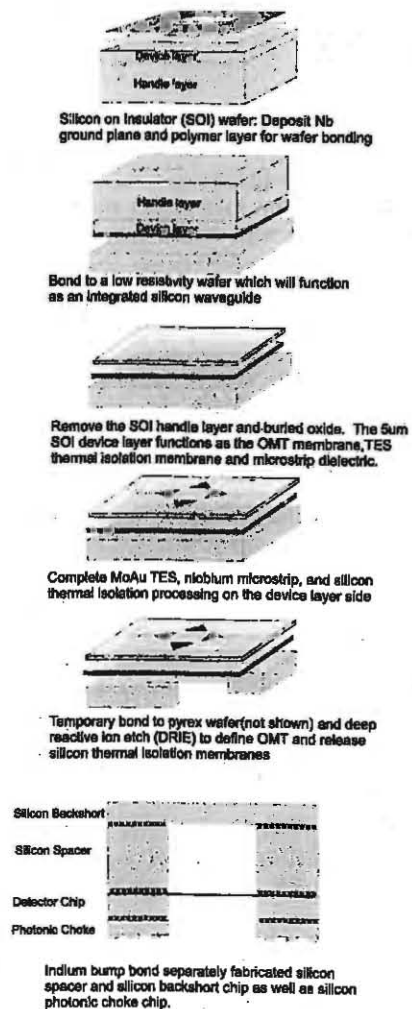Fabrication of the CLASS 40GHz detectors has been described previously in [1]. Here we give a brief overview of

the process. Fabrication begins with a silicon on insulator wafer with a 5um thick device layer and 375um thick handle wafer. The device layer will serve as the microstrip dielectric as well as the thermal link between the leg isolated silicon membranes and the thermal bath. After patterning and etching a niobium ground plane the wafer is bonded to a degeneratively doped silicon wafer with a polymer adhesive. Subsequently the handle wafer is removed from the wafer stack by a plasma dry etching step. This naturally stops on the SOI buried oxide which is removed in buffered HF solution. At this point the wafer resembles a modified SOI wafer where the buried silicon oxide is replaced by the polymer adhesive, the handle wafer is degeneratively doped silicon and the silicon device layer has a buried niobium layer. Subsequent processing follows standard device fabrication since the polymer adhesive, when properly cured is inert in standard micromaching chemicals. Additionally, after the silicon oxide is removed the silicon layer is clean, unroughned and provides an excellent surface for formation of the transition edge sensors.

The next step is deposition and characterization of the transition edge sensors (TES). We use Mo/Au TES consisting of 500A of Mo and 2700A of gold. The deposition is done in a two stage process where the first stage is a sputter deposition of a MoAu seed layer and the second stage is an ebeam deposition of gold to the thickness required to suppress the Mo transition temperature which is typically 900mK to our target of 150mK. The sputtered gold in the seed layer is thick enough to prevent subsequent molybdenum oxidation while not too thick to suppress bilayer Tc significantly. Our seed layers have typical Tc of 700mK. The benefit of this approach is the availability of a batch process where a number of product wafers along with test wafer seed films can be processed at the same time and have similar transmission coupling between the molybdenum and gold. Also, the molybdenum transition temperatures have minimal variation for films deposited in the same vacuum pump down. Gold electron beam depositions are done subsequently after an in-situ surface cleaning on the witness wafers to bracket the bilayer transition as a function of gold thickness prior to committing our product wafers. Electron beam deposited gold gives a higher residual resistivity ratio than room temperature sputtered gold and this can help suppress bilayer Tc for minimal additional gold [2]. We anneal our MoAu bilayers at 150C after deposition to stabilize them against subsequent high temperature processes [3].

The TES gold is patterned and ion mill etched stopping on the molybdenum. Next the niobium microstrip is deposited by sputter deposition. The niobium is then reactive ion etched in a fluorine based plasma in two steps. In the first step for the majority of the microstrip geometry the plasma chemistry is adjusted for a vertical niobium sidewall slope profile. This is to minimize additional microwave loss due to sloped sidewalls. A second lithography step patterns the niobium in areas where it must make contact to other metal layers and this requires a sloped sidewall for good step coverage. The plasma chemistry is adjusted by adding oxygen to the chamber. The

niobium etching is done in a bench top reactive ion etching tool using fluorine and oxygen plasma chemistry. We have found that the etching process roughens the silicon under the niobium upon completion of the etch. We have done a number of experiments to determine the extent of silicon roughening and ways of minimizing it.

Detector Fabrication Process

Silicon on Insulator (SOI) wafer: Deposit Nb ground plane and polymer layer for wafer bonding

Bond to a low resistivity wafer which will function as an integrated silicon waveguide

Remove the SOI handle layer and buried oxide. The 5um SOI device layer functions as the OMT membrane, TES thermal isolation membrane and microstrip dielectric.

Complete MoAu TES, niobium microstrip, and silicon thermal isolation processing on the device layer side

Temporary bond to pyrex wafer(not shown) and deep reactive ion etch (DRIE) to define OMT and release silicon thermal isolation membranes

Indium bump bond separately fabricated silicon spacer and silicon backshort chip as well as silicon photonic choke chip.

Following the second niobium step the gold broadband load is deposited and patterned by liftoff. The broadband load is used as a termination in the magic-T and cross-over components. It is also used as a contact between the niobium microstrip and the PdAu termination resistor. These connections require the niobium microstrip to have a sloped sidewall for adequate step coverage. The PdAu deposition is optimized for 5ohm/square resistance. The final metal deposition step is ebeam deposition of Pd which is used to provide the necessary heat capacity on the TES membrane for required response time and to maintain the TES membrane at an isothermal temperature. Following the Pd deposition and liftoff the silicon legs and the TES membrane are defined and etched. This is done in an SF6 plasma using a capacitive coupled RIE.

A typical profile of the silicon legs and the TES membrane is shown in figure 2.
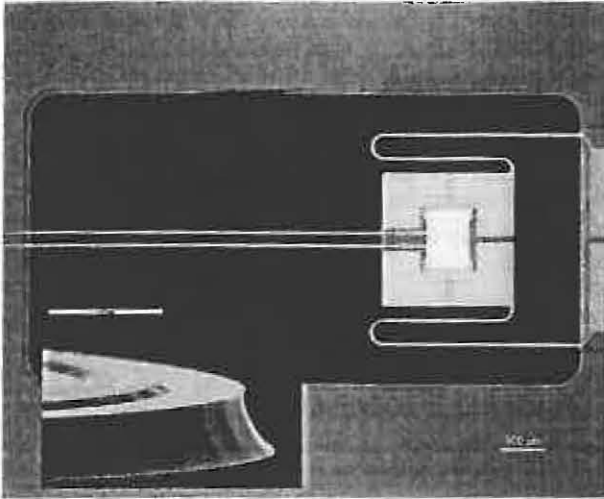
below. The silicon is etched isotropically with 2um of lateral etching for 5um of vertical etching. The leg cut mask continues through the buried niobium ground plane and stops on the polymer bonding material. Next, the wafer is temporarily bonded to a pyrex handle wafer and the backside is patterned for deep reactive ion etching. The DRIE defines the detector chip extent as well as the membranes for the antenna, crossover and magic-T. Next the polymer layer is removed in an O2 plasma stopping on the niobium ground plane and the silicon. The wafer is then soaked in solvent to remove the pyrex handle wafer and the individual chips are released. An image of the final detector chip is shown in figure 3.
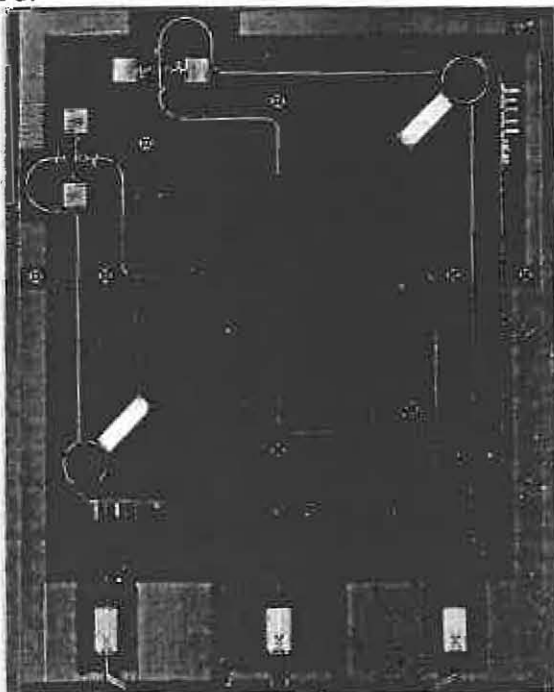

III. SILICON BACKSHORT FABRICATION

For the 40GHz CLASS detector the backshort must be placed 2.04mm from the OMT. We elected to integrate the backshort into silicon using micromaching techniques. For CLASS the silicon backshort assembly not only provides a backshort but also provides mitigation against high frequency leakage from the focal plane that can be picked up in the TES or in unshielded circuit components. An additional component called the silicon interface chip is bonded to the detector chip. This component is used to shield the backside of the TES and OMT from high frequency leakage as well as to extend the ground plane of the detector chip improving the efficiency of photonic choke which is machined into the focal plane. In this section we will discuss the fabrication of the silicon backshort as well as the silicon interface chip.

A. Silicon backshort

The silicon backshort for the 40GHz detector is made up of 3 silicon wafers. 1. A 0.87mm thick interface wafer, 2. A 1.160mm thick spacer wafer, and 3. A 0.325um thick cap wafer. All of the wafers are degeneratively doped silicon with room temperature resistance between 1 to 3mohm-cm and RRR of 1.7. Each of the 3 wafers are processed separately then subsequently bonded at the wafer level with gold thermocompression bonding.

We split up the backshort into a stack of three wafers to improve the sidewall profile of the waveguide which is etched by deep reactive ion etching using the well known Bosch process. The Bosch process consists of alternating a plasma passivation step with an etching step. By adjusting the ratio between the etch time and the passivation time the etch rate and sidewall slope can be controlled. For very thick wafers however, it is difficult to maintain a high aspect slope without the buildup of silicon grass which forms due to unetched passivation. The grass can ultimately limit silicon etching. To simplify the requirements we split the through wafer etching into two steps where we etch halfway through the wafer from either side. This requires a front to back alignment and results in an hourglass waveguide profile with a 2-3 degree slope off of 90deg. A representative profile of the 1.16mm thick spacer is shown in the figure 3 below.
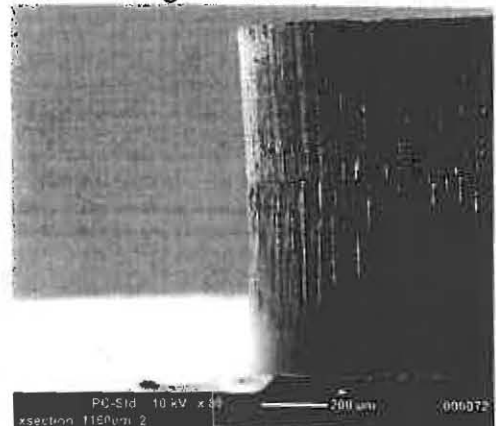
The 0.87mm thick wafer is processed similarly to the 1.16mm wafer where the through wafer DRIE is etched from both sides. Since this wafer forms the interface to the detector chip there is an additional 50um deep relief etch completed on the surface of the backshort wafer which mates to the detector chip to accommodate the Nb microstrip. The backshort wafer contacts the detector wafer around the OMT and around the TES membranes with only a small 150um wide mousehole to accommodate the niobium wiring. The sizes of the cavities around the TES are designed such that they are too small to support high frequency out of band modes that could couple into the TES. An SEM image of the relief etch is shown in figure 4. We additionally micro-machine silicon bumps at the contact interface. When the bonding epoxy is applied to the silicon bumps, capillary action forces it to flow between the bumps only in the contact area while maintaining it only in areas where bonding should occur.

Once the three backshort wafers are complete they are cleaned and coated with 0.5um of gold by electron beam evaporation. The gold coats both the sidewalls of the waveguide as well as the surface of the silicon. The gold coated wafers are bonded in a Karl Suss SB6e substrate bonder at 360C and 4bar pressure following standard Au-Au thermo-compression bonding procedures [7]. The bonding sequence consists of first bonding the cap wafer to the 1.16mm spacer wafer, then bonding the cap/spacer stack to the backshort interface wafer. The surface which interfaces with the detector chip is then coated with niobium to reduce microwave loss. The final step in the process is to dice the 2mm thick stack into individual backshorts. An image of the backshort chip is shown in figure 5.
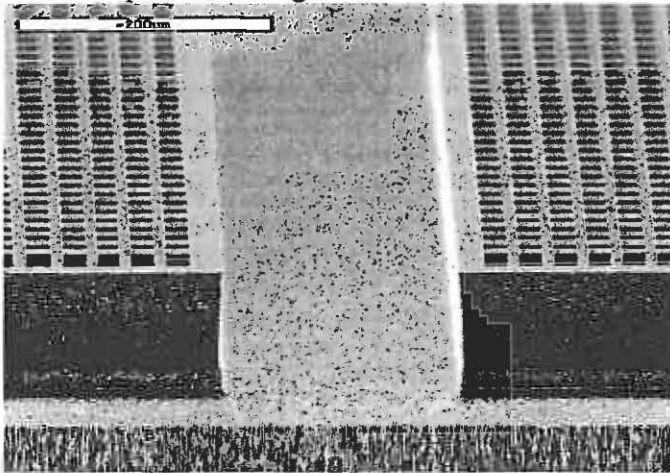
B. Silicon Interface Chip

The last component in the detector assembly is a silicon interface chip which mates the detector chip with the CLASS focal plane. We elected to incorporate the interface chip in order to reduce the required size of the detector chips which are the most complicated and time consuming fabrication process. This allowed us to increase the number of chips per four inch wafer from 4 to 12. The interface chip increases the effective size of the detector chip ground plane thus improving the efficiency of a photonic choke machined into the focal plane. It also caps off the back of the cavities under the TES membrane, magic-T and microstrip crossovers reducing out of band leakage. It is etched such that it can be clamped against metal posts on the focal plane. The interface chip is 0.32mm thick low resistance silicon that is coated by aluminum to reduce microwave loss. Assembly of the backshort, detector chip and interface chip is done by flip chip bonding. First the backshort is bonded with epoxy to the detector chip and next the interface chip is bonded to the back of the detector chip. The photo in figure 6 shows the detector chip bonded to the interface chip.
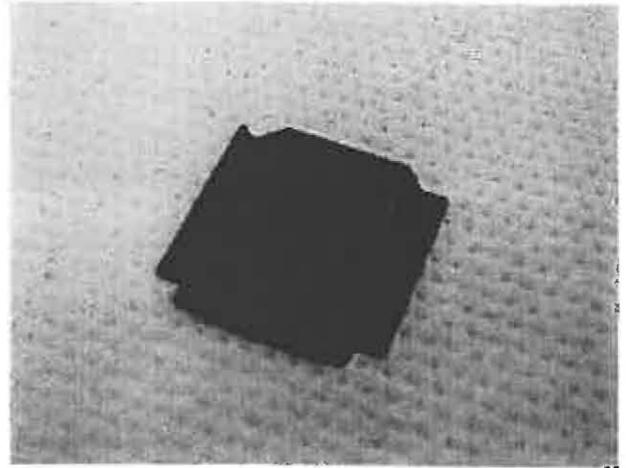
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