Analog Signal Correlating Using an Analog-Based Signal Conditioning Front End

Converting a signal into a bit stream simplifies the correlation function calculation.

John H. Glenn Research Center, Cleveland, Ohio

This innovation is capable of correlating two analog signals by using an analog-based signal conditioning front end to hard-limit the analog signals through adaptive thresholding into a binary bit stream, then performing the correlation using a Hamming "similarity" calculator function embedded in a one-bit digital correlator (OBDC). By converting the analog signal into a bit stream, the calculation of the correlation function is simplified, and less hardware resources are needed. This binary representation allows the hardware to move from a DSP where instructions are performed serially, into digital logic where calculations can be performed in parallel, greatly speeding up calculations.

Each of two analog signals (channels A and B) is converted to a digital bit stream by phase correcting it and comparing it to an average of itself at a sampling clock rate f. The hard-limited conversions of A and B are bitwise compared to measure the level of similarity between the two by the OBDC. This similarity measurement X is equal to the maximum possible Hamming distance (N bits in disagreement) minus the measured number of bits in disagreement.

The OBDC functions are embedded into a field programmable gate array (FPGA). The OBDC is made up of two shift registers containing the current sample values (of length N) from each of the two input channels (A and B). During each sample clock, a new sample from each A and B input is clocked into the input linear shift register for each respective channel; this input shifts the current values in the linear shift register. The oldest ($N + 1$ sample clocks ago) sample is clocked out of the register. Once the inputs have been clocked in, the correlation routine can start. This rising edge of the sample clock also clears the max correlation value, the best correlation index, and the shift counter registers, initializing the correlator.

When the two registers match exactly, or are correlated, the X value will equal N. Once the correlation value has been calculated, this result is forwarded to compare with the max correlation value register. If the X value is greater than the current max correlation value, then the max correlation value becomes X, and the shift counter register is latched and put into the best correlation index register, providing the index of the current best correlation.

This index is the number of sample clock periods difference between the two input signals and thus, for sample clock rate f, indicates the delay between the signals A and B.

This work was done by Norman Prokop and Michael Krasowski of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18902-1.

Micro-Textured Black Silicon Wick for Silicon Heat Pipe Array

This technology can be used for microprocessors, power switching circuits, and diode lasers in high-power electronics.

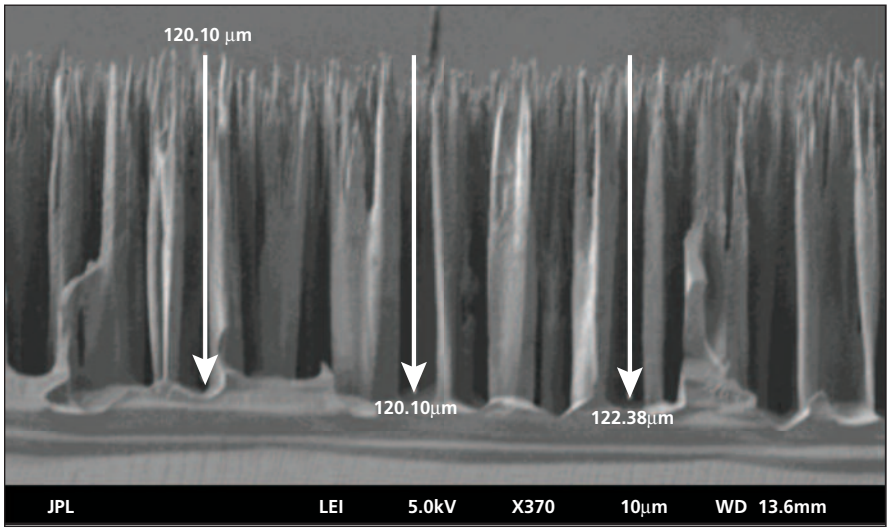
NASA's Jet Propulsion Laboratory, Pasadena, California

Planar, semiconductor heat arrays have been previously proposed and developed; however, this design makes use of a novel, microscale black silicon wick structure that provides increased capillary pumping pressure of the internal working fluid, resulting in increased effective thermal conductivity of the device, and also enables operation of the device in any orientation with respect to the gravity vector.

In a heat pipe, the efficiency of thermal transfer from the case to the working fluid is directly proportional to the surface area of the wick in contact with the fluid. Also, the primary failure mechanism for heat pipes operating within the temperature range of interest is inadequate capillary pressure for the return of fluid from the condenser to the wick. This is also what makes the operation of heat pipes orientation-sensitive. Thus, the two primary requirements for a good wick design are a large surface area and high capillary pressure. Surface area can be maximized through nanomachined surface roughening. Capillary pressure is largely driven by the working fluid and wick structure.

The proposed nanostructure wick has characteristic dimensions on the order of tens of microns, which promotes menisci of very small radii. This results in the possibility of enormous pumping potential due to the inverse proportionality with radius. Wetting, which also enhances capillary pumping, can be maximized through growth of an oxide layer or material deposition (e.g. TiO_2) to create a superhydrophilic surface.

In addition, the wick fabrication technique produces nanostructure forests that



SEM photo showing black silicon formed by ICP cryo etching.

are planar, and can take advantage of 2D heat spreading over a surface vs. state-of-the-art 1D heat transport associated with heat pipes. The combined result of these benefits promises to be a two-phase heat transfer device, which is very insensitive to a gravity field. Although liquid pressure drops may be relatively large depending on the nanostructure density, the overall device dimensions of ≈ 7×7 cm are expected to be well within the overall capillary limit. The novel aspects of the currently proposed effort include the use of the phenomenon of superhydrophilicity in a heat pipe, and the wick geometry, control of the nanotip height density, and the method for creating this nanotip texture. A cryo-etch inductively coupled plasma is used to make the nanotips, enabling the cost-effective, mask-free formation of a uniform black silicon surface over a large area, with nanotip heights exceeding 100 microns. Unlike nanotextured surfaces formed by the growth or deposition of materials (e.g. carbon nanotubes), the resulting formations are robust and compatible with liquid processes.

This work was done by Karl Y. Yee, Eric T. Sunada, Gani B. Ganapathi, Harish Manohara, and Andrew Homyk of Caltech, and Mauro Prina of SpaceX for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). ***NPO-47299***

Robust Multivariable Optimization and Performance Simulation for ASIC Design

Systematic method automates the simulation and optimization of circuits.

Goddard Space Flight Center, Greenbelt, Maryland

Application-specific-integrated-circuit (ASIC) design for space applications involves multiple challenges of maximizing performance, minimizing power, and ensuring reliable operation in extreme environments. This is a complex multidimensional optimization problem, which must be solved early in the development cycle of a system due to the time required for testing and qualification severely limiting opportunities to modify and iterate. Manual design techniques, which generally involve simulation at one or a small number of corners with a very limited set of simultaneously variable parameters in order to make the problem tractable, are inefficient and not guaranteed to achieve the best possible results within the performance envelope defined by the process and environmental requirements. What is required is a means to automate design parameter variation, allow the designer to specify operational constraints and performance goals, and to analyze the results in a way that facilitates identifying the tradeoffs defining the performance envelope over the full set of process and environmental corner cases.

The system developed by the Mixed Signal ASIC Group (MSAG) at the Goddard Space Flight Center is implemented as a framework of software modules, templates, and function libraries. It integrates CAD tools and a mathematical computing environment, and can be customized for new circuit designs with only a modest amount of effort as most common tasks are already encapsulated. Customization is required for simulation test benches to determine performance metrics and for cost function computation. Templates provide a starting point for both, while toolbox functions minimize the code required. Once a test bench has been coded to optimize a particular circuit, it is also used to verify the final design. The combination of test bench and cost function can then serve as a template for similar circuits or be re-used to migrate the design to different processes by re-running it with the new process-specific device models. The system has been used in the design of time- to-digital converters for laser ranging and time-of-flight mass spectrometry to optimize analog, mixed signal and digital circuits such as charge sensitive amplifiers, comparators, delay elements, radiation tolerant dual interlocked (DICE) flip-flops, and two of three voter gates.

The overall structure of the framework consists of two processes running independently and communicating with each other via a data and handshaking file interface. The master optimization process contains the multivariable optimization algorithm and performs top level analysis of results to select the best solution. It is currently implemented in the Scilab open source environment for numerical computation. This environment is supported on multiple platforms, is well suited to performing numerical analysis and data visualization, and has the advantage of being free to use. Cost can be a significant consideration since multiple copies of the environment may need to run for hours or even days at a time.