

Prognostics of Power Electronics, methods and validation experiments

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Abstract—Failure of electronic devices is a concern for future electric aircrafts that will see an increase of electronics to drive and control safety-critical equipment throughout the aircraft. As a result, investigation of precursors to failure in electronics and prediction of remaining life of electronic components is of key importance. DC-DC power converters are power electronics systems employed typically as sourcing elements for avionics equipment. Current research efforts in prognostics for these power systems focuses on the identification of failure mechanisms and the development of accelerated aging methodologies and systems to accelerate the aging process of test devices, while continuously measuring key electrical and thermal parameters. Preliminary model-based prognostics algorithms have been developed making use of empirical degradation models and physics-inspired degradation model with focus on key components like electrolytic capacitors and power MOSFETs (metal-oxide-semiconductor-field-effect-transistor). This paper presents current results on the development of validation methods for prognostics algorithms of power electrolytic capacitors. Particularly, in the use of accelerated aging systems for algorithm validation. Validation of prognostics algorithms present difficulties in practice due to the lack of run-to-failure experiments in deployed systems. By using accelerated experiments, we circumvent this problem in order to define initial validation activities.

I. INTRODUCTION

This paper presents current results in prognostics of electrolytic capacitors and a discussion of validation approaches for the prognostics methods. This research is geared towards the system-level development of model-based approaches to study the degradation effects of power supply converters on avionics systems. Most devices and systems today contain embedded electronic modules for monitoring, control and enhanced functionality. In spite of the electronic modules being used to enhance system performance and capabilities, these modules are often the first elements in the system to fail [1]. These failures can be attributed to adverse operating conditions, such as high temperatures, voltage surges and current spikes.

Avionics systems combine physical processes, computational hardware, and software systems, and present unique challenges to performing root cause analysis when faults occur, and also for establishing the effects of faults on overall

system behavior and performance. However, systematic analysis of these conditions is very important for analysis of safety and also to avoid catastrophic failures in navigation systems. This drives the need for integrated prognostics and health management (PHM) technologies for flight-critical avionics. Flight and ground crews require accurate health state estimates of these critical avionics components, including accurate detection of faults and prediction of time to the functional failure of the avionics system. An understanding of how components degrade is needed as well as the capability to anticipate failures and predict the remaining useful life of electronic components [2], [3]. Studying and analyzing the degradation of these systems (i.e., degradation in performance) to improve aircraft reliability, assure in-flight performance, and reduce maintenance costs, [2], [3] therefore it is absolutely necessary to provide system health awareness for electronics systems. In addition to this, an understanding of the behavior of deteriorated components is needed as well as the capability to anticipate failures and predict the remaining life of electronics systems.

PHM methodologies have emerged as one of the key enablers for achieving efficient system level maintenance and lowering life cycle costs in military systems [2], [4]. Prognostics and health management for electronic systems aims to detect, isolate, and predict the onset and source of system degradation as well as the time to system failure. The goal is to make intelligent decisions about the system health and to arrive at strategic and business based decisions. As electronics become increasingly complex, performing PHM efficiently and cost-effectively is becoming highly demanding [4].

Some of earlier efforts in diagnostic health monitoring of electronic systems and subsystems involved the use of a built-in test (BIT), defined as an on-board hardware-software diagnostic tests to identify and locate faults. Studies conducted by [4] on the use of BITs for fault identification and diagnostics showed that they can be prone to false alarms and may result in unnecessary costly replacement, re-qualification, delayed shipping, and loss of system availability. The persistence of such issues over the years is perhaps because the use of BIT has been restricted to low-volume systems. In general, BITs

generally have not been designed to provide prognostics or remaining useful life due to accumulated damage or progression of faults. Rather, it has served primarily as a diagnostic tool.

The problem addressed in this research applies effective PHM methodologies to electronic systems and components. The research work focuses on developing and implementing effective diagnostic and prognostic methodologies, including the ability to detect degradation in electrical and electronic components through failure precursors in the system. A major task requires developing the physics-based failure models for electronic components and further studying their effect on the overall system performance. Our research goal is to develop physics-based failure models, derived from first principle of operation, for electronic components in a general framework, which can be then be applied to studying performance parameters related to degradation, aging of components and their cascading effects on systems and subsystems. Early detection and analysis may lead to better prediction and end of life estimates by tracking and modeling the degradation process. One of our goals is to use these estimates to make accurate and precise prediction of the time to failure of components and the overall subsystem. This is achieved through a physics based modeling approach to predict the dynamic behavior of the system under nominal and degraded conditions.

In this work we study the degradation effects of electrolytic capacitors on the DC-DC converter systems. In our earlier work [5], [6], we developed models for prognostics studies at the component level, while in [7] a model based DC-DC converter system was studied and fault diagnosis was done by introducing faults in the MOSFETs and Capacitors.

A. Background on DC-DC converter health management

In this section we discuss the DC-DC converter model derived based on the bond graph methodology as discussed in section earlier. A circuit diagram of a buck-boost converter used for this study is shown in Fig.1. In this work we study the degradation effects of electrolytic capacitors on the DC-DC converter systems. In our earlier work [5], [6], we developed models for prognostics studies at the component level, while in [7] a model based DC-DC converter system was studied and fault diagnosis was done by introducing faults in the MOSFETs and Capacitors. A circuit diagram of a buck-boost converter used for this study is shown in Fig. 1. In the circuit diagram it can be seen that, the electrolytic capacitor at the output is composed of a series combination of Capacitor (C) and equivalent series resistance (ESR).

II. MODEL-BASED PROGNOSTICS FOR ELECTRONICS

A model-based prognostics methodology for electrolytic capacitors is presented in this section. This methodology relies on accelerated aging experiments to identify degradation behavior and to create time dependent degradation models. The process followed in the proposed methodology is presented in the block diagram in Fig. 2 and further described in the upcoming paragraphs.

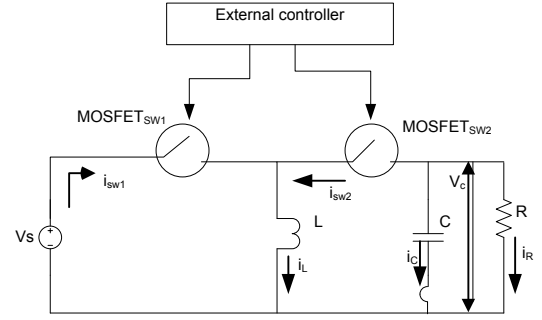


Fig. 1. Buck boost converter circuit.

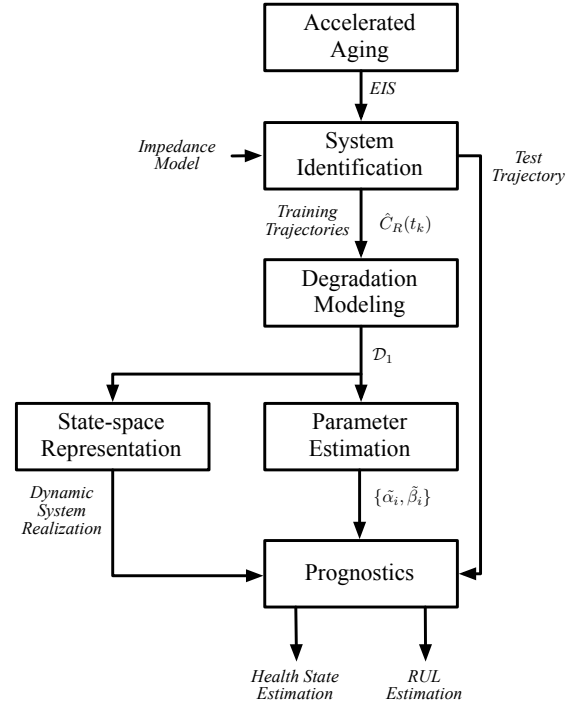


Fig. 2. Methodology for development of model-based prognostics algorithms for electronics.

Accelerated Aging: The methodology is based on results from an accelerated life test on real electrolytic capacitors. This test applied electrical overstress to commercial, off the shelf capacitors, in order to observe and record the degradation process and identify performance conditions in the neighborhood of the failure criteria in a considerably reduced time frame. Several measurements are made through the aging time, including measurements at pristine condition and measurements after failure condition.

System Identification: A lumped-parameter model of the non-ideal capacitor impedance was assumed. This impedance model included a capacitance element and an equivalent series resistance parasitic element. The Electrochemical Impedance Spectroscopy (EIS) measurements along with the impedance model structure are used in a systems identification setting to estimate the model parameters available throughout the aging

test (see section II-A).

Degradation Modeling: The objective of the model is to generate a parametrized model of the time-dependent capacitance degradation as generated by the system identification step. This model was based on a single precursor to failure feature representing capacitor functional performance.

Parameter Estimation: The parameters of the degradation model are typically estimated using nonlinear least-squares regression for models with static parameters or with a Bayesian tracking framework in cases where parameters need to be estimated online.

Prognostics: A Bayesian framework is employed to estimate (track) the state of health of the capacitor based on measurement updates of key capacitor parameters. The filter algorithm is used to track the state of health and the degradation model is used to make predictions of remaining useful life once no further measurements are available. The methodology consists of the following three main steps and it is depicted in Fig. 3.

- 1) State tracking: The capacitance loss or the capacitance are defined as the state variable to be estimated and the degradation model is expressed as a discrete time dynamic model in order to estimate capacitance loss as new measurements become available. Direct measurements of the capacitance are assumed for the filter.
- 2) Health state forecasting: It is necessary to forecast the state variable once there are no more measurements available at time or RUL prediction t_p . This is done by evaluating the degradation model through time using the state estimate at time t_p as initial value.
- 3) Remaining life computation: RUL is computed as the time between time of prediction t_p and the time at which the forecasted state crosses the failure threshold value.

This process is repeated for different values of t_p through the life of the component under consideration.

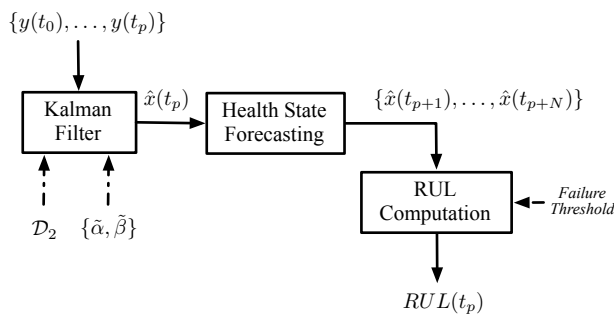


Fig. 3. Model-based prognostics methodology.

A. Prognostics based on Electrical Overstress Experiments

Electrical overstress accelerated aging experiments were conducted in order to understand the failure mechanisms related to electrical operation and to understand the degradation process' time evolution. The electrical overstress consists on continuously charging and discharging the capacitors under test using a square waveform at 12V for capacitors rated at

10V. The waveform frequency was 20mHz and a set of 6 capacitors were aged for 200+ hours. Details of the experiment are presented in detail in [8].

Periodic characterization of ESR and capacitance were conducted. The ESR value is the real impedance measured through the terminal software of the instrument. Similarly, the capacitance value is computed from the imaginary impedance using EIS. Characterization of all the capacitors was done for measuring the impedance values using an SP-150 Biologic impedance measurement instrument [9]. Fig. 4 presents results of the time evolution of the percentage capacitance loss for the 6 capacitors under test. Failure threshold is consider as 20% loss in capacitance.

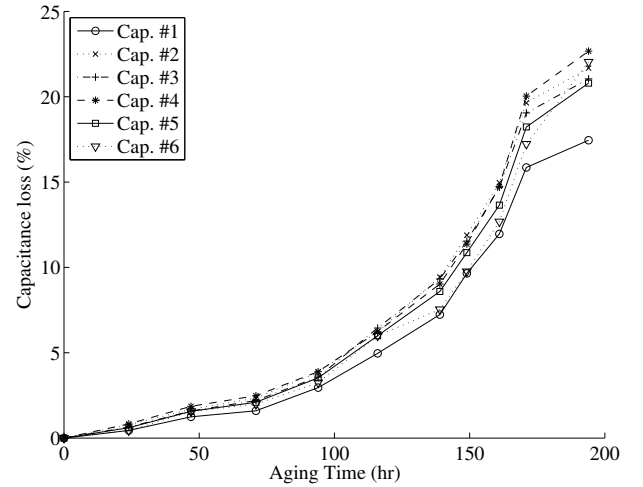


Fig. 4. Degradation of capacitor performance, percentage capacitance loss as a function of aging time.

1) *Empirical degradation model for capacitance loss:* The percentage loss in capacitance is used as a precursor of failure variable and it is used to build a model of the degradation process. This model relates aging time to the percentage loss in capacitance. Let C_l be the percentage loss of capacitance due to degradation as shown by Fig. 4. The following equation is a *degradation model* \mathcal{D}_1 of the capacitance parameter in the non-ideal capacitor.

$$\mathcal{D}_1 : C_l(t) = e^{\alpha t} + \beta, \quad (1)$$

where α and β are degradation model parameters that will be estimated from the experimental data of accelerated aging experiments. The experimental results presented in Fig. 4 show that the degradation process is very similar among all the capacitors under test. As a result, the parameters of the model were estimated off-line using all the test data and the nonlinear least-squares regression. This parameters remain static through the RUL estimation process. Further details are available in [10].

The estimated degradation model is used as part of a Bayesian tracking framework to be implemented using the Kalman filter technique. This method requires a state-space dynamic model relating the degradation level at time t_k to the

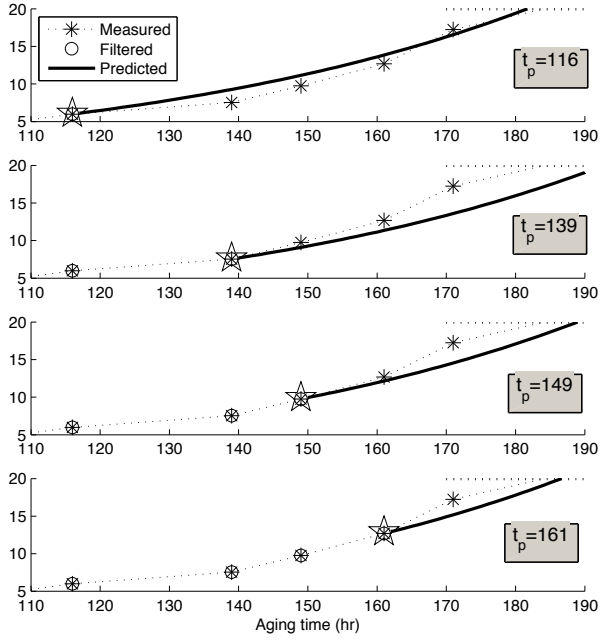


Fig. 5. RUL prediction process results

degradation level at time t_{k-1} . The procedure to obtain a state-space model for \mathcal{D}_1 is as follows. The non-linear exponential behavior described in the model is represented as a first order differential equation which can represent the time evolution of $C_l(t)$. Then, the model is discretized in time in order to obtain a discrete-time state-space model \mathcal{D}_2 .

$$\mathcal{D}_2 : C_l(t_k) = (1 + \alpha\Delta_k)C_l(t_{k-1}) - \alpha\beta\Delta_k. \quad (2)$$

This model is used in a Bayesian tracking framework in order to continuously estimate the value of the loss in capacitance through time as measurement become available.

2) *Prediction of Remaining Useful Life Results:* Fig. 5 presents results from the remaining useful life prediction algorithm at different aging times $t_p = 116, 139, 149$ and 161 (hrs), at which the capacitors are characterized and their capacitance (C) value is available. The failure threshold is considered to be 20% decrease in capacitance value. End of life (EOL) is defined as the time at which the forecasted capacitance value trajectory crosses the failure threshold. Fig. 6 presents the RUL prediction results for capacitor #6 using the α - λ metric. Additional details and results for all capacitors are presented in [10].

B. Prognostics based on Thermal Overstress Experiments

In this setup we emulated conditions similar to high temperature storage conditions [5], [11], where capacitors were placed in a controlled chamber and the temperature raised to 105°C while the capacitor is rated for 85°C . ESR and capacitor parameters are available through periodic EIS characterization.

Under thermal overstress conditions, since the device was subjected to only high temperature with no charge applied, we observe degradation only due to electrolyte evaporation. The

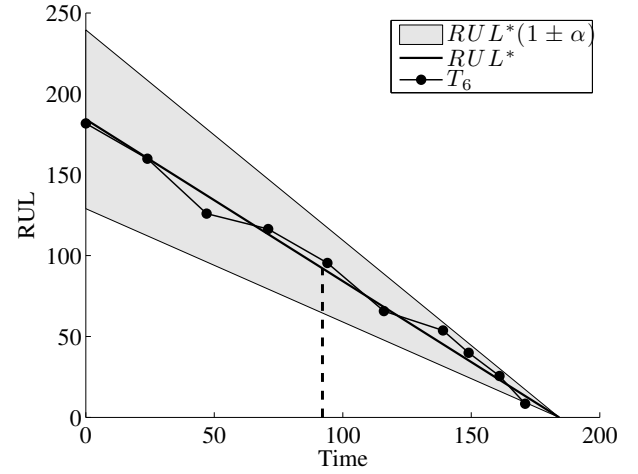


Fig. 6. Performance based on α - λ performance metric.

models are derived based on this observations and measurements see during from the experimental data. For deriving the physics based models it is also necessary to know about the structural details of the component under study since health estimations are done based on the type of electrolyte, volume of electrolyte, oxide layer thickness etc. The models defined use this information for making effective degradation/failure predictions. A detail structural study of the electrolytic capacitor is available in [12].

1) *Capacitance Degradation Model:* Exposure of the capacitors to high temperatures, $T_{applied} > T_{rated}$ results in accelerated aging of the devices [6], [13]. Higher ambient storage temperature accelerates the rate of electrolyte evaporation leading to degradation of the capacitance [5], [14].

Details of for the derived capacitance degradation model are in [12]. The complete discrete time dynamic model for capacitance degradation is given by

$$\mathcal{D}_3 : C_{k+1} = C_k - \frac{(2\epsilon_R\epsilon_0w_eA_sj_{eo})}{d_c * d_s} \Delta t, \quad (3)$$

where:

ϵ_R = relative dielectric constant

ϵ_0 = permittivity of free space

j_{eo} = evaporation rate ($\text{mg min}^{-1} \text{area}^{-1}$)

w_e = volume of ethyl glycol molecule

A_s = oxide surface area

d_c = thickness of cathode strip

d_s = thickness of spacer paper. t = time in hours.

The model \mathcal{D}_3 , in Eq. (3) is implemented in a Bayesian tracking framework (unscented Kalman filter (UKF)) since the degradation in capacitance (state) due to decrease in electrolyte volume, (V) is considered to be a dynamic linear model and the evaporation rate, (j_{eo}) parameter, assumed to be varying. The parameter j_{eo} is estimated online since it depends on the amount of electrolyte present in the capacitor, as the volume changes with time j_{eo} changes and is estimated accordingly. Details on the methodology are presented in [15], [16].

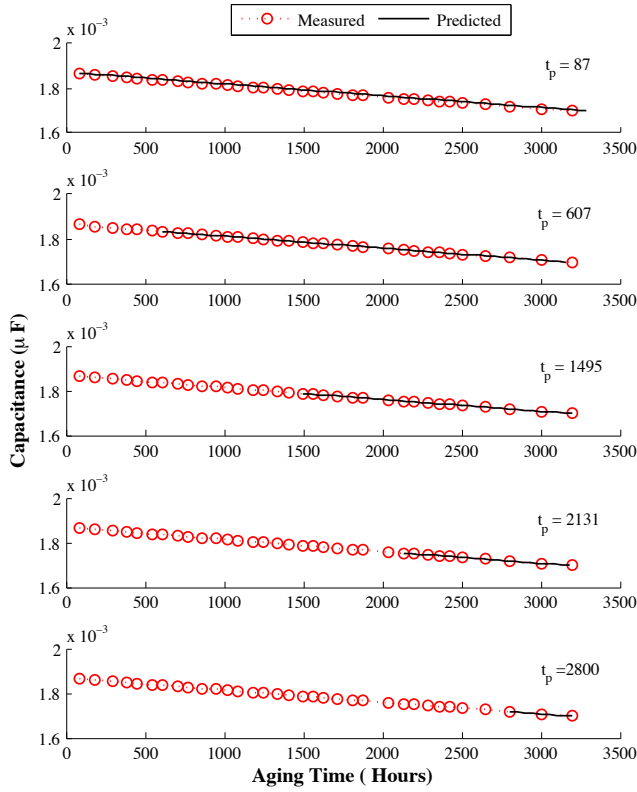


Fig. 7. Capacitance decrease prediction at different Aging Time for Cap # 5

2) *Prediction of Remaining Useful Life Results:* Fig. 7 presents results from the remaining useful life prediction algorithm at different aging times $t_p = 87, 607, 1495, 2131, 2800$ (hrs), at which the capacitors are characterized and their capacitance (C) value is calculated. The failure threshold is considered to be 10% decrease in capacitance value, which in this case is at 3200 hours of aging time. End of life is defined as the time at which the forecasted capacitance value trajectory crosses the EOL threshold. Therefore, RUL is EOL minus aging times $t_p = 87.5, 607, 1495, 2131, 2800$ (hrs).

An α - λ prognostics performance metric [17], [18] is presented in Fig. 8 for test case of Cap #5. Performance metric identifies whether the algorithm performs within desired error margins (specified by the parameter α) of the actual RUL at any given time instant (specified by the parameter λ) [17] and is based on relative accuracy (RA) metric in equation (4).

$$RA = 100 \left(1 - \frac{RUL^* - RUL'}{RUL^*} \right) \quad (4)$$

III. VALIDATION APPROACHES

A. Prognostics validation for electrical overstress mechanisms

Validation experiments for electrical overstress consists of 6 samples and have previously presented [6], [12] as a leave one out validation test. In this algorithm, parameters are static and the validity of the model and its corresponding static parameters are assessed by the leave one out validation test.

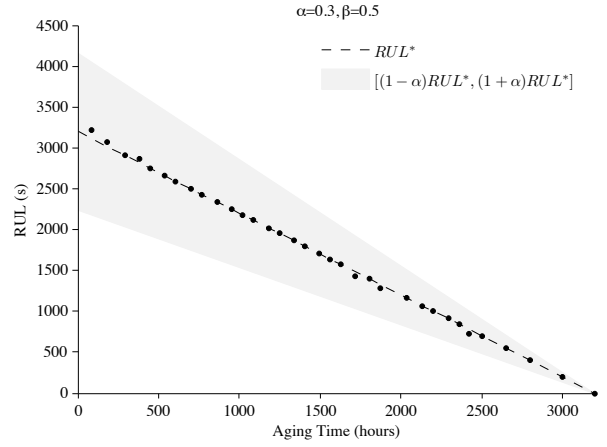


Fig. 8. Performance based on Alpha-Lambda metric for Cap#5

Details can be found on [6], [12]. In addition for results described in this work, several capacitors at different stress levels are being tested. This will help to identify the validity of the model with respect to different usage condition and guide the enhancement of degradation models to include loading.

B. Prognostics validation for thermal overstress mechanism

Validation experiments for thermal overstress data consists of several samples at same temperature level, results are presented on the form of RA metric as summarized in table I, where \overline{RA}_a is the mean relative accuracy of each capacitor at all prediction times.

Capacitors	\overline{RA}_a
C1	87.13
C2	90.78
C3	87.99
C4	96.60
C5	99.39
C6	89.29
C7	94.45
C8	85.73
C9	92.14
C10	92.50
C11	90.32
C12	87.15
C13	95.49
C14	94.97
C15	92.38

TABLE I
SUMMARY OF RUL FORECASTING RESULTS.

From table I it is observed that the prediction with physics-based degradation model for all the 15 capacitors under test is within acceptable limits. But the mean accuracy of capacitor over aging time dropped due to the non-linearity observed in the data at the end of the aging time and the limitation of the model due to not including the oxide layer breakdown.

Experiments conducted at different temperatures and different capacitors at same temperatures are currently underway

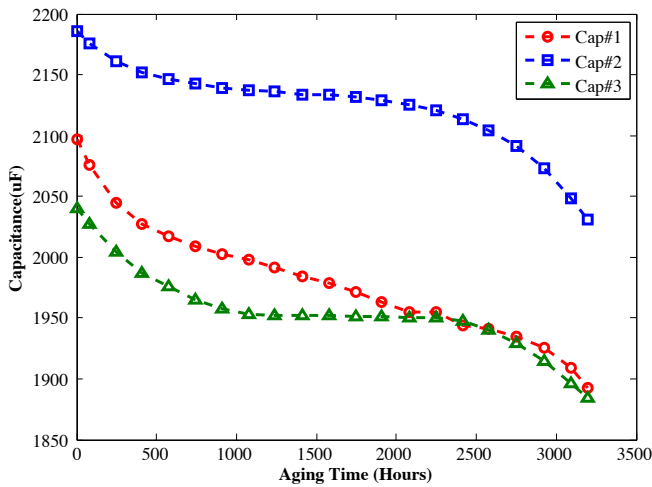


Fig. 9. Capacitance degradation under nominal usage in DC-DC converter.

and will be used for validation. This should help identify the validity of the model for cases with different loading (different aging temperature) and for capacitors of different manufacturing batch or different manufacturing process.

C. Prognostics validation based on nominal usage experiments

A small set of capacitors is available representing nominal usage on a DC-DC converter. These capacitors are of the same type as considered for thermal and electrical overstress cases in previous section. They have been in operation during 2+ years. They are periodically characterized in terms of C and ESR and this data is currently being target for validation of the previously presented empirical degradation model for electrical overstress and for physics-based degradation models for thermal overstress and electrical overstress (not discussed in this paper). Figure 9 presents results from capacitance performance degradation under nominal usage on the DC-DC converter. The main challenge on this work is to map the models currently developed on an accelerated lifetime time frame, to the time frame of real usage condition. The nominal degradation experiments will aid in the validation process and on guiding enhancements to such models. A set of 20 additional nominal degradation tests are currently being implemented.

IV. CONCLUSION

An overview of the current results of prognostics for DC-DC power converters is presented, focusing on the output filter capacitor component. The electrolytic capacitor used typically as filter capacitor is one of the components of the power supply with higher failure rate, hence the effort in developing component level prognostics methods for capacitors. An overview of prognostics algorithms based on electrical overstress and thermal overstress accelerated aging data is presented and a discussion on the current efforts in terms of validation of the algorithms is included. The focus of current

and future work is to develop a methodology that allows for algorithm development using accelerated aging data and then transform that to a valid algorithm on the real usage time scale.

ACKNOWLEDGMENT

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