CMOS-Compatible SOI MESFETS for Radiation-Hardened DC-to-DC Converters

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A radiation-tolerant transistor switch has been developed that can operate between –196 and +150 °C for DC-to-DC power conversion applications. A prototype buck regulator component was demonstrated to be performing well after a total ionizing dose of 300 krad(Si). The prototype buck converters showed good efficiencies at ultra-high switching speeds in the range of 1 to 10 MHz. Such high switching frequency will enable smaller, lighter buck converters to be developed as part of the next project. Switching regulators are widely used in commercial applications including portable consumer electronics.

This work was done by Trevor Thornton of Arizona State University and William Lepkowski and Seth Wilk of SJT Micropower for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16304-1

Silicon Heat Pipe Array

Applications include high-power electronic circuits or components such as microprocessors, diode lasers, and concentrated solar collectors.

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Improved methods of heat dissipation are required for modern, high-power-density electronic systems. As increased functionality is progressively compacted into decreasing volumes, this need will be exacerbated. High-performance chip power is predicted to increase monotonically and rapidly with time. Systems utilizing these chips are currently reliant upon decades of old cooling technology.

Heat pipes offer a solution to this problem. Heat pipes are passive, self-contained, two-phase heat dissipation devices. Heat conducted into the device through a wick structure converts the working fluid into a vapor, which then releases the heat via condensation after being transported away from the heat source. Heat pipes have high thermal conductivities, are inexpensive, and have been utilized in previous space missions. However, the cylindrical geometry of commercial heat pipes is a poor fit to the planar geometries of microelectronic assemblies, the copper that commercial heat pipes are typically constructed of is a poor CTE (coefficient of thermal expansion) match to the semiconductor die utilized in these assemblies, and the functionality and reliability of heat pipes in general is strongly dependent on the orientation of the assembly with respect to the gravity vector. What is needed is a planar, semiconductor-based heat pipe array that can be used for cooling of generic MCM (multichip module) assemblies that can also function in all orientations. Such a structure would not only have applications in the cooling of space electronics, but would have commercial applications as well (e.g. cooling of microprocessors and high-power laser diodes).

This technology is an improvement over existing heat pipe designs due to the finer porosity of the wick, which enhances capillary pumping pressure, resulting in greater effective thermal conductivity and performance in any orientation with respect to the gravity vector. In addition, it is constructed of silicon, and thus is better suited for the cooling of semiconductor devices.

The device consists of two silicon wafers, one of which has a mechanically drilled hole for a fill port. Each wafer is lithographically masked and etched to define a hermetic seal ring and the structural support elements. Each wafer then undergoes a mask-free cryo etch to define the black Si wick structure (the etch process developed results in an ≈3× taller black Si structure than has been reported elsewhere). The wafers are then cleaned, thermally oxidized, and fusion-bonded together. Precision metering is then utilized to fill the device with the working fluid (e.g. water) through the fill port, which is then sealed off.

This device is able to absorb a large quantity of heat due to the phase change of the working fluid, and transport the heat efficiently away from the source (i.e., it has a large effective thermal conductivity). Due to the small effective pore radius of the nanotextured surface, high capillary forces are exerted on the working fluid and the device is able to work in any orientation with respect to the gravity vector. In addition, due to the all silicon construction, the device is expansion-matched to the types of high-power die that would potentially be mounted to it.

The novel aspects of this assembly include:

(1) Co-fabrication of the heat pipe structure and the wick. A black Si wick structure is utilized so that the housing of the heat pipe and the wick structure can be co-fabricated. This enables stress-free operation of the device over temperature, as the device is of homogenous material construction. Adhesion of the wick to the structure is not an issue, as the wick is etched from the structure itself, and is not grown or deposited.

(2) Direct attachment or integration of heat-generating elements to the heat pipe. Fabrication of the heat pipe from Si allows stress-free, expansion-matched attachment of high-power semiconductor components or even the direct integration of such components. For example, high-power

semiconductor lasers could be solder-attached in modular fashion to the heat pipe, or could be made directly from the heat pipe structure itself for increased thermal efficiency. Another example would be the fabrication of solar cells for use in concentrated solar collectors; co-fabrication of the heat pipe with the solar cells from the same silicon wafer would enable more efficient thermal management.

This work was done by Karl Y. Yee, Gani B. Ganapathi, Eric T. Sunada, Youngsam Bae, Jennifer R. Miller, and Daniel F. Berisford of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-47306

Adaptive Phase Delay Generator

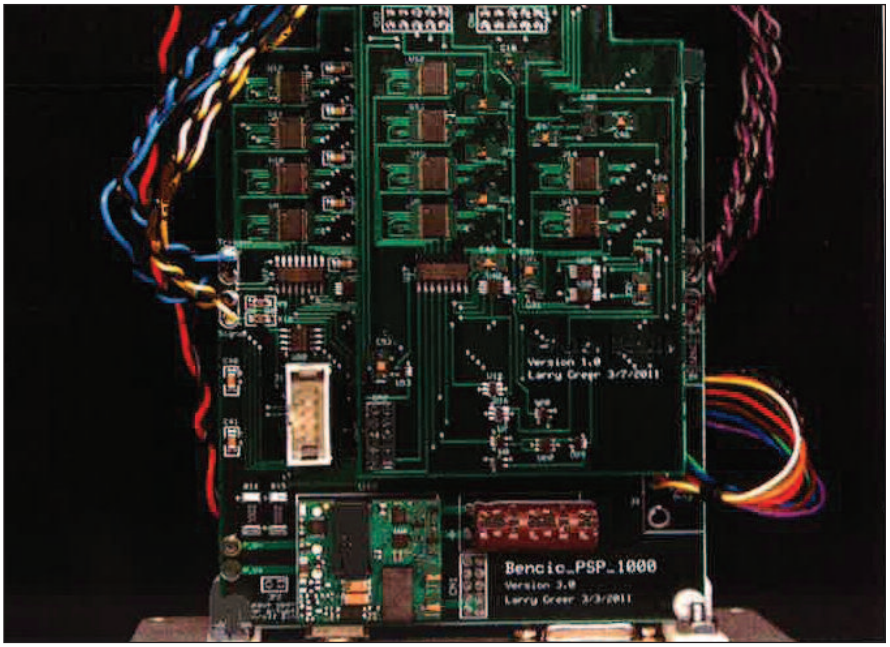
Test facilities that need to synchronize test equipment with rotating machinery could make use of this device.

John H. Glenn Research Center, Cleveland, Ohio

There are several experimental setups involving rotating machinery that require some form of synchronization. The adaptive phase delay generator (APDG) — the Bencic-1000 — is a flexible instrument that allows the user to generate pulses synchronized to the rising edge of a tachometer signal from any piece of rotating machinery. These synchronized pulses can vary by the delay angle, pulse width, number of pulses per period, number of skipped pulses, and total number of pulses. Due to the design of the pulse generator, any and all of these parameters can be changed independently, yielding an unparalleled level of versatility.

There are two user interfaces to the APDG. The first is a LabVIEW program that has the advantage of displaying all of the pulse parameters and input signal data within one neatly organized window on the PC monitor. Furthermore, the LabVIEW interface plots the rpm of the two input signal channels in real time. The second user interface is a handheld portable device that goes anywhere a computer is not accessible. It consists of a liquid-crystal display and keypad, which enable the user to control the unit by scrolling through a host of command menus and parameter listings.

The APDG combines all of the desired synchronization control into one unit. The experimenter can adjust the delay, pulse width, pulse count, number of skipped pulses, and produce a specified number of pulses per revolution. Each of these parameters can be changed independently, providing an unparalleled level of versatility when synchronizing hardware to a host of rotating machinery. The APDG allows experimenters to set up quickly and generate a host of synchronizing configurations using a simple user interface, which hopefully leads to faster results.



The construction of the **Adaptive Phase Delay Generator** allows for inclusion of multi-pulse functions by adding an expansion board to each channel.

The heart of the Bencic-1000 is a reconfigurable pulse-generating state machine that cycles through three to four primary states, depending on the mode of operation. A second state machine tracks the period of the input signal by incorporating a latching synchronous 32-bit counter and a microcontroller. These hardware state machines make use of high-speed CMOS technology, primarily from the HC family of parts, and have no problem operating with the 10-MHz master clock. The microcontroller is a 50-MHz 8051 derivative optimized to run at 50 MIPS.

This work was done by Lawrence Greer of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18942-1.