



DSP/FPGA Design for a High-Speed Programmable S-Band Space Transceiver

Goddard Space Flight Center, Greenbelt, Maryland

Traditional command uplink receivers are very limited in performance capability, take a long time to acquire, cannot operate on both uplink bands (NASA & AFSCN), and only support low-rate communications. As a result, transceivers end up on many programs' critical paths, even though they should be a standard purchased spacecraft subsystem. Also, many missions are impacted by the low effective uplink throughput. In order to tackle these challenges, a transceiver was developed that will provide on-site frequency agility, support of high uplink rates, and operation on both NASA and AFSCN frequency bands.

The device is a low-power, high-reliability, and high-performance digital signal processing (DSP) demodulator for an on-orbit programmable com-

mand receiver. There are several drivers available for the modulation technique. Those drivers include receiver complexity, power consumption, spectral efficiency, and CCSDS (Consultative Committee for Space Data Systems) framework recommendations. Previous research suggests that GMSK (Gaussian Minimum Shift Keying) and BPSK (Binary Phase Shift Keying) are good choices for the uplink modulation format. This approach is supported by CCSDS and helps reduce receiver complexity.

Analysis and derived simulations were performed for power, bandwidth, clock generator, bit synchronizer, and carrier loop. At the time of this reporting, the code was not yet written, and will evolve from the existing analysis and simulation.

The demodulator operates on the two selected modes, BPSK and GMSK. The bit rate covers multiple octaves and includes a bit synchronizer function. The modulator is unique in that it operates with high Doppler, over a large bit rate range, and in a space environment. In addition, this demodulator attempts to maximize low power, small size, and ease of modification to new applications.

Novel features of the innovation include DSP logic for multiple modulation types in a low-power and rad-tolerant platform. Advantages include on-the-fly programmable low-power receive communications for spacecraft.

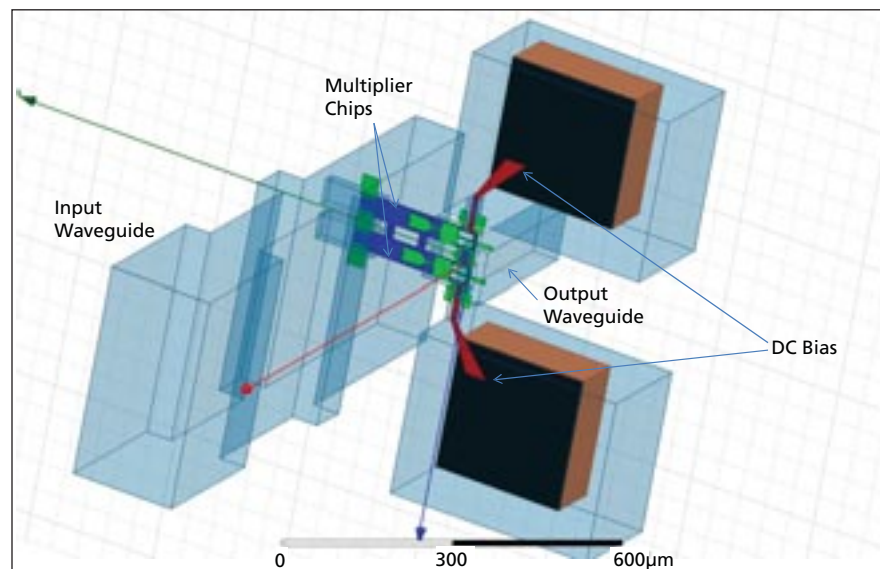
This work was done by Jeffrey Janick and Assi Friedman of Innoflight, Inc. for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16030-1

On-Chip Power-Combining for High-Power Schottky Diode-Based Frequency Multipliers

High-power solid-state sources operate at terahertz frequencies.

NASA's Jet Propulsion Laboratory, Pasadena, California

A 1.6-THz power-combined Schottky frequency tripler was designed to handle approximately 30 mW input power. The design of Schottky-based triplers at this frequency range is mainly constrained by the shrinkage of the waveguide dimensions with frequency and the minimum diode mesa sizes, which limits the maximum number of diodes that can be placed on the chip to no more than two. Hence, multiple-chip power-combined schemes become necessary to increase the power-handling capabilities of high-frequency multipliers. However, the traditional power-combining topologies that are used below 1 THz present some inconvenience beyond 1 THz. The use of Y-junctions or hybrid couplers to divide/combine the input/output power at these frequency bands increases unnecessarily the electrical path of the sig-



1.9 THz On-Chip Power-Combining (2 chips).

nal in the range of frequencies where waveguide losses are considerable. Also, guaranteeing a perfect alignment of the very small chips during assembly, in order to preserve the balanced nature of the multiplier, is practically impossible with the subsequent impact on the multiplier performance.

The design presented here overcomes these difficulties by performing the power-combining directly on-chip. Four E-probes are located at a single input waveguide in order to equally pump four multiplying structures (featuring two diodes each). The produced output power is then recombined at the output using the same concept. The four multiplying structures are physically connected on one chip, so that the align-

ment and symmetry of the circuits can be very well preserved. Contrary to traditional frequency triplers, in this design the input and output waveguides are perpendicular to the waveguide channels where the diodes are located. Therefore, the multiplier block is easier to fabricate with silicon micromachining technology instead of regular machining. The expected conversion efficiency of the tripler is ≈ 2 to 3% over a $\approx 20\%$ bandwidth, which is similar to that which is simulated for an equivalent single-chip tripler driven with one fourth the input power.

This work was done by Goutam Chattopadhyay, Imran Mehdi, Erich T. Schlecht, and Choonsup Lee of NASA's Jet Propulsion Laboratory and Caltech; Jose V. Siles – Fulbright

Fellow at NASA's Jet Propulsion Laboratory; Alain E. Maestrini of the University of Paris; Bertrand Thomas of Radiometer Physics; and Cecile D. Jung of ORU for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

*Innovative Technology Assets Management
JPL*

Mail Stop 202-233

4800 Oak Grove Drive

Pasadena, CA 91109-8099

E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-48155, volume and number of this NASA Tech Briefs issue, and the page number.

FPGA Vision Data Architecture

This is an aid to any FPGA vision processing, and can be used by the automotive industry to detect collisions before they occur, and for robotic autonomous navigation for disaster relief.

NASA's Jet Propulsion Laboratory, Pasadena, California

JPL has produced a series of FPGA (field programmable gate array) vision algorithms that were written with custom interfaces to get data in and out of each vision module. Each module has unique requirements on the data interface, and further vision modules are continually being developed, each with their own custom interfaces.

Each memory module had also been designed for direct access to memory or to another memory module. On the development board originally used (an Alpha Data XRC4), there were six independent SSRAM (synchronous static RAM) banks that allowed each module sole access. For a flight mission, there likely would be between one and three memory banks, and arbitration of those banks would need to be supported, interleaving access to individual memory banks between multiple modules.

An FPGA data architecture was required to allow arbitration to onboard DDR (double data rate) and/or SSRAM memory, and to allow up to 10 to 30 independent agents access to that memory. It also required a method of exchanging data directly between modules without reducing the throughput of memory access. This architecture also had to support both low-latency reads and writes, and offer high throughput.

Each FPGA vision module had slightly different input and output re-

quirements. Some required serial access to data, and some were random access. There were 8-bit, 16-bit, and 32-bit input/output widths. Three modules could connect directly together in a series or go directly to memory, depending on runtime configuration options. One of the larger difficulties was posed by the random read access. For industry-standard buses such as AMBA, PLB, or OPB, a single random-read request can take 5 to 10 clock cycles, locking out all other users on the bus until the request was complete. This is far too slow for the vision modules and would effectively reduce performance by 2 to 5 times.

An architecture was created that met the same data throughput as the prior custom interface that had no arbitration. The new architecture also allowed for multiple memory types (DDR, DDRII, SSRAM, NAND memory) without any modification of the FPGA vision modules themselves.

The current Rover Navigation FPGA Vision system contains five vision modules: Rectification, Filtering, Disparity, Feature Detector (via a Harris detector), and Visual Odometry score computation (via a sum of absolute differences operator). Further modules to handle path planning are likely.

Each vision module has an “agent” — an interface to memory for both reads

and writes of different sizes. R32 means a read agent of width 32 bits, and W8 means a write agent of width 8 bits. Each memory bank has a single arbiter that handles all memory requests to its bank. Each agent maps to a single arbiter, but because this mapping will be dependent upon the memory devices used and the number of memory devices available (i.e. two DDR banks vs. six SSRAM banks), there is a large multiplexer called the “vision agent to bank mapping,” which assigns agents to appropriate arbiters and memory banks.

Each agent can queue multiple memory requests and queue multiple responses from memory. This allows bursting of data for high throughput, and decouples the action of requesting memory from the action of receiving data. Many of the vision modules have one part dedicated to computing the location of the next request, and a separate part dedicated to handling the data at that location.

This work was done by Arin C. Morfopoulos and Thang D. Pham of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to the Patent Counsel, NASA Management Office-JPL. Refer to NPO-47869.