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Fabrication of Microstripline Wiring for Large Format Transition Edge Sensor Arrays

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Abstract We have developed a process to integrate microstripline wiring with transition edge sensors (TES). The process includes additional layers for metal-etch stop and dielectric adhesion to enable recovery of parameters achieved in non-microstrip pixel designs. We report on device parameters in close-packed TES arrays achieved with the microstrip process including R_n, G, and T_c uniformity. Further, we investigate limits of this method of producing high-density, microstrip wiring including critical current to determine the ultimate scalability of TES arrays with two layers of wiring.

Keywords Transition edge sensor · Fabrication · Large format array

1 Introduction

Superconducting transition edge sensors have enabled substantial increase in the size of arrays of sensitive cryogenic detectors due to their ease of lithographic fabrication and integrability with multiplexed amplifiers. Here, we explore a more practical aspect of scaling to large format arrays: integration of superconducting microstrip wiring with transition edge sensors. One of the limitations of the pixel pitch and scalability of transition edge sensor arrays is the amount of space one needs to dedicate to the bias wiring in between pixels. We address the specific geometry for single photon microcalorimetric sensors for high photon energies (>100 eV), in which a separate absorber layer is attached to the sensor such that the sensor element and its wiring can be located underneath the absorber.

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For several pixel types and sizes, narrow gaps between the attached photon absorbers have been demonstrated with a number of different assembly techniques [1–5]. In this configuration, wiring can be in the same plane as the pixels but large arrays will then have dense wire bundles. High density wiring has the potential for increased electromagnetic interactions (crosstalk) and decreased yield. In large arrays of small pixels, wiring typically determines the ultimate pixel pitch while contact pad and heatsinking requirements determine the chip size external to the array.

Microstripline geometry, where the pixel bias line and its return are stacked, is a straightforward means of reducing the area needed for wiring as compared to coplanar designs where the bias and return lines run side-by-side. Proper design of microstrip will generate lower magnetic fields due to the bias current than coplanar leads and reduce coupling of higher frequency signals among neighboring bias lines. We have developed a process order that achieves the configuration shown in Fig. 1, integrating multilayer wiring with TES sensors that have all standard components including normal metal noise suppression, overhanging absorbers, and on-chip heatsinking. We have fabricated kilopixel scale arrays using the multilayer wiring as well as coplanar wiring to verify device performance with the new process. We have further explored the limitations of our microstrip procedure in scaling to denser wiring, to examine whether yield and electrical requirements (such as critical current) are met in the smaller wires.

2 Fabrication

We describe a process that integrates superconducting microstripline with a TES bilayer with Au as the noble metal top layer in a kilopixel (32 × 32) microcalorimeter array. The process description starts with our TES-to-lead attachment method and then adds the additional steps to enable the stacked lead arrangement. First, we select thermally oxidized silicon wafers to be coated with a target thickness of low-stress (silicon rich) plasma enhanced chemical vapor deposited (PECVD) SiN. Alignment marks are etched into the dielectric and then the substrate cleaned for TES deposition. We use a high temperature electron beam (e-beam) molybdenum deposition followed by e-beam gold after allowing time for the substrate to cool, but the methods described here are transferrable to any noble metal toplayer (Au, Cu, Ag, Pd, AuPd, etc.). For microstrip leads, we typically add a thin silicon oxide layer before the bilayer deposition to prevent roughening of the nitride membrane surface during subsequent etches.

Standard photolithographic techniques using a contact printer in hard contact will be used for all steps (although methods using different contact modes and optical reduction can also be employed). The Au layer is patterned and ion milled to define the TES detector elements, leaving a continuous Mo sheet on the wafer. Superconducting lead material (in our case, Nb) is then deposited over the entire wafer. This material is patterned to leave rails on both sides of the TES element as well as pads and the wider return line (6 μms wide for the 300 μm pixel). In a coplanar arrangement, the leads would now be complete.

To enable the microstrip lead geometry, a thin layer of e-beam deposited Mo is added to the TES regions to enable adhesion of the insulator. Mo is selected due

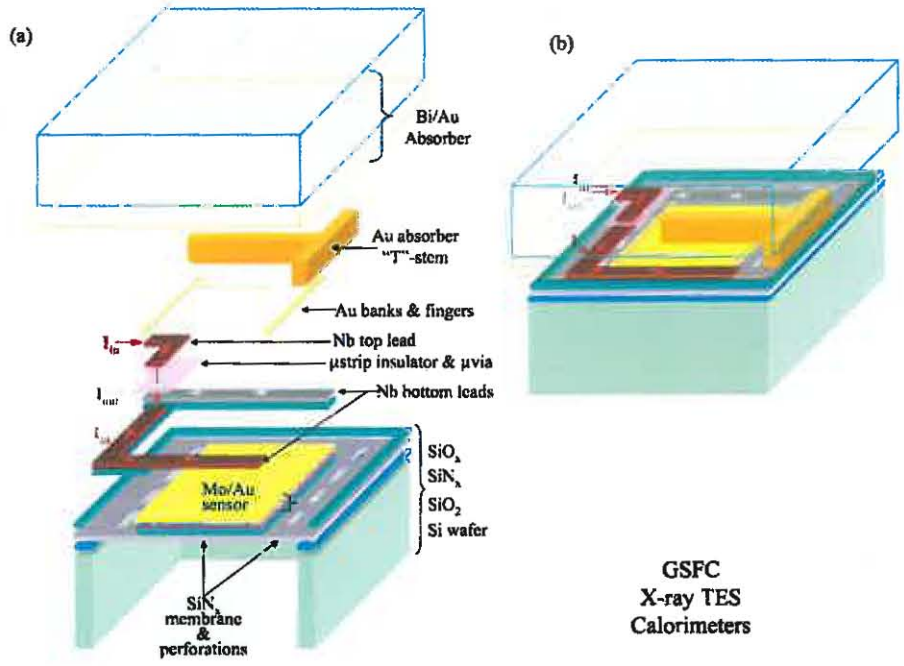

Fig. 1 (Color online) (**a**) A microstripline superconducting transition edge sensor microcalorimeter with backetched membrane and lithographically patterned overhanging absorber. Layers are separated and labeled. Fabrication order is from bottom to top except backetch, which is performed last. (**b**) Current path in the microstripline arrangement is shown. An estimate of the applied field from this wiring arrangement as well as neighboring wire bundles has been calculated

to its low interdiffusion and intermetallic formation with noble metals and its easy removal in fluorine reactive ion etch. A pinhole free insulator (e.g., PECVD SiO_2) is deposited, where the wafer temperature is kept below 200°C to prevent diffusion effects or dramatic resistance changes in the Mo/Au detector element. Vias through the SiO_2 layer to one Nb bias rail (and contact pads as needed) are plasma etched. The base wiring layer is then cleaned with an *in situ* argon sputter and the top lead layer is deposited. After etching the Nb top layer, typically 2/3 of the insulating layer remains, having protected the TES and other regions during the long clean. The insulator over the TES and the adhesion layer is removed using the same dry etch followed by a wet etch removal of the oxide remaining over the exposed membrane regions of the pixel. Thus, the insulating layer in the microstrip is entirely removed from the pixel except the region on top of the leads. The thin oxide underlayer deposited prior to the bilayer remains under the TES and leads but is removed from the open areas of the membrane, allowing the thermal conductance to again be defined by the silicon nitride thickness. The fully defined microstrip circuit is shown in Fig. 2. It is important that the nitride membrane is not roughened in the oxide removal steps to approach the thermal conductance geometry of the non-microstrip design.

This microstrip fabrication technique contrasts with earlier reports [6, 7]. For example the choice of liftoff for lead and insulator regions [6] is less conducive to scaling to tight lead spacing since the method relies on narrow photoresist features

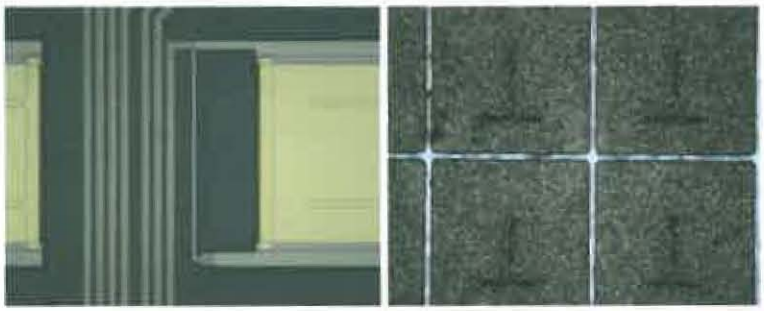

Fig. 2 (Color online) Photomicrographs of a microstripline TES microcalorimeter. *Left*: the device is shown prior to absorber attachment with added oxide and oxide adhesion layers removed. Via is observable at lower wiring rail (*bottom center*). Microstrip geometry and proximity to wiring bundle is typical for the array. *Right*: array detail is shown with devices with completed absorber attachment (photo rotated 90° from left side photo)

between wires that are further narrowed by the undercut required for the liftoff. The SCUBA II fabrication [7] uses similar lead etch but omits the sacrificial Mo adhesion and oxide underlayers. The Mo layer generalizes the described technique to more metal/oxide combinations (e.g. Au and PECVD SiO_2) and it is hoped that the oxide underlayer will promote better uniformity and reproducibility in the membrane thermal conductance.

After the oxides have been removed, the microstrip definition is complete and the device is built up conventionally. Normal metal bars, front side heatsinking, contact pads, and other required metal structures are added via liftoff depositions. Membrane perforations to define the thermal conductance are added with a silicon nitride reactive ion etch. Then a 3–4 μm thick photoresist layer is patterned to provide absorber attachment locations to both the TES and to open areas of the membrane. Typically this "stem" (absorber support post) area is minimized to reduce electrical effects on the TES [8] and hot phonon loss to the membrane [9]. A seed layer (typically Ti/Au) is deposited for electroplating. The absorber film thicknesses (Au for thermalization, Bi for low heat capacity material with reasonable photon absorption cross-section) are electroplated, patterned lithographically and Ar ion milled. While the substrate is positioned at an angle of 20 degrees to the ion mill beam, some photoresist etchback can occur during the etch. In practice, the minimum gap between absorbers will approach the thickness (i.e., about 5 μms in this case).

With all metallization and etches complete, individual array chips can now be yielded from the wafer. The bilayer absorber is susceptible to oxidation and interdiffusion, so an effort is made to keep the heating time and oxygen exposure at elevated temperature to a minimum. The device-side of the wafer is mounted in wax to a backing wafer (at a temperature of 120°C for less than 0.5 hours) and patterned for backetch. After deep reactive ion etching to the thermally deposited silicon dioxide etchstop, the SiO_2 is removed in a wet etch and the wafer is soaked in acetone overnight to remove the wax and photoresist sacrificial layers. Parts are dried in a liquid CO_2 critical point dryer.

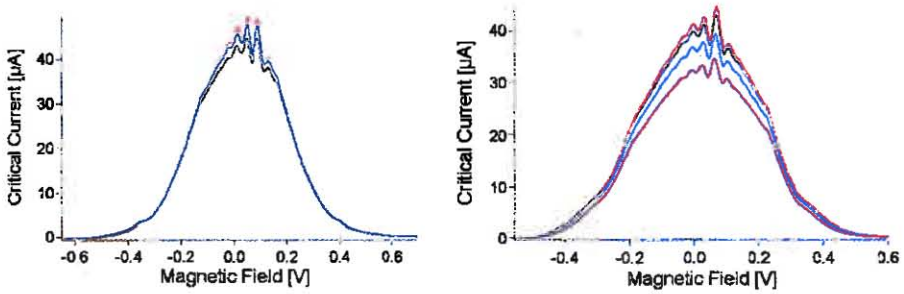

Fig. 3 (Color online) Critical current as a function of applied magnetic field by microstripline wiring is compared in two cases: *left*: when the additional bias currents are applied to six more distant pixels in the array and *right*: when two of the six additional pixels are biased in the array are nearest neighbors

3 Design and Testing

Testing of large format arrays we have produced using this microstripline technique is in progress. We have a few measurements available but await a larger statistical sample to report full uniformity and reproducibility results. We can, however, discuss the basic electronic performance of the arrays and infer some design requirements from them.

Devices showed low sensitivity to magnetic field generated from the bias when microstripline wiring was integrated. In Fig. 3, measurements are shown on typical pixels within the microstrip kilopixel array when other pixels are biased at high currents. In each case, six other pixels are biased such that their bias currents run close to the measured pixel, though on the righthand plot, some of the six pixels are also located near to the measured pixel in the array. The $I_c(B)$ curve of these pixels is known to be a sensitive measurement of fields applied to the TES devices [8, 9]. When the neighbors are biased at high currents, the heat generated is sufficient to suppress the magnitude of the critical current (through local increase in the base temperature of the silicon frame) without perceptibly shifting the magnetic field sensitive features in the data. The $I_c(B)$ curve shows no change in location of the peaks in I_c, indicating that a negligble field is applied by the nearby bias. The reduction of amplitude of I_c on the righthand figure indicates thermal effects from dissipation in the nearby pixels. Results were independent of polarity and reproduced with raising the bath temperature at zero bias.

These encouraging observations are consistent with realizing the benefits of microstrip field cancellation as indicated by a simple calculation of the fields applied in our detector geometry. The Biot-Savart first order fields generated by the self-cancelling pair of wires in the microstrip (300 nm wire separation) are three orders of magnitude lower than that of the coplanar wiring (4 μm wire separation) at practical distances (20–100 μms).

Device parameters and the ultimate limits of microstripline using our fabrication procedure in TES arrays have been investigated. Microstripline arrays with TES operation temperatures (bilayer T_{cs}) of 85 mK and 155 mK have been fabricated and tested. In each case, the thermal conductance G of the SiN membrane was measured

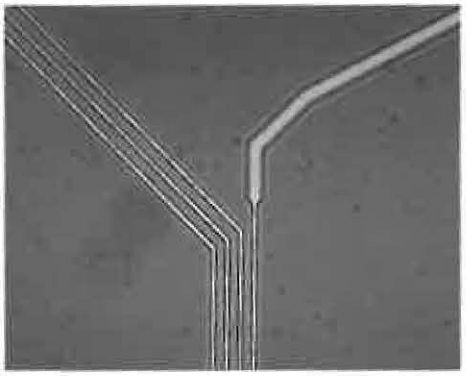

Fig. 4 (Color online) Microstripline wiring with a 1 μm wide top lead on a 2 μm wide bottom layer has been fabricated for critical current measurement

using device current-voltage (IV) characteristics and complex impedance as a function of bias. G (0.1 K) varied from the expected value of 250 pW/K for the high temperature device to 400 pW/K in the low temperature design. However, the cause of the variation is still being investigated and we are not certain if it can be attributed to the incorporation of microstrip or some other material (e.g. SiN membrane) or a change in the heatsinking requirements of the silicon frame at the different operating temperatures.

Narrower wires and spacing between wires will enable larger arrays. A estimate of the achievable size of array ($N \times N$) where $N^2/4$ pixels are wired in N muntons is $c \sim N/4$ where c is the wirecount in an interpixel bundle. The interpixel spacing divided by w, the sum of the wire width and spacing, determines the maximum wirecount for an array. In our 32 × 32 array, 80 micron interpixel spacing is populated with $w = 9$ micron such that $c = 8$ wire pairs per bundle are allowed. The relatively wide microstrip on the 9 μm pitch (6 micron bottom lead and 3 μm top lead) carried in excess of 5 mA at low temperatures. We produced several wire patterns using the device process reported above to determine whether the process scales to finer-wire lithography. Figure 4 shows, in the narrowest region, a 1 μm wire atop a 2 μm return line. The 2 μm lines were observed to carry greater than 2 mA currents at low temperature while the 1 μm measurements are underway. A 4 μm pitch microstripline would enable an 80 × 80 array maintaining the same munton width of the current design.

In conclusion, we have demonstrated a process for production of microstripline TES arrays. Benefits of the low magnetic field have been realized while device parameter variance is under study. Initial attempts to scale to ultrafine wiring suggest that a 4 μm wire pitch microstripped 6400 element array is feasible in our 300 μm absorber design. Our future work will concentrate on high performance wiring for enabling these larger formats.

References

1. R.L. Kelley, The microcalorimeter spectrometer on the Astro-E X-ray observatory. Nucl. Instrum. Methods A **444**, 170–174 (2000)
2. N. Tralshawala et al., Design and fabrication of superconducting transition edge X-ray calorimeters. Nucl. Instrum. Methods A **444**, 188–191 (2000)

3. H. Kudo et al., Fabrication of an X-ray microcalorimeter with an electrodeposited X-ray microabsorber, in *Low. Temp. Det.* AIP 0-7354-0049-0, ed. by F.S. Porter (2002), p. 235
4. W.B. Doriese et al., 14-pixel, multiplexed array of gamma-ray microcalorimeters with 47 eV energy resolution at 103 keV. Appl. Phys. Lett. **90**, 193508 (2007)
5. S.J. Moseley, C.A. Allen, N. Costen, R. Kelley, C. Kilbourne, T. Miller, Automated Hybridization of X-Ray Absorber Elements: A Path to Large Format Microcalorimeter Arrays (2008), pp. 418
6. D.M. Glowacka, D.J. Goldie, S. Withington, M. Crane, V. Tsaneva, M.D. Audley, A. Bunting, A fabrication process for microstrip-coupled superconducting transition edge sensors giving highly reproducible device characteristics. J. Low Temp. Phys. **151**(3), 249–254 (2008)
7. M.D. Audleya et al., Fabrication of the *SCUBA*-2 detector arrays. Nucl. Instrum. Methods Phys. Res. **520**, 483–486 (2004)
8. S. Smith et al., Implications of weak-link behavior on the performance of Mo/Au bilayer transition-edge sensors. J. Appl. Phys. (2012, submitted)
9. M.E. Eckart et al., Kilopixel X-ray microcalorimeter arrays for astrophysics: device performance and uniformity. Proceedings LTD14, J. Low Temp. Phys. (2012)