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Lead-Free Experiment in a Space Environment

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July 2012

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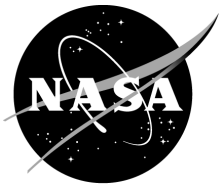

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LIST OF ACRONYMS AND SYMBOLS

AWG	American Wire Gauge
BGA	ball grid array
CH	channel
COTS	commercial off-the-shelf
CSP	chip scale package
Cu	copper
CxP	Constellation Program
DIP	dual in-line package
HASL	hot-air solder level
ImAg	immersion silver
IMC	intermetallic compound
ISS	International Space Station
JCAA/JG-PP	Joint Council on Aging Aircraft/Joint Group on Pollution Prevention
LPI	liquid photoimagable
LTESE	Lead-Free Technology Experiment in Space Environment
MISSE-7	Materials International Space Station Experiment-7
MSFC	Marshall Space Flight Center
Pb	lead
PBGA	plastic ball grid array
PEC-A	passive experiment container-A

LIST OF ACRONYMS AND SYMBOLS (Continued)

PEC-B	passive experiment container-B
QFP	quad flat pack
RoHS	Reduction of Hazardous Substances
SEM	scanning electron microscope
Sn	tin
TQFP	thin quad flat pack
XRF	x-ray fluorescence

NOMENCLATURE

g	gravity
Tg	glass transition temperature
ΔT	temperature excursion

TECHNICAL MEMORANDUM

LEAD-FREE EXPERIMENT IN A SPACE ENVIRONMENT

1. INTRODUCTION AND BACKGROUND

Due to the enactment of the Reduction of Hazardous Substances (RoHS) directive by the European Union and lead (Pb) reduction efforts by a number of Asian countries, the majority of electronic part manufacturers are producing only Pb-free parts, and the probability of Pb-free hardware being delivered to NASA and military programs, both inadvertently and in commercial off-the-shelf (COTS) systems, is high.

NASA's Constellation Program (CxP) Workmanship Requirements (CxP 70165) prohibited use of Pb-free technology. The Joint Council on Aging Aircraft/Joint Group on Pollution Prevention (JCAA/JG-PP) Lead-Free Solder Project Joint Test Report published July 27, 2007, recommended that the next steps for aerospace and defense Pb-free applications include experiments to gather data in operational environments. Ground testing of Pb-free solder has been performed but no testing of launch and space exposure has been performed for comparison.

NASA engineering technical authority requires space environment data in order to realistically determine risk and make recommendations to Materials Review Boards when Pb-free technology is inadvertently incorporated into flight hardware and to project offices when COTS systems are proposed for incorporation. To date, these evaluations and recommendations have been limited to conservative extrapolations based on ground test data. As the risk of Pb-free technology incorporation increases, it is necessary to more fully understand the impacts of this technology to enable efficient engineering mitigation.

2. OBJECTIVES

The Lead-Free Technology Experiment in Space Environment (LTESE) objectives are as follows:

- Obtain Pb-free technology reliability data in a space environment for comparison to ground test data.

- Capture lessons learned regarding safe conditions and durations for inadvertent use of Pb-free technology in flight hardware.

3. APPROACH AND METHODOLOGY

The LTESE implementation approach is summarized as follows:

- Build a small experiment containing Pb-free, mixed (Pb-free parts with tin/lead (Sn/Pb) solder, and control (Sn/Pb solder) test vehicles.
- Expose the assembly to launch and then to space for a time.
- Record the events and failures in the same enclosure.
- Record temperature and resistance 10 times an hour to give an accurate thermal environments history.
- Perform failure analysis of the solder joints upon return including visual inspection, x-ray examination, and microsectioning.

3.1 Test Vehicles and Data Board

The LTESE assembly contained the following three test board types:

- Pb-free parts/Pb-free board/Pb-free solder to represent a COTS system.
- Pb-free parts/SnPb board/SnPb solder to represent the inadvertent incorporation of Pb-free parts.
- SnPb parts/SnPb board/SnPb solder as a control board.

The test boards were double-sided, epoxy glass, high glass transition temperature (Tg) (170 °C) printed wiring boards with 1-oz. copper (Cu) foil. They were built by Sierra Proto Express to comply with the requirements of IPC-6012, Class 3/A. The control boards and the mixed alloy boards had a SnPb hot-air solder leveled (HASL) finish, and the Pb-free boards had an immersion silver (ImAg) finish. All test boards had liquid photoimagable (LPI) solder mask over bare Cu and nonsolder mask defined pads. Prior to assembling the boards, they were exposed to x-ray fluorescence (XRF) spectroscopy using a Fisherscope XDAL X-Ray Fluorescence Measurement System to verify that the finish was as ordered. On the HASL boards, XRF established that the mean percentage of Sn was 66.02% and of Pb was 33.98%. On the ImAg boards, XRF established that there was 15.08 μin of Ag over pure Cu.

Each test board contained daisy-chained dummy parts mounted on one side only, and each daisy-chained part forms one test circuit, except that all 27 chip resistors form a single circuit.

The parts were plastic ball grid arrays (BGAs), chip scale packages (CSPs), thin quad flat packs (TQFPs), plastic dual in-line packages (DIPs), and chip resistors. They were populated with multiple devices to increase the number of each type of joint. Each test board contained 1,464 solder joints under test.

The data board was an eight-layer printed wiring board with 1-oz Cu on all layers. It was built by Sierra Proto Express to comply with the requirements of IPC-6012, Class 3/A. The board was HASL and had LPI solder mask over bare Cu and nonsolder mask defined pads. Parts were mounted on both sides of the board. The data board was not Pb-free and did not use radiation-hardened parts.

The circuit boards (see figs. 1 and 2) were vapor phase soldered. The Sn/Pb solder used was Sn63Pb37 eutectic solder and the Pb-free solder used was Sn3Ag0.5Cu (SAC305). The SnPb boards and the mixed alloy boards were soldered using a 217 °C vapor and the Pb-free board used a 240 °C vapor. All boards were vapor degreased after assembly, baked out, and conformally coated with Solithane 113-300.

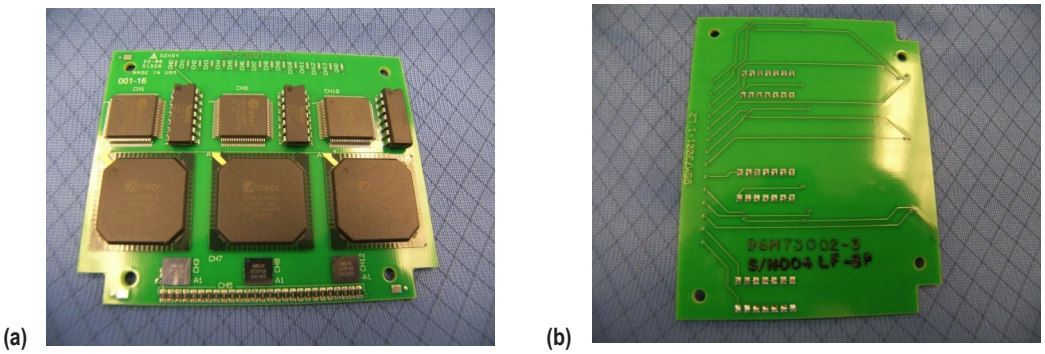

Figure 1. Test board (a) top and (b) bottom.

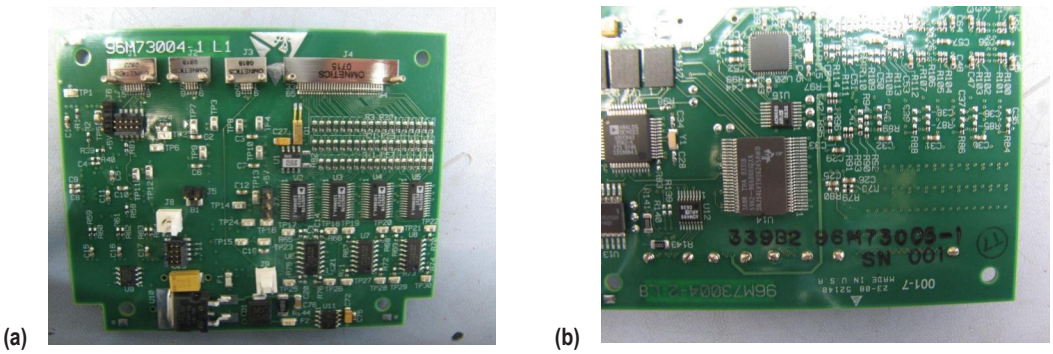

Figure 2. Data board (a) top and (b) bottom.

3.2 Housing

The housing (see fig. 3) was machined from 6061T6 aluminum, which is typical of NASA electronics housings. It was finished with a chemical conversion coating per MIL-DTL-5541, Type II, Class 3.

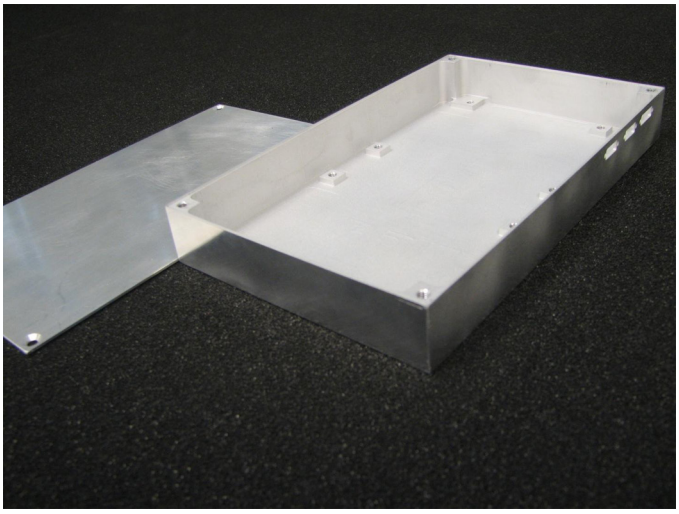

Figure 3. LTESE housing.

3.3 X-Ray Fluorescence and X-Ray Results of Part Lead Finish

The piece parts used were daisy-chained dummy parts. The CSPs, quad flat packs (QFPs), and PBGAs were procured from Practical Components, Inc. The DIPs were procured from TopLine Corporation. The 0805 0-Ω resistors were obtained through Allied Electronics (comp) and are Vishay Dale CRCW08050000ZSTA-ND (Allied P/N 895-2671 (SnPb)) and CRCW08050000Z0EA (Allied P/N 895-3913 (SAC305)).

When the piece parts were received, the finish on the leads was verified using XRF. Certain assumptions had been made about the Pb finishes that were proven incorrect by the XRF. The SnPb finish was believed to be Sn63/Pb37, which was the case on the CSPs and the PBGAs; however, the finish on the DIPs and the QFPs was Sn85/Pb15. It was also assumed that the Pb-free 0805 resistor finish was 100% Sn but was actually SAC305.

Daisy chaining was verified using a Phoenix Microfocus X-Ray System. The x-rays showed that all samples checked were daisy chained. Table 1 lists the XRF and x-ray results.

Table 1. XRF and x-ray results.

Part Type	Part Number	Finish	XRF Results		Daisy Chained
0805 0-Ω resistor	895-3913	Pb-free	Sample 1	SAC 305	Yes
			Sample 2	SAC 305	Yes
	895-2671	SnPb	Sample 1	Sn63/Pb37	Yes
			Sample 2	Sn63/Pb37	Yes
14 lead DIP	DIP14M3-TIN-DE	Pb-free	Sample 1	Sn	Yes
			Sample 2	Sn	Yes
	DIP14M3-DE	SnPb	Sample 1	Sn85/Pb15	Yes
			Sample 2	Sn85/Pb15	Yes
98 lead CSP	30621	Pb-free	Sample 1	SAC 405	Yes
			Sample 2	SAC 405	Yes
	30620	SnPb	Sample 1	Sn63/Pb37	Yes
			Sample 2	Sn63/Pb37	Yes
100 lead QFP	30989	Pb-free	Sample 1	Sn	Yes
			Sample 2	Sn	Yes
	30767	SnPb	Sample 1	Sn85/Pb15	Yes
			Sample 2	Sn85/Pb15	Yes
256 lead PBGA	30443	Pb-free	Sample 1	SAC 405	Yes
			Sample 2	SAC 405	Yes
	30447	SnPb	Sample 1	Sn63/Pb37	Yes
			Sample 2	Sn63/Pb37	Yes

3.4 Lead-Free Technology Experiment in Space Environment Assembly

The LTESE (see fig. 4) used Omnetics microconnectors and all wires in the internal harness were 30 AWG Cu. All boards were soldered, the harness was fabricated, and the box was assembled by the Electronic Fabrication and Test Team in the Space Systems Department of the Marshall Space Flight Center.

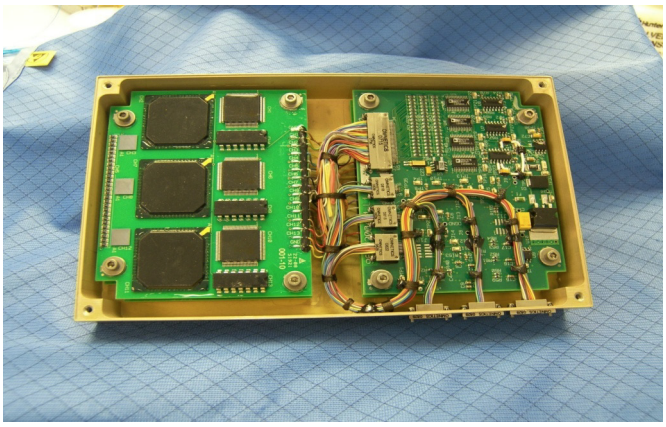

Figure 4. LTESE assembly with the cover removed.

The LTESE package was designed to fit the small space allocated for it. It is $7 \times 4.25 \times$ 0.92 in and weighs 417 gm/0.92 lb. The LTESE was located on the underside of the experiment base plate on the wake side of passive experiment container-B (PEC-B) on Materials International Space Station Experiment-7 (MISSE-7) (see figs. 5 and 6).

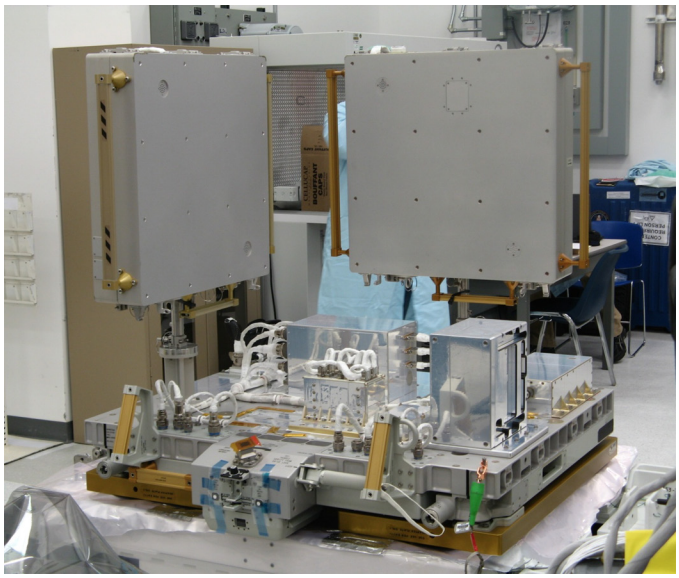

Figure 5. MISSE-7 PEC-B and PEC-A on the express logistics carrier.

Figure 6. MISSE-7 PEC-B and PEC-A with covers removed.

LTESE was launched as part of MISSE-7 on STS-129 on November 16, 2009. Spacewalker Randy Bresnik completed installation of the MISSE-7 experiment on ExPRESS Logistics Carrier 2 on November 22, 2009, and it was first powered up on the International Space Station (ISS) on November 23, 2009. A ground unit, operating in parallel for comparison, was powered up on December 4, 2009, and ran until May 20, 2011. Temperature limits for PEC-B were set by the Naval Research Laboratory at 40 to –40 °C and it was initially estimated that PEC-B would be powered down because of out-of-limit temperatures for approximately 70 days out of the scheduled year of exposure to space.

PEC-B overheated unexpectedly on January 31, 2011, and was powered down. It was powered back up on February 2, 2011, and had overheated again within two orbits. The most probable cause of the overheating was determined to be a fault in the PEC-B computer. Because of potential for continued overheating and PEC-B outgassing and adversely affecting other science on the ISS, it was powered down and remained off until MISSE-7 was removed from the ISS on May 20, 2011, and returned to Earth on STS-134 on June 1, 2011. On July 18, 2011, the LTESE was removed from the MISSE-7 PEC-B base plate and returned to ES43 for evaluation.

4. RESULTS

The ground unit that had operated in the laboratory from December 4, 2009, until May 20, 2011, never showed any hard failures. On July 25, 2011, the flight unit was powered up in the laboratory for a preliminary look at the flight data. There were no hard failures of any of the solder joints. Intermittent failures would not show up until the resistance measurements were downloaded from the memory on the data board.

Both the ground and flight units (see figs. 7 and 8) were disassembled, photographed, and visual observation made of the test and data boards. It was noted that the location of the control test board and Pb-free test board were reversed from what was shown on the assembly drawing on both units. Because of this, it was verified with XRF that the actual build of the test boards was as marked on the boards.

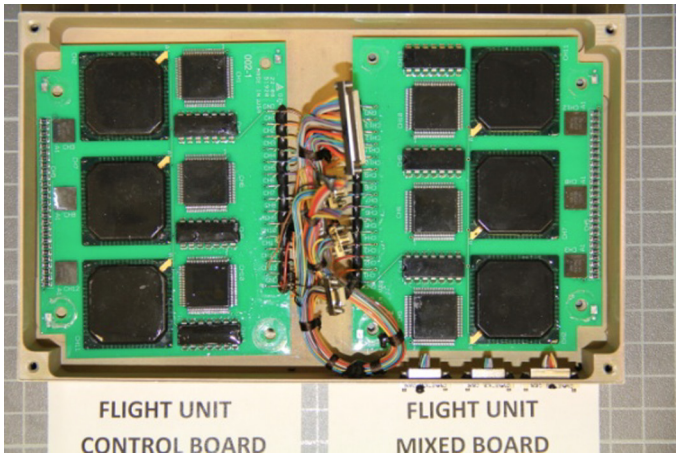

Figure 7. Flight unit bottom level.

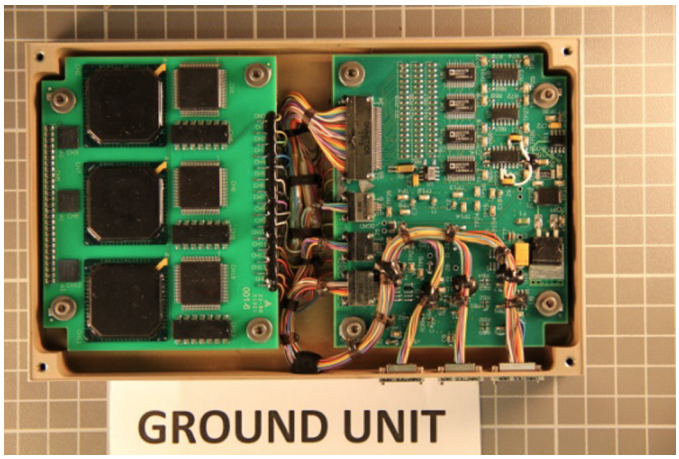

Figure 8. Ground unit top level.

Visual observation at the time of disassembly showed all boards to be in excellent shape, and no signs of degradation were present. Low-power inspection showed no Sn whiskers or Sn pest on either the test or data boards.

The test boards were x-rayed for comparison with the preflight x-rays. No differences were observed. One thing that was observed on all test boards (preflight and postflight) was the high degree of voiding seen on the 0805 chip resistors. Figures 9–12 show the voiding on these chip parts.

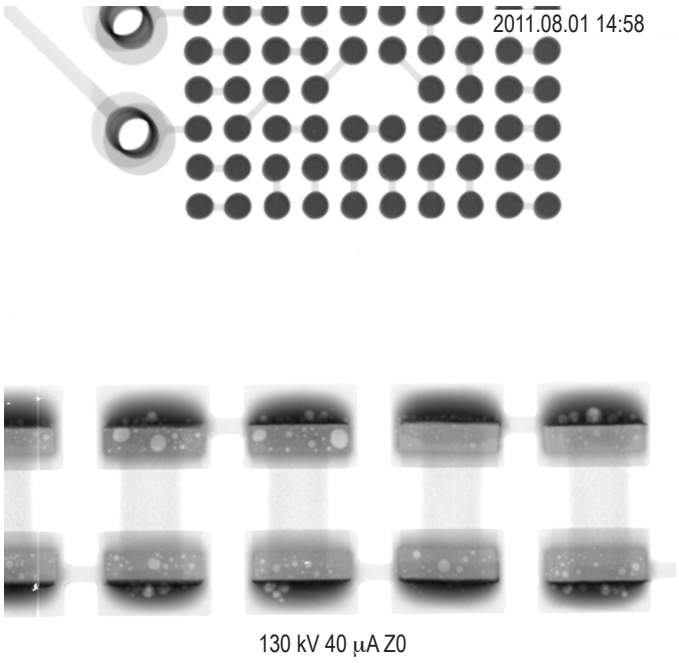

Figure 9. Mixed solder postflight.

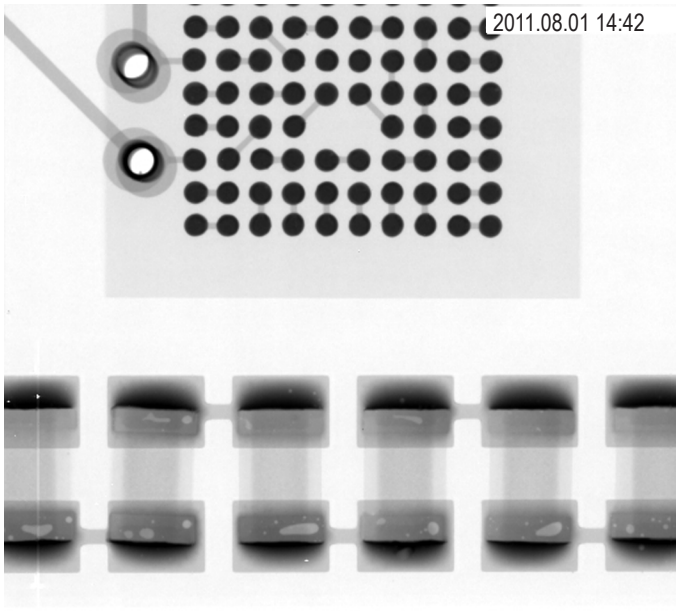

Figure 10. SnPb/SnPb solder postflight.

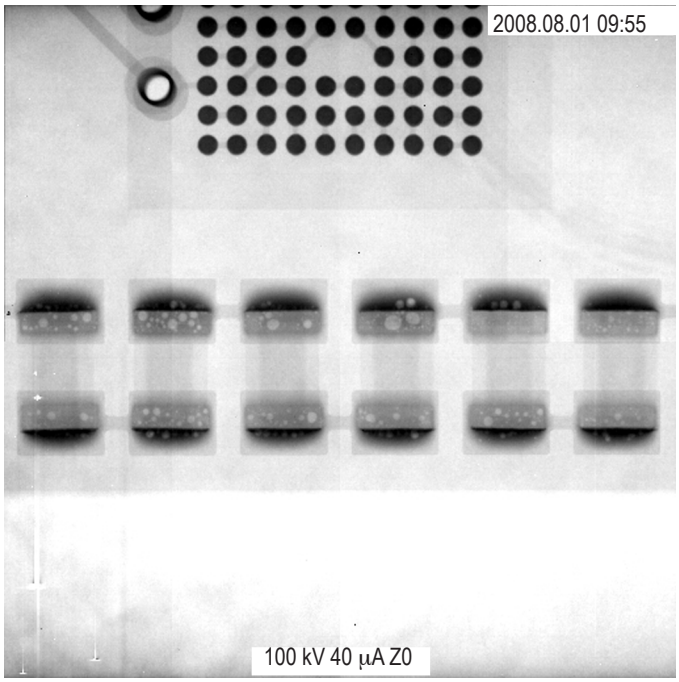

Figure 11. Mixed solder preflight.

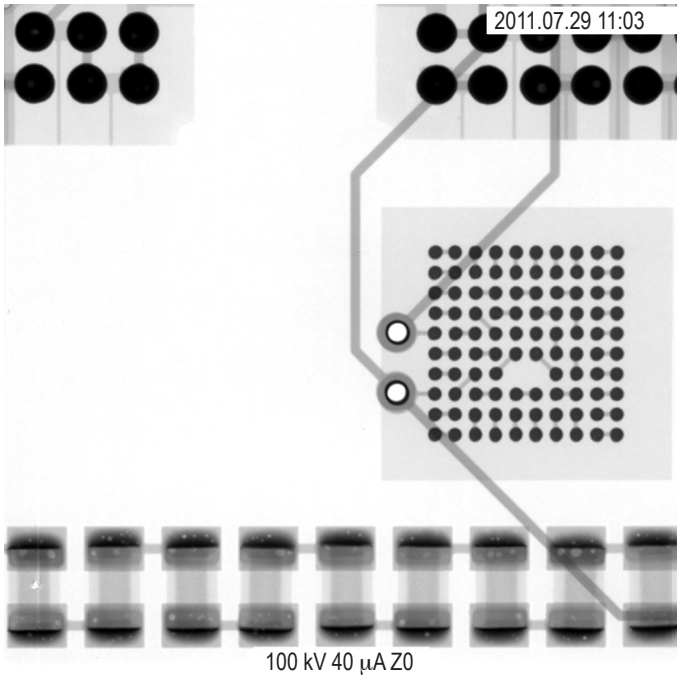

Figure 12. Pb-free solder postflight.

The ground unit boards were then inspected at × 200 magnification for Sn whiskers and none were seen. The LTESE boards were next inspected at × 1,000 magnification for Sn whiskers. A few whiskers were observed on the knees of the pure Sn plated DIPs on the flight unit mixed solder board (see figs. 13–15). They ranged from 13 to 18 μm in length. There were possibly some whiskers starting on the flight unit Pb-free board but were too small even at × 1,000 magnification to be sure. Scanning electron microscope (SEM) pictures were not taken because of charging issues with the conformal coating on the boards. Figures 13–15 are for channel (CH) 4 of 13 channels and the DIP was a 14-pin device.

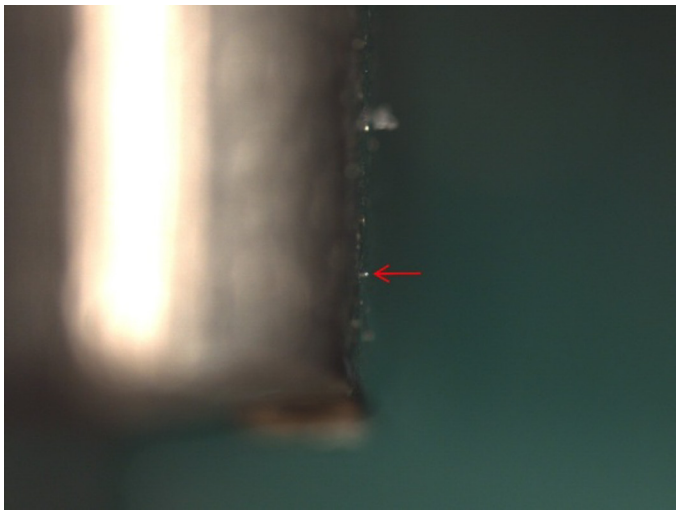

Figure 13. Flight mixed solder board CH4 DIP, lead 10 of 14, 13-µm whisker, × 100 magnification.

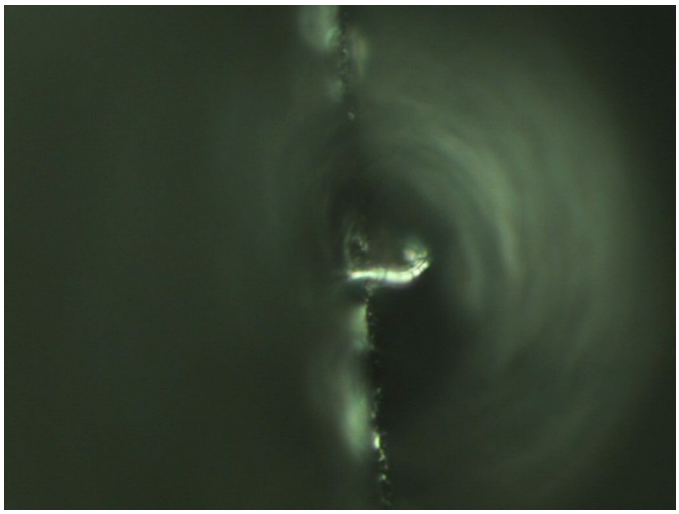

Figure 14. Flight mixed solder board CH4 DIP, lead 10 of 14, 13-µm whisker, × 1,000 magnification.

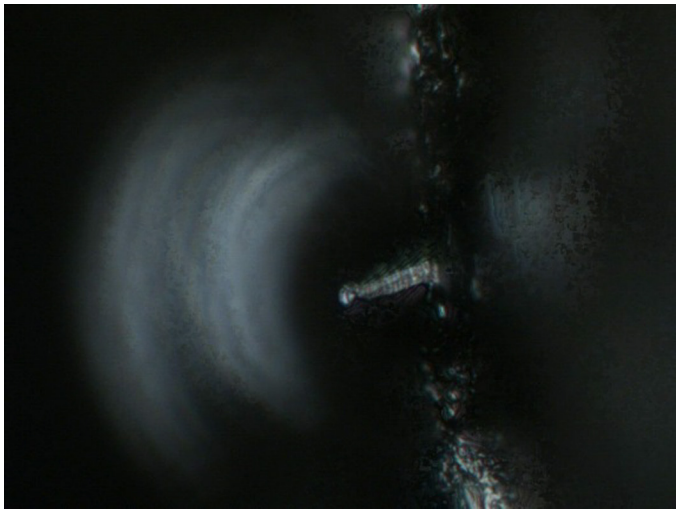

Figure 15. Flight mixed solder board CH4 DIP, lead 2 of 14, 18-μm whisker.

The LTESE flight data were downloaded from the data system board and converted from the recorded form of 'counts' to temperatures and resistances. It is ≈360 days of data with one set of measurements (39 resistance and 2 temperature measurements) taken every 6 min. The board temperature is a measurement taken in free space on the LTESE data system board and ranged from –26 to 45 °C. The processor temperature is a temperature measurement taken from the core of the LTESE processor and ranged from 12.5 to 82 °C. The board temperature excursion (ΔT) over a single orbit was small and ranged from 13 °C when ambient temperatures were low to 23 °C when ambient temperatures were high. The processor temperature ΔT was a nearly constant 14 °C, and what little change there was took place over a matter of days. The resistances of the test solder joints all read zero except for the CSPs, which were initially in the 60-Ω range. Each device channel sample was a 12-bit value but it was necessary to drop the lowest 4 bits for it to fit in the FLASH memory. The zero count could really be any number between 0 and 4 Ω. The measured CSPs resistances ranged from 49 to 62 Ω.

The LTESE ground data were downloaded and converted. The board temperatures ranged from 17 to 36 °C and the processor temperature ranged from 12 to 82 °C.

Microsections were made for comparison with preflight microsections. Figures 16–25 show that there was very little intermetallic compound (IMC) growth over time in any of the three solder types tested in either the flight or ground units compared to the preflight IMC. These figures are of CSP joints, but other types of part joints reflect the same thing (see figs. 26–60).

Figure 16. Pb-free/Pb-free chip scale package joint: Preflight.

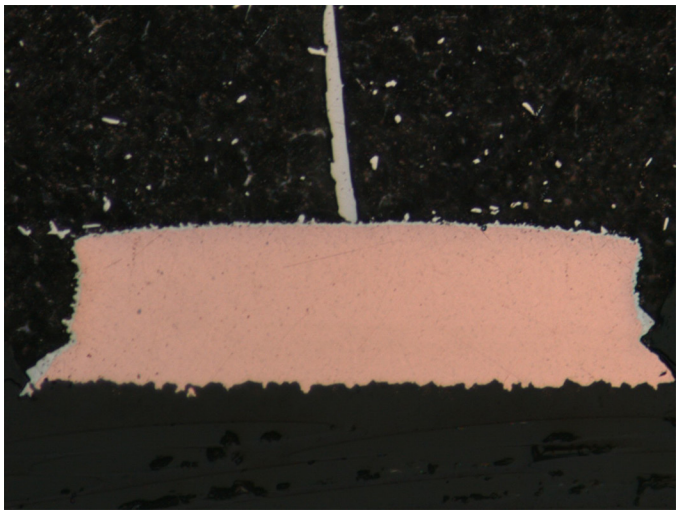

Figure 17. Pb-free/Pb-free chip scale package joint: Postflight, flight unit.

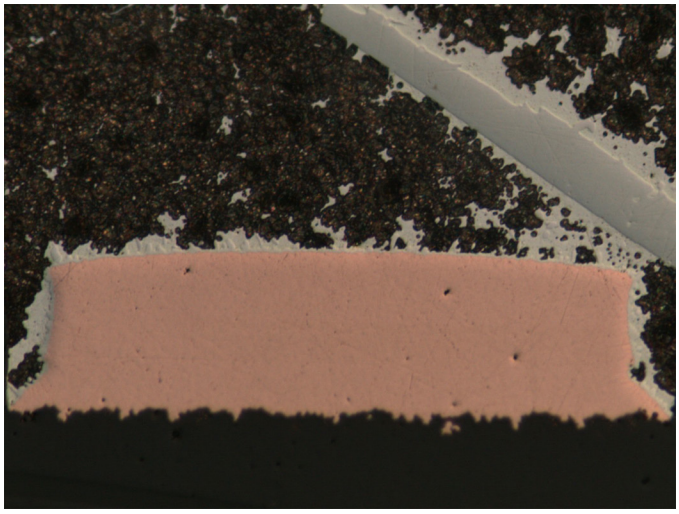

Figure 18. Pb-free/Pb-free chip scale package joint: Postflight, ground unit.

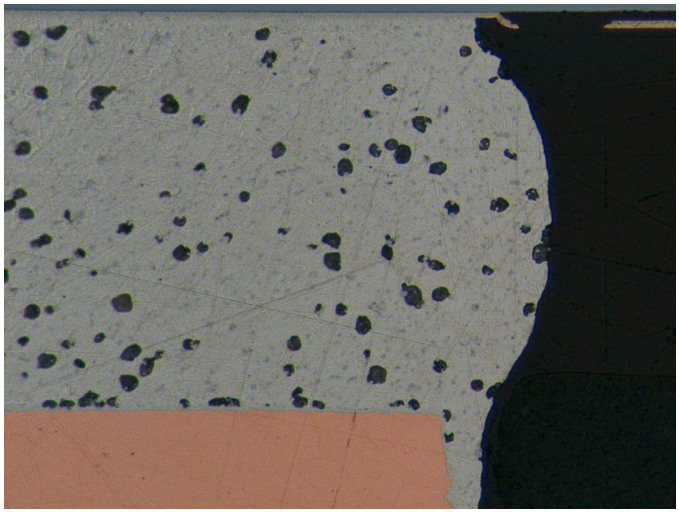

Figure 19. Pb-free/SnPb chip scale package joint: Preflight.

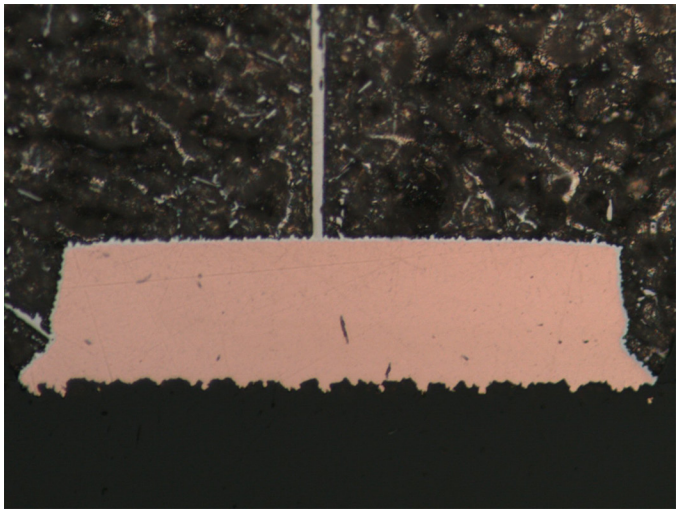

Figure 20. Pb-free/SnPb chip scale package joint: Postflight, flight unit.

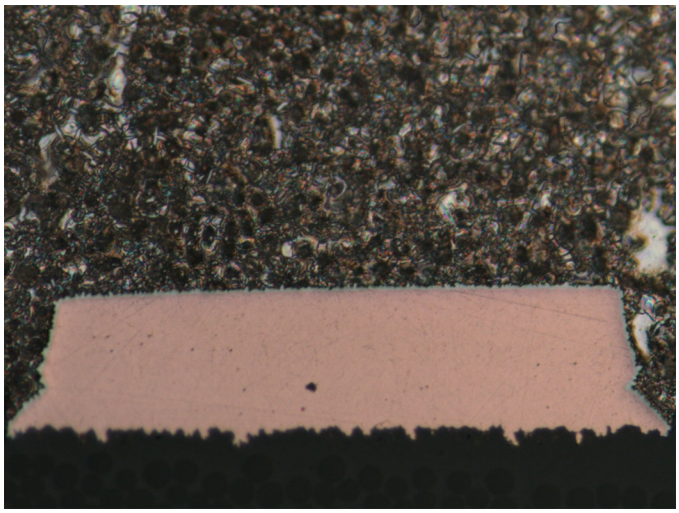

Figure 21. Pb-free/SnPb chip scale package joint: Postflight, ground unit.

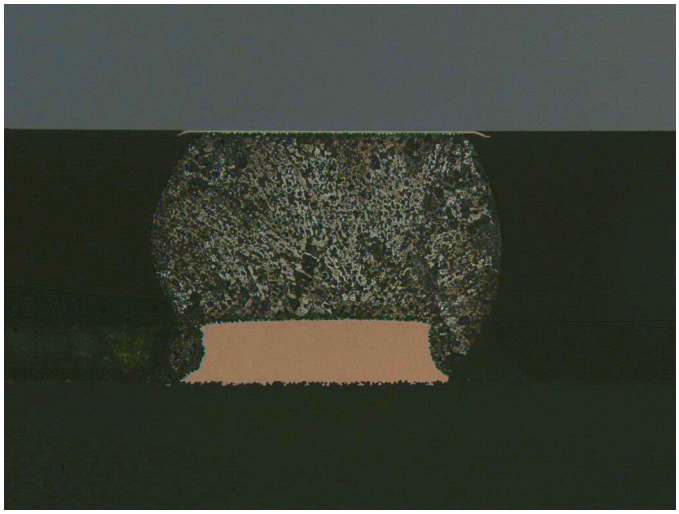

Figure 22. SnPb/SnPb chip scale package joint: Preflight.

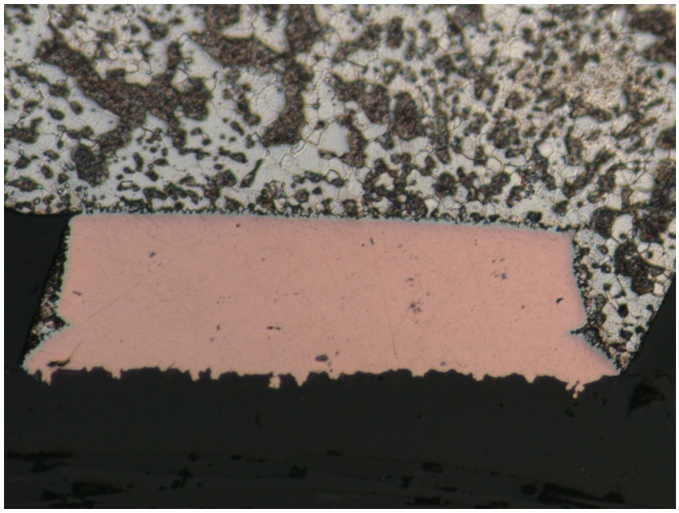

Figure 23. SnPb/SnPb chip scale package joint: Postflight, flight unit.

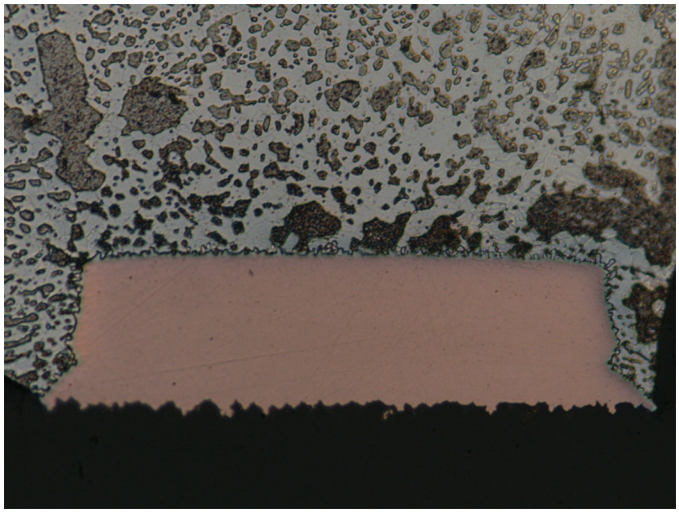

Figure 24. SnPb/SnPb chip scale package joint: Postflight, ground unit.

Figure 25. Mixed solder: TQFP preflight.

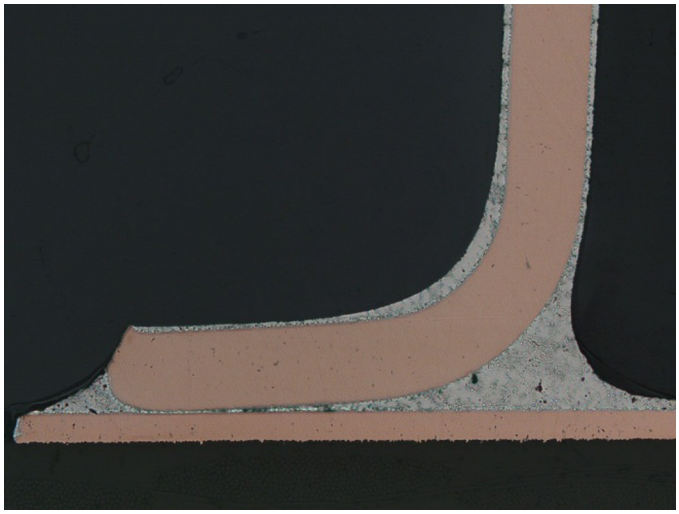

Figure 26. Mixed solder: TQFP postflight, flight unit.

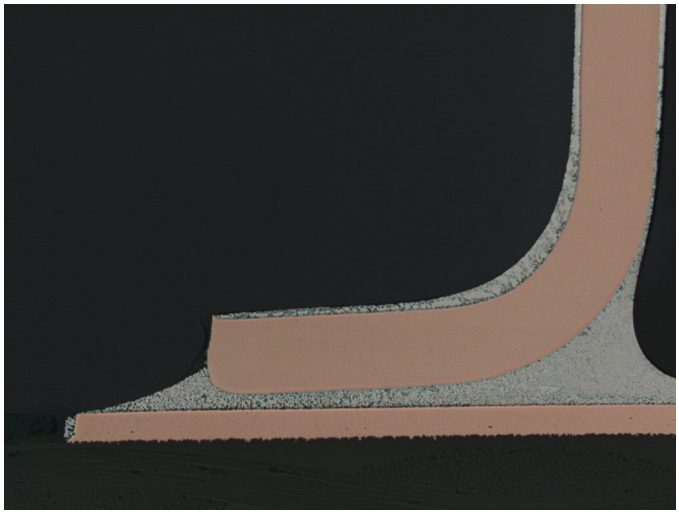

Figure 27. Mixed solder: TQFP postflight, ground unit.

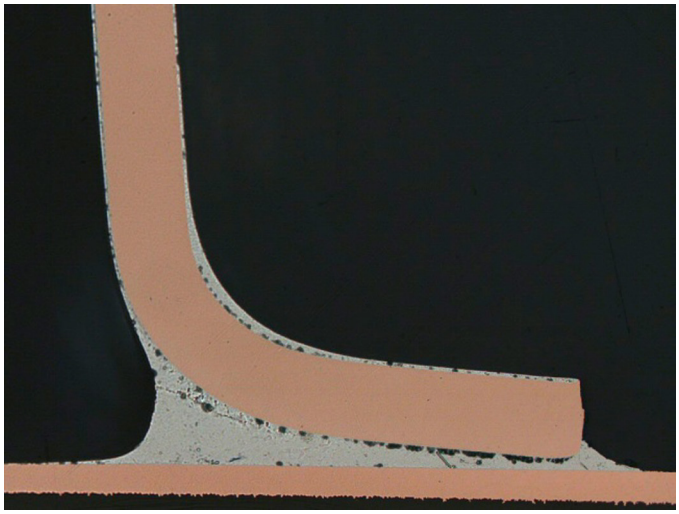

Figure 28. Pb-free solder: TQFP preflight.

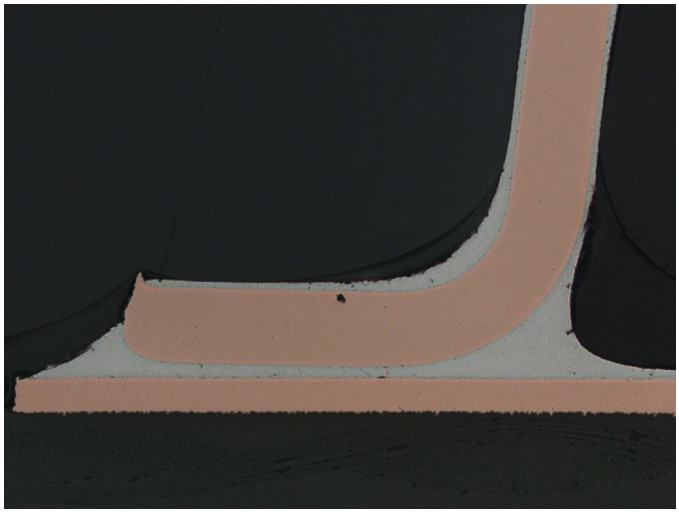

Figure 29. Pb-free solder: TQFP postflight, ground unit.

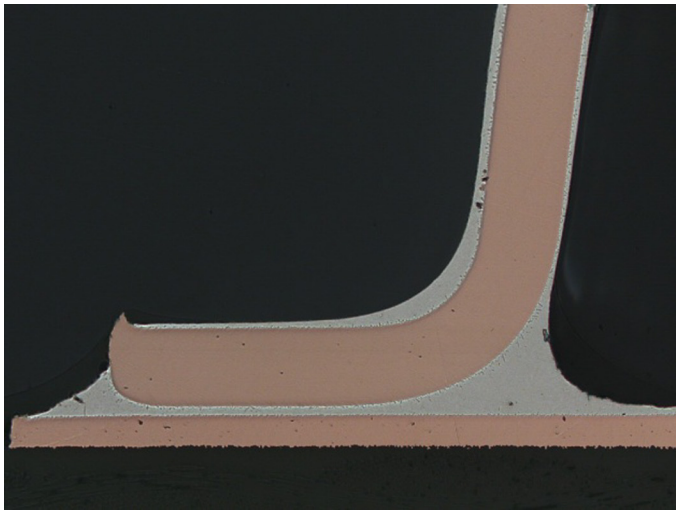

Figure 30. Pb-free solder: TQFP postflight, flight unit.

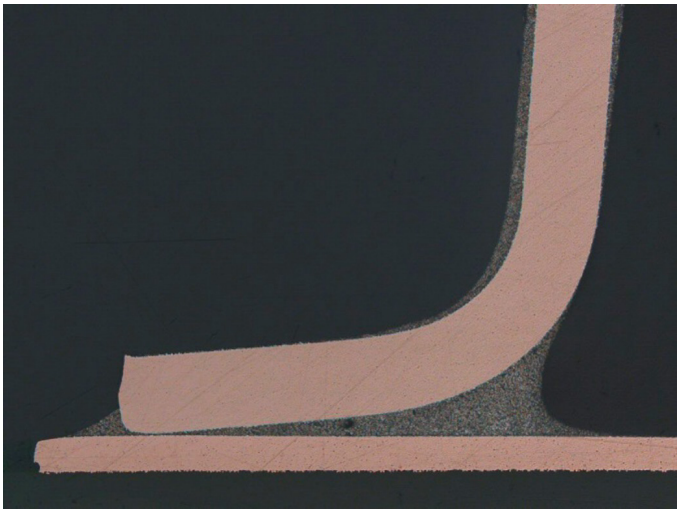

Figure 31. Sn/Pb solder: TQFP preflight.

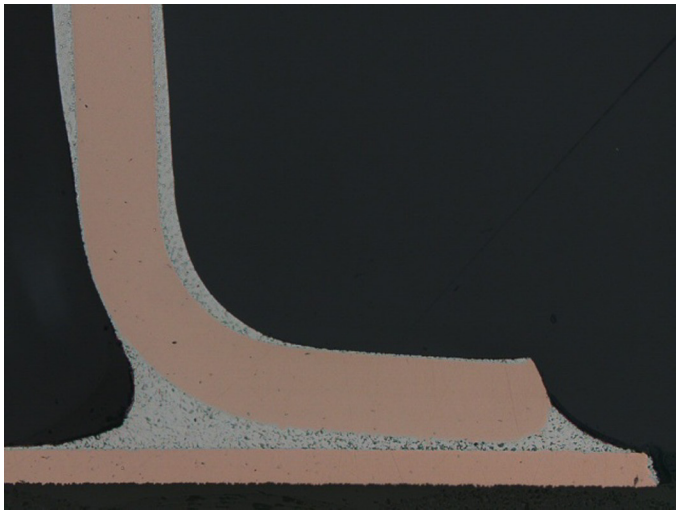

Figure 32. Sn/Pb solder: TQFP postflight, flight unit.

Figure 33. Sn/Pb solder: TQFP postflight, ground unit.

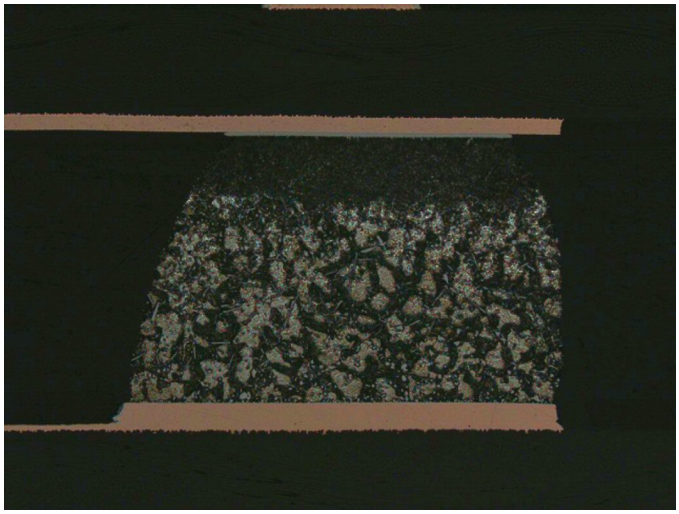

Figure 34. Mixed solder: PBGA preflight.

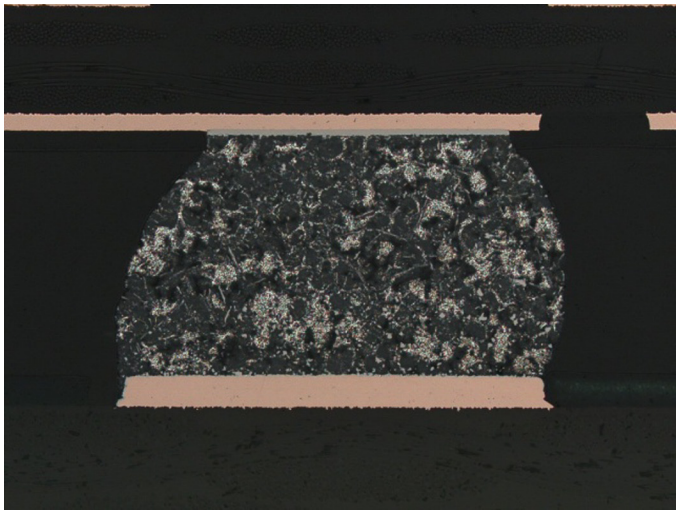

Figure 35. Mixed solder: PBGA postflight, flight unit.

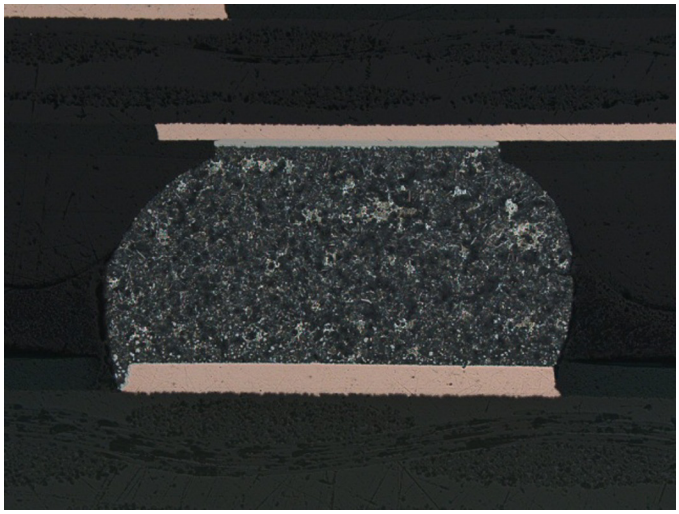

Figure 36. Mixed solder: PBGA postflight, ground unit.

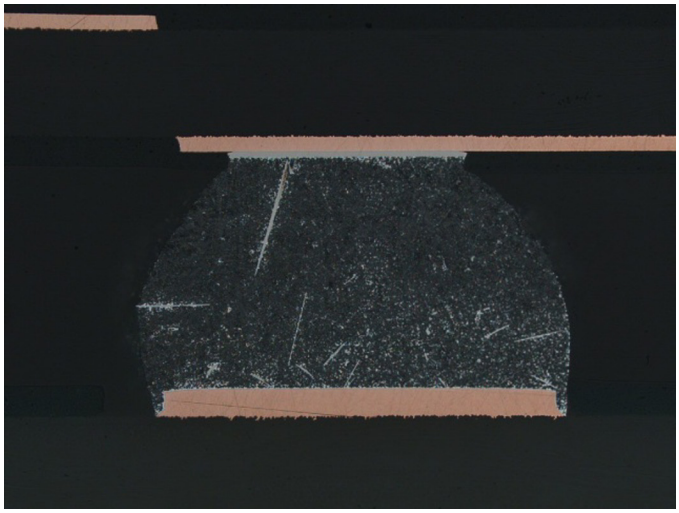

Figure 37. Pb-free solder: PBGA preflight.

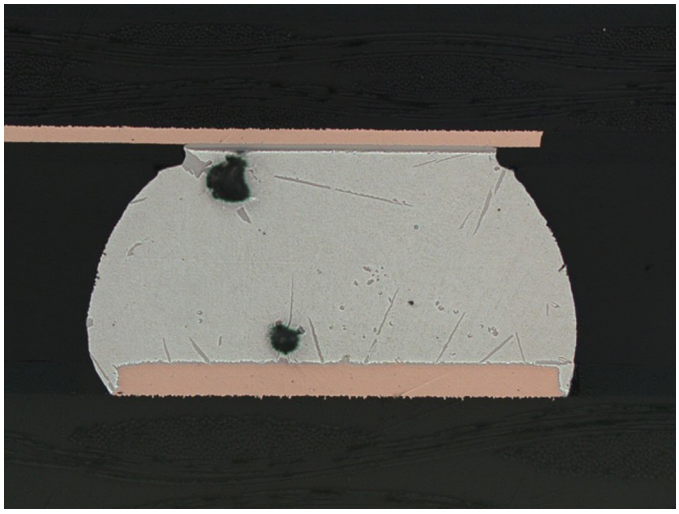

Figure 38. Pb-free solder: PBGA postflight, flight unit.

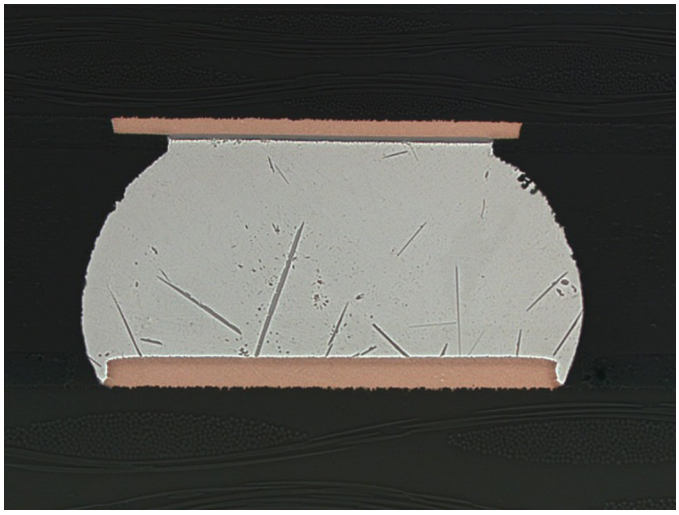

Figure 39. Pb-free solder: PBGA postflight, ground unit.

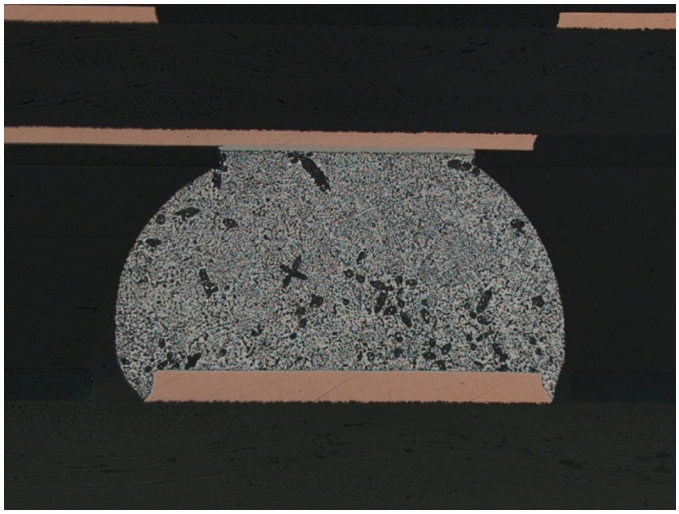

Figure 40. Sn/Pb solder: PBGA preflight.

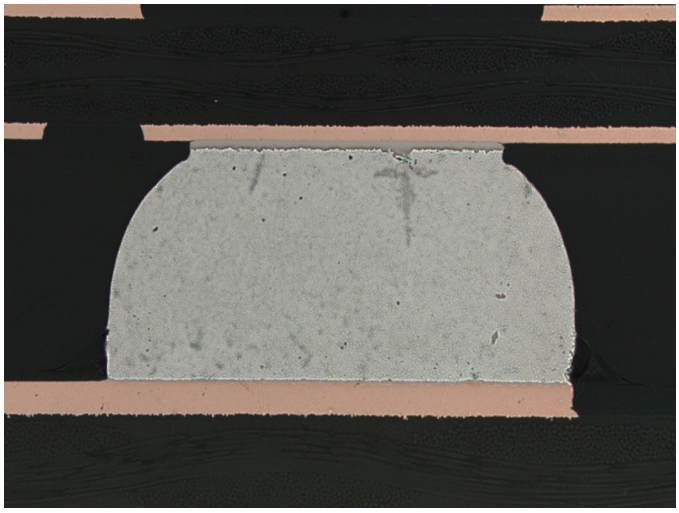

Figure 41. Sn/Pb solder: PBGA postflight, flight unit.

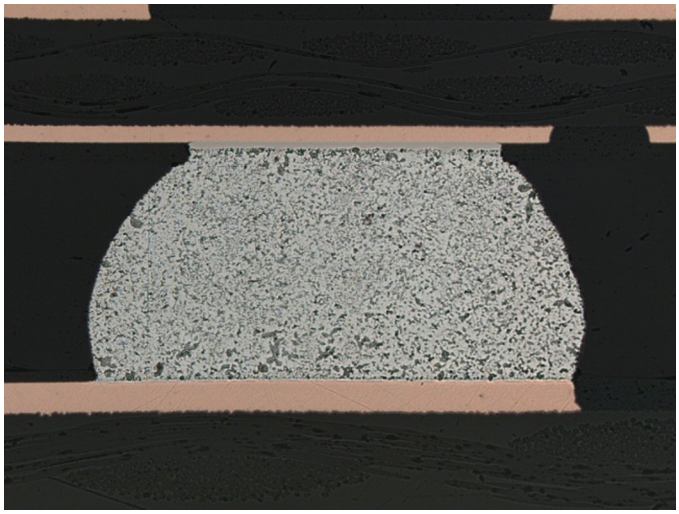

Figure 42. Sn/Pb solder: PBG postflight, ground unit.

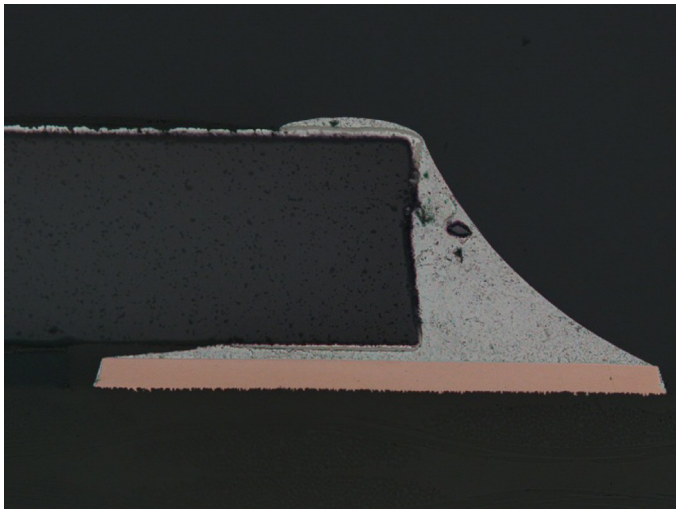

Figure 43. Mixed solder: Chip resistor preflight.

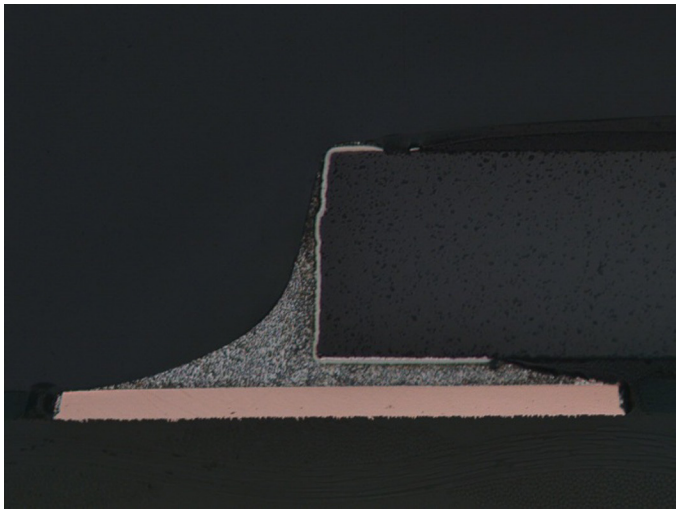

Figure 44. Mixed solder: Chip resistor postflight, flight unit.

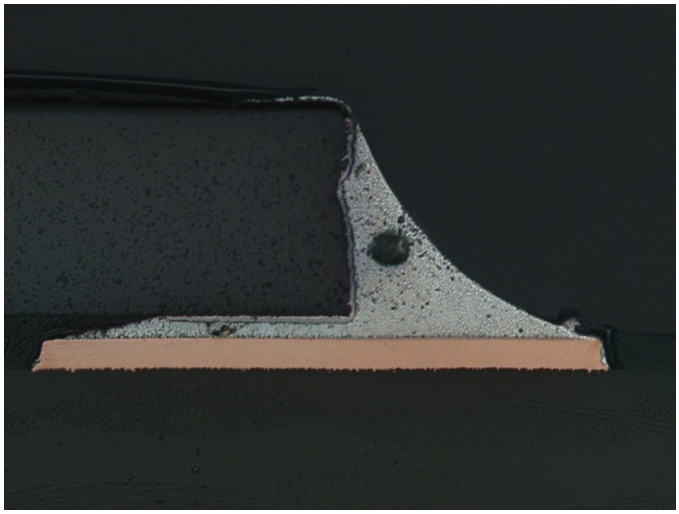

Figure 45. Mixed solder: Chip resistor postflight, ground unit.

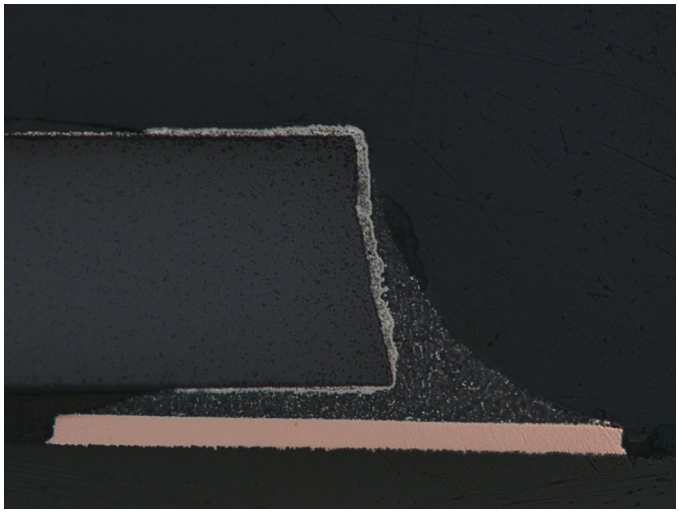

Figure 46. Pb-free solder: Chip resistor preflight.

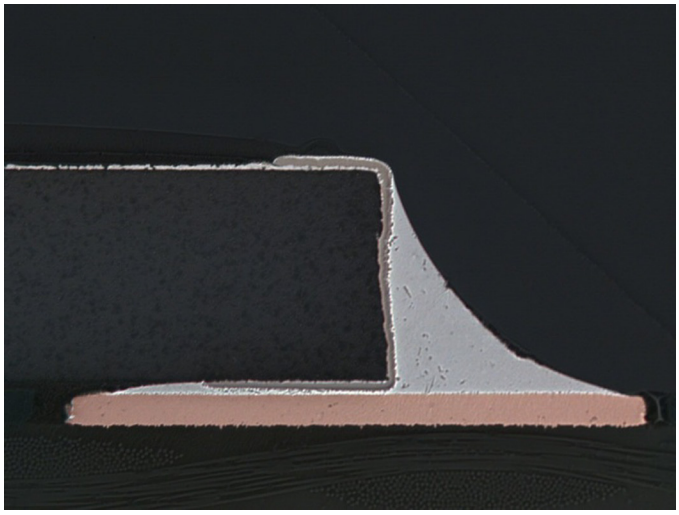

Figure 47. Pb-free solder: Chip resistor postflight, flight unit.

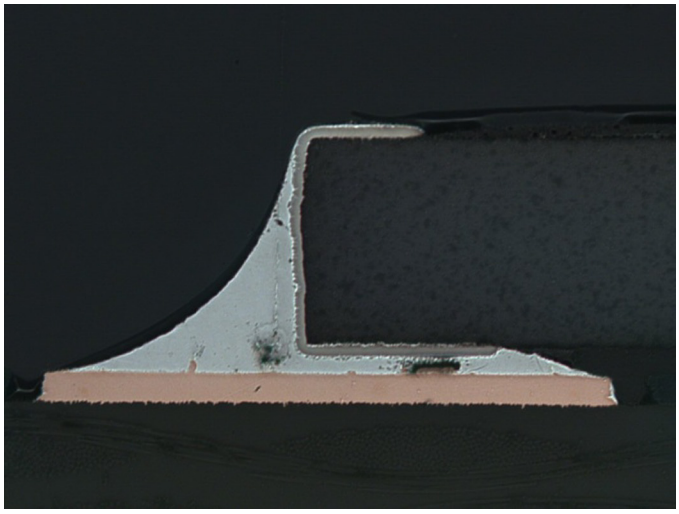

Figure 48. Pb-free solder: Chip resistor postflight, ground unit.

Figure 49. Sn/Pb solder: Chip resistor preflight.

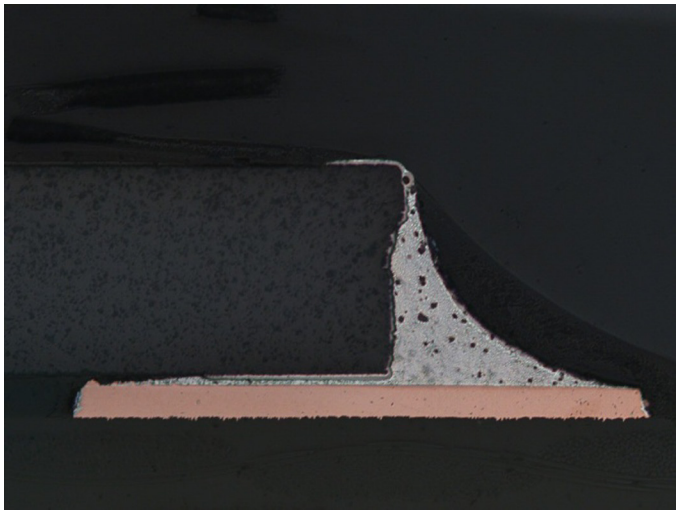

Figure 50. Sn/Pb solder: Chip resistor postflight, flight unit.

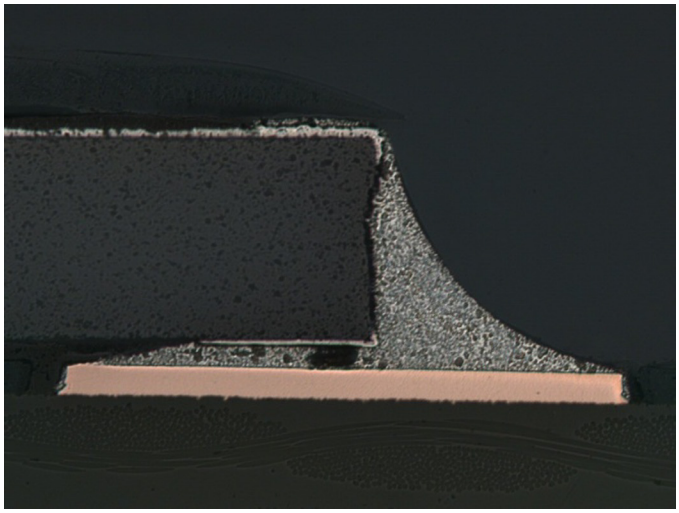

Figure 51. Sn/Pb solder: Chip resistor postflight, ground unit.

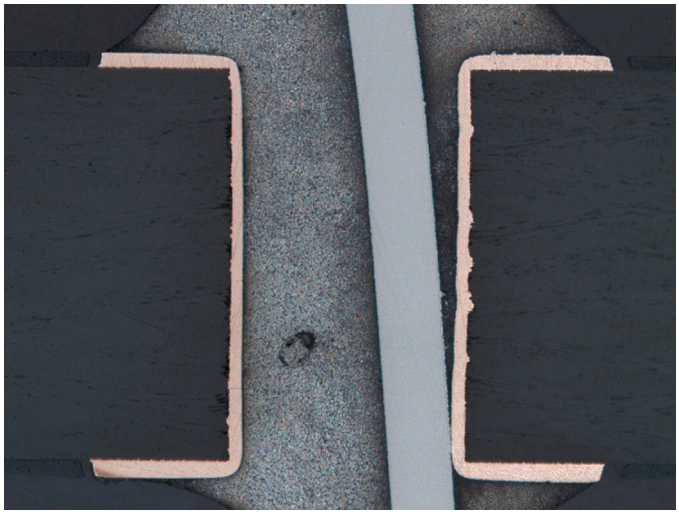

Figure 52. Mixed solder: DIP preflight.

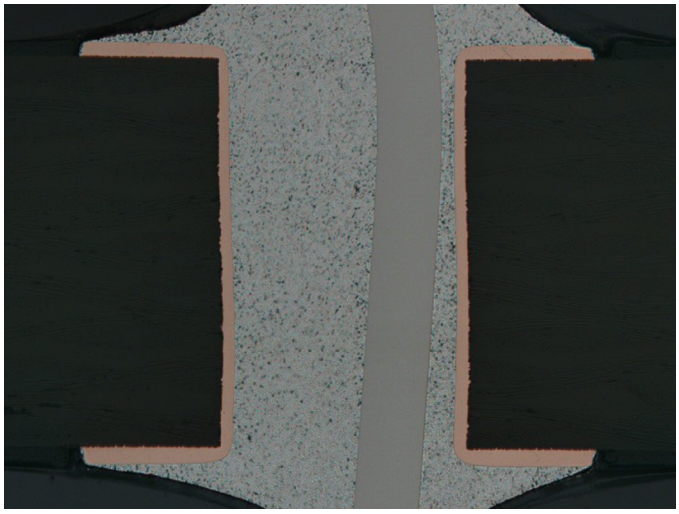

Figure 53. Mixed solder: DIP postflight, flight unit.

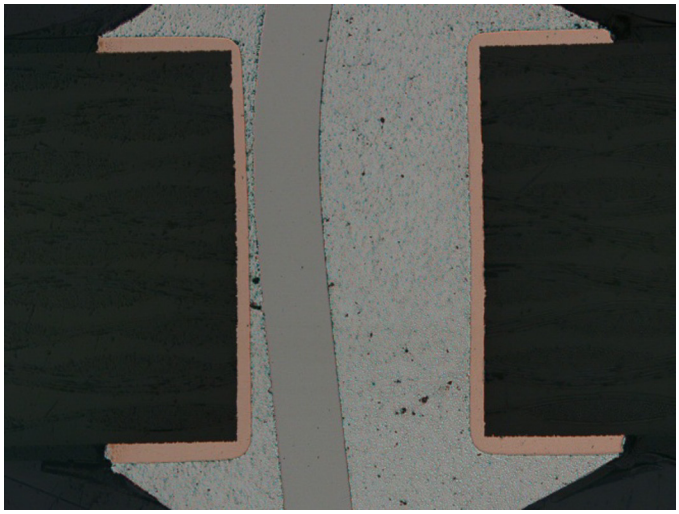

Figure 54. Mixed solder: DIP postflight, ground unit.

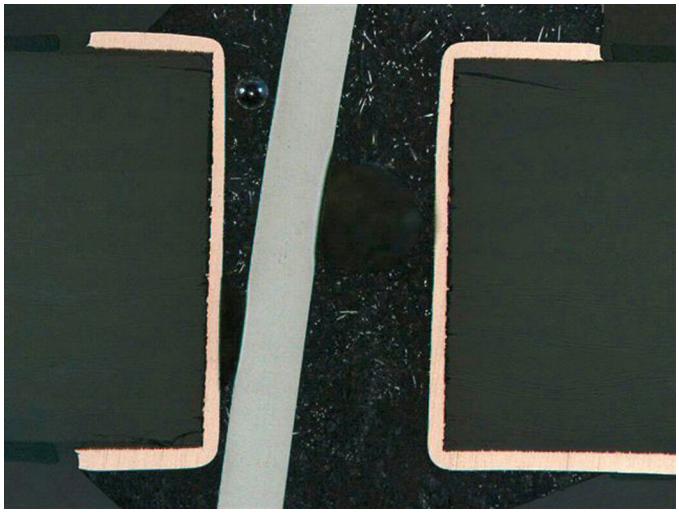

Figure 55. Pb-free solder: DIP preflight.

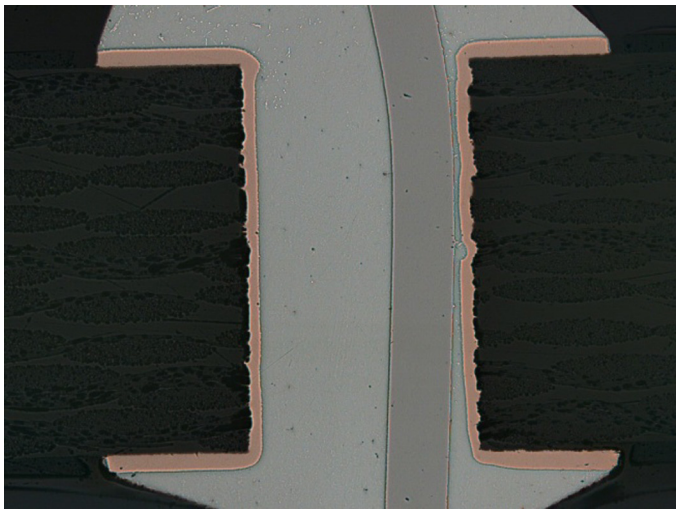

Figure 56. Pb-free solder: DIP postflight, flight unit.

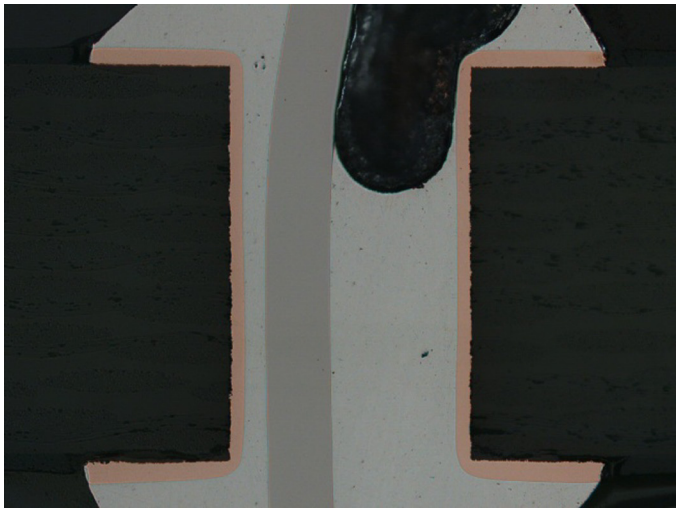

Figure 57. Pb-free solder: DIP postflight, ground unit.

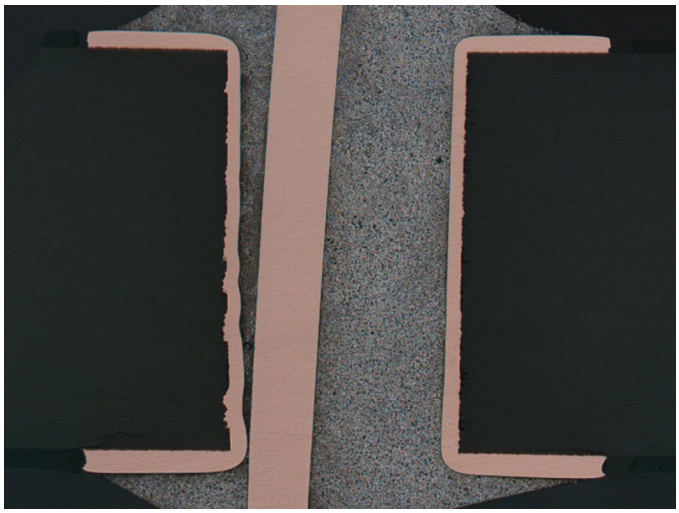

Figure 58. Sn/Pb solder: DIP preflight.

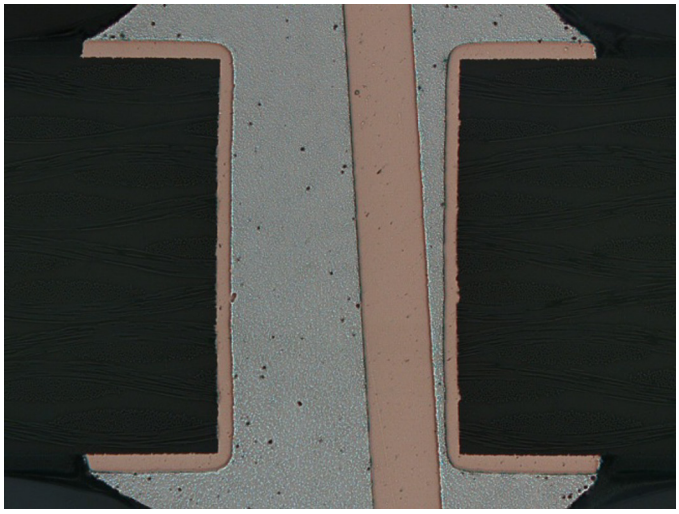

Figure 59. Sn/Pb solder: DIP postflight, flight unit.

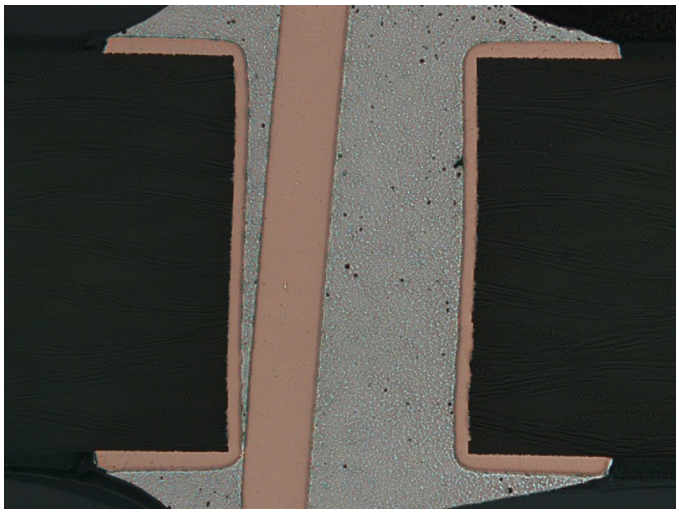

Figure 60. Sn/Pb solder: DIP postflight, ground unit.

5. OBSERVATIONS

The items being investigated were the following:

- IMC formation and growth under near 0 g and various temperatures.
- Solder joint life under temperature extremes.
- Aging effects under space environments.
- Effect of launch and reentry dynamics.
- Tin whisker growth under known conditions.
- The possible formation of Sn pest.

No significant IMC growth was observed either between the preflight and postflight microsections or between the postflight flight unit that was exposed to near 0-g conditions on the ISS and the ground unit that was in a 1-g environment in the laboratory.

Board delamination was observed in the microsection of the DIP lead on the Pb-free/Pb-free preflight board (see fig. 55). These leads were the only through-hole and hand-soldered joints on the boards. The joints were made by a competent NASA certified operator who had no prior experience with Pb-free solder and its higher associated melting temperature. No delamination was observed on the DIP microsections from the postflight ground or flight boards.

There were no solder joint failures or joint degradations. The temperature in space on the outside of the ISS was relatively benign and the experiment ranged from –26 to 45 °C, which is much less than the NASA normal ground testing thermal cycle range of –55 to 125 °C.

The joints did not exhibit damage from the launch and reentry dynamic loads.

No aging effects were observed on the flight or ground unit.

Tin pest is a low temperature phenomenon and can initiate at temperatures as high as 13 °C. Although Sn pest can initiate at temperatures as high as 13 °C, the flight unit board temperature remained below 0 °C for as long as 16 days at a time and no Sn pest was formed on the Pb-free or mixed solder boards.

Tin whiskers were found on the pure Sn portion of the dual in-line packages' leads on the flight unit mixed solder test board, but that is related to the part lead finish rather than to the solder joint composition. The whiskers were short, with the longest being 18 μm.

6. SUMMARY

No NASA program currently has plans to use Pb-free parts, boards, or solder in flight electronics. The primary concern is and has been inadvertent and unknown incorporation of Pb-free parts into flight systems or their use in COT systems that could be used in a flight program. Lead-free technology is assumed to be a problem and there have been some Sn whisker failures experienced, but there have been no controlled experiments to provide flight data to support these assumptions. The LTESE was a small (approximately 7- × 4.5- × 0.92-in) package containing a printed wiring data board and three printed wiring test boards, a Pb-free board with Pb-free parts attached using Pb-free solder, a SnPb board with Pb-free parts attached using SnPb solder, and an all SnPb control board. Each test board contained 1,464 solder joints under test. The LTESE was located in PEC-B of the MISSE-7. LTESE was launched on STS-129 on November 16, 2009. Spacewalker Randy Bresnik completed installation of the MISSE-7 experiment on ExPRESS Logistics Carrier 2 on November 22, 2009, and it was first powered up on the ISS on November 23, 2009. A ground unit operating in parallel for comparison was powered up on December 4, 2009, and ran until May 20, 2011. MISSE-7 was removed from the ISS on May 20, 2011, and returned to ground on STS-134 on June 1, 2011, for evaluation. There were no solder joint failures on either the flight or ground unit.

The experiment provided data that did not previously exist on flight safety resulting from inadvertent incorporation of Pb-free parts or their use in COTS. The Pb-free elements being investigated were IMC formation and growth under near 0 g and various temperatures, solder joint life under temperature extremes, aging effects under space environments, effect of launch and reentry dynamics, Sn-whisker growth under known conditions, and the possible formation of Sn pest.

7. CONCLUSION

Based upon the limited number of samples tested in this experiment, the following conclusion can be drawn. From a solder joint perspective, if Sn whisker mitigation is incorporated into the design, the risk from inadvertent incorporation of Pb-free parts into a Sn/Pb system or use of Pb-free COTS systems should be acceptable for low-Earth orbit space flight applications.

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14. ABSTRACT

This Technical Memorandum addresses the Lead-Free Technology Experiment in Space Environment that flew as part of the seventh Materials International Space Station Experiment outside the International Space Station for approximately 18 months. Its intent was to provide data on the performance of lead-free electronics in an actual space environment. Its postflight condition is compared to the preflight condition as well as to the condition of an identical package operating in parallel in the laboratory. Some tin whisker growth was seen on a flight board but the whiskers were few and short. There were no solder joint failures, no tin pest formation, and no significant intermetallic compound formation or growth on either the flight or ground units.

15. SUBJECT TERMS

lead-free solder, lead-free in space, lead-free electronics, space environment, MISSE-7 experiment, lead-free experiment, tin whiskers

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