Self-Nulling Lock-in Detection Electronics for Capacitance Probe Electrometer

NASA's Jet Propulsion Laboratory, Pasadena, California

A multi-channel electrometer voltmeter that employs self-nulling lock-in detection electronics in conjunction with a mechanical resonator with noncontact voltage sensing electrodes has been developed for space-based measurement of an Internal Electrostatic Discharge Monitor (IESDM). The IESDM is new sensor technology targeted for integration into a Space Environmental Monitor (SEM) subsystem used for the characterization and monitoring of deep dielectric charging on spacecraft.

Use of an AC-coupled lock-in amplifier with closed-loop sense-signal nulling via generation of an active guard-driving feedback voltage provides the resolution, accuracy, linearity and stability needed for long-term space-based measurement of the IESDM. This implementation relies on adjusting the feedback voltage to drive the sense current received from the resonator's variable-capacitance-probe voltage transducer to approximately zero, as limited by the signal-to-noise performance of the loop electronics. The magnitude of the sense current is proportional to the difference between the input voltage being measured and the feedback voltage, which matches the input voltage when the sense current is zero. High signal-to-noise-ratio (SNR) is achieved by synchronous detection of the sense signal using the correlated reference signal derived from the oscillator circuit that drives the mechanical resonator. The magnitude of the feedback voltage, while the loop is in a settled state with essentially zero sense current, is an accurate estimate of the input voltage being measured. This technique has many beneficial attributes including immunity to drift, high linearity, high SNR from synchronous detection of a single-frequency carrier selected to avoid potentially noisy 1/f low-frequency spectrum of the signal-chain electronics, and high accuracy provided through the benefits of a driven shield encasing the capacitance-probe transducer and guarded input triaxial lead-in.

Measurements obtained from a 2-channel prototype electrometer have demonstrated good accuracy ($|\text{error}| < 0.2$ V) and high stability. Twenty-four-hour tests have been performed with virtually no drift. Additionally, 5,500 repeated one-second measurements of 100 V input were shown to be approximately normally distributed with a standard deviation of 140 mV.

This work was done by Brent R. Blaes and Rembrandt T. Schaefer of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-47339

Discontinuous Mode Power Supply

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A document discusses the changes made to a standard push-pull inverter circuit to avoid saturation effects in the main inverter power supply. Typically, in a standard push-pull arrangement, the unsymmetrical primary excitation causes variations in the volt second integral of each half of the excitation cycle that could lead to the establishment of DC flux density in the magnetic core, which could eventually cause saturation of the main inverter transformer.

The relocation of the filter reactor normally placed across the output of the power supply solves this problem. The filter reactor was placed in series with the primary circuit of the main inverter transformer, and is presented as impedance against the sudden changes on the input current. The reactor averaged the input current in the primary circuit, avoiding saturation of the main inverter transformer. Since the implementation of the described change, the above problem has not reoccurred, and failures in the main power transistors have been avoided.

This work was done by John Lagadinos and Ethel Poulos of Pulse Systems, Inc. for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16281-1

Optimal Dynamic Sub-Threshold Technique for Extreme Low Power Consumption for VLSI

This technique approaches increased chip density with lower power consumption.

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For miniaturization of electronics systems, power consumption plays a key role in the realm of constraints. Considering the very large scale integration (VLSI) design aspect, as transistor feature size is decreased to 50 nm and below, there is sizable increase in the number of transistors as more functional building blocks are embedded in the same chip. However, the consequent increase in power consumption (dynamic and leakage) will serve as a key constraint to inhibit the advantages of transistor feature size reduction.

Power consumption can be reduced by minimizing the voltage supply (for dynamic power consumption) and/or increasing threshold voltage (V_{th}, for re-