Verilog-A Device Models for Cryogenic Temperature Operation of Bulk Silicon CMOS Devices

These models can be used in cryogenic electronics applications such as cooled imagers and sensors, medical electronics, and remote sensing satellites.

Goddard Space Flight Center, Greenbelt, Maryland

Verilog-A based cryogenic bulk CMOS (complementary metal oxide semiconductor) compact models are built for state-of-the-art silicon CMOS processes. These models accurately predict device operation at cryogenic temperatures down to 4 K. The models are compatible with commercial circuit simulators. The models extend the standard BSIM4 [Berkeley Short-channel IGFET (insulated-gate field-effect transistor) Model] type compact models by re-parameterizing existing equations, as well as adding new equations that capture the physics of device operation at cryogenic temperatures. These models will allow circuit designers to create optimized, reliable, and robust circuits operating at cryogenic temperatures.

Circuits that operate reliably at cryogenic temperatures are very difficult to design, because reliable semiconductor device and circuit models are not available for these temperatures. The unique aspect of this problem is the unknown physical characteristics of devices operating at cryogenic temperatures. Standard circuit models such as BSIM4 contain equations that can only predict device operation near room temperature. Therefore, new equations and re-parameterization of existing equations need to be done in order to functionalize the operation of state-of-the-art silicon CMOS devices at cryogenic temperatures.

These models will extend the room-temperature BSIM4 type compact models to temperatures as low as 4 K. The models are developed using the behavioral description language Verilog-A. Verilog-A allows for change in standard BSIM equations, re-parameterization of existing equations, and addition of new equations that capture the physics of semiconductor device operation at cryogenic temperatures.

Creation of these Verilog-A based cryogenic models requires the following:

a. Test chip with an array of devices fabricated in the process of interest or test data for the process;
b. Room and cryogenic temperature measurement of test chip;
c. First parameterization of BSIM4 model using room temperature data;
d. Verilog-A model parameterization using the developed equations and using the cryogenic temperature data;
e. Optimization of new model; and
f. Testing the new model by simulating test circuits and comparing them with measurements of circuits on the test chip.

Next, Verilog-A cryogenic CMOS device models are inserted into a simulator. Circuit simulations are run using the new models at temperatures as low as 4 K. These models work in conjunction with other standard compact models without causing any convergence or other errors in the circuit simulator.

The models can be further modified to include effects of radiation such as total ionizing dose at cold temperatures. These models will be able to predict long-term reliability of CMOS-based electronics operating under cryogenic temperatures in radiation-rich environments. The new models include the effect of threshold voltage variation at extreme cold temperatures and variation in mobility at cryogenic temperatures.

This work was done by Akin Akturk, Siddharth Potbhare, Neil Goldsman, and Michael Holloway of CoolCAD Electronics for Goddard Space Flight Center. Further information is contained in a TSP (see page 1).
GSC-16112-1

Rapid Process to Generate Beam Envelopes for Optical System Analysis

Two models take less time to complete beam envelope analysis.

Goddard Space Flight Center, Greenbelt, Maryland

The task of evaluating obstructions in the optical throughput of an optical system requires the use of two disciplines, and hence, two models: optical models for the details of optical propagation, and mechanical models for determining the actual structure that exists in the optical system. Previous analysis methods for creating beam envelopes (or cones of light) for use in this obstruction analysis were found to be cumbersome to calculate and take significant time and resources to complete. A new process was developed that takes less time to complete beam envelope analysis, is more accurate and less dependent upon manual node tracking to create the beam envelopes, and eases the burden on the mechanical CAD (computer-aided design) designers to form the beam solids.

This algorithm allows rapid generation of beam envelopes for optical system obstruction analysis. Ray trace information is taken from optical design software and used to generate CAD objects that represent the boundary of the beam envelopes for detailed analysis in mechanical CAD software.

Matlab is used to call ray trace data from the optical model for all fields and