Iridium Interfacial Stack — IrIS

A bondable metallization stack prevents diffusion of oxygen and gold into silicon carbide monolithically integrated circuits operating above 500 °C.

John H. Glenn Research Center, Cleveland, Ohio

Iridium Interfacial Stack (IrIS) is the sputter deposition of high-purity tantalum silicide ($TaSi_2$-400 nm) / platinum (Pt-200 nm) / iridium (Ir-200 nm) / platinum (Pt-200 nm) in an ultra-high vacuum system followed by a 600 °C anneal in nitrogen for 30 minutes. IrIS simultaneously acts as both a bond metal and a diffusion barrier. This bondable metallization that also acts as a diffusion barrier can prevent oxygen from air and gold from the wire-bond from infiltrating silicon carbide (SiC) monolithically integrated circuits (ICs) operating above 500 °C in air for over 1,000 hours. This $TaSi_2$/Pt/Ir/Pt metallization is easily bonded for electrical connection to off-chip circuitry and does not require extra anneals or masking steps.

There are two ways that IrIS can be used in SiC ICs for applications above 500 °C: it can be put directly on a SiC ohmic contact metal, such as Ti, or be used as a bond metal residing on top of an interconnect metal. For simplicity, only the use as a bond metal is discussed. The layer thickness ratio of $TaSi_2$ to the first Pt layer deposited thereon should be 2:1. This will allow Si from the $TaSi_2$ to react with the Pt to form Pt_2Si during the 600 °C anneal carried out after all layers have been deposited. The Ir layer does not readily form a silicide at 600 °C, and thereby prevents the Si from migrating into the top-most Pt layer during future anneals and high-temperature IC operation. The second (i.e., top-most) deposited Pt layer needs to be about 200 nm to enable easy wire bonding. The thickness of 200 nm for Ir was chosen for initial experiments; further optimization of the Ir layer thickness may be possible via further experimentation. Ir itself is not easily wire-bonded because of its hardness and much higher melting point than Pt. Below the iridium layer, the $TaSi_2$ and Pt react and form desired Pt_2Si during the post-deposition anneal while above the iridium layer remains pure Pt as desired to facilitate easy and strong wire-bonding to the SiC chip circuitry.

This work was done by David Spry of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18736-1 .

Downsampling Photodetector Array With Windowing

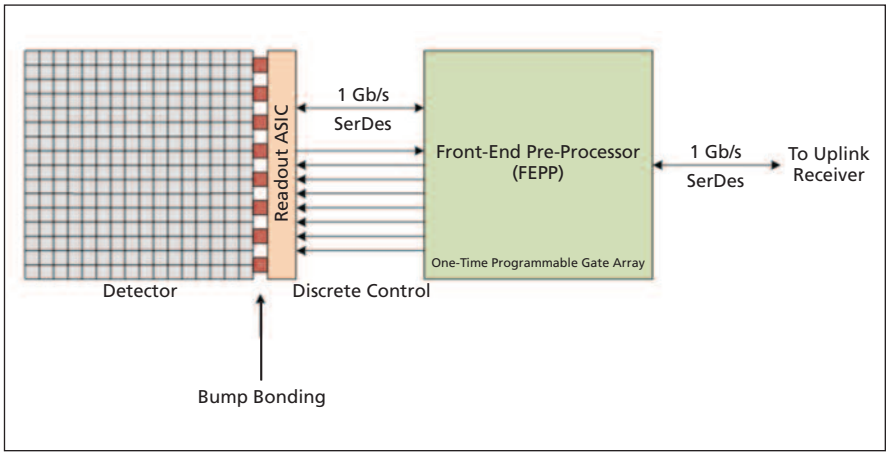
Applications include laser ranging for commercial surveys, and building-to-building optical data links.

NASA's Jet Propulsion Laboratory, Pasadena, California

In a photon counting detector array, each pixel in the array produces an electrical pulse when an incident photon on that pixel is detected. Detection and demodulation of an optical communication signal that modulated the intensity of the optical signal requires counting the number of photon arrivals over a given interval. As the size of photon counting photodetector arrays increases, parallel processing of all the pixels exceeds the resources available in current application-specific integrated circuit (ASIC) and gate array (GA) technology; the desire for a high fill factor in avalanche photodiode (APD) detector arrays also precludes this.

Through the use of downsampling and windowing portions of the detector array, the processing is distributed between the ASIC and GA. This allows demodulation of the optical communication signal incident on a large photon counting detector array, as well as providing architecture amenable to algorithmic changes.

The detector array readout ASIC functions as a parallel-to-serial converter, serializing the photodetector array output for subsequent processing. Additional downsampling functionality for each pixel is added to this ASIC. Due to the large number of pixels in the array, the readout time of the entire photodetector is greater than the time between photon arrivals; therefore, a downsampling pre-processing step is done in order to increase the time allowed for the readout to occur. Each pixel drives a small counter that is incremented at every detected photon arrival or, equivalently, the charge in a storage capacitor is incremented. At the end of a user-configurable counting period (calculated independently from the ASIC),



Processing can be distributed across an ASIC and GA through downsampling and windowing portions of the **Detector Array**.

the counters are sampled and cleared. This downsampled photon count information is then sent one counter word at a time to the GA.

For a large array, processing even the downsampled pixel counts exceeds the capabilities of the GA. Windowing of the array, whereby several subsets of pixels are designated for processing, is used to further reduce the computational requirements. The grouping of the designated pixel frame as the photon count information is sent one word at a time to the GA, the aggregation of the pixels in a window can be achieved by selecting only the designated pixel counts from the serial stream of photon counts, thereby obviating the need to store the entire frame of pixel count in the gate array. The pixel count sequence from each window can then be processed, forming lower-rate pixel statistics for each window. By having this processing occur in the GA rather than in the ASIC, future changes to the processing algorithm can be readily implemented.

The high-bandwidth requirements of a photon counting array combined with the properties of the optical modulation being detected by the array present a unique problem that has not been addressed by current CCD or CMOS sensor array solutions.

This work was done by Ferze D. Patawaran, William H. Farr, Danh H. Nguyen, Kevin J. Quirk, and Adit Sahasrabudhe of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-48346

Optical Phase Recovery and Locking in a PPM Laser Communication Link

Coherence augmentation in a pulsed optical communication link will enable enhanced Doppler tracking and ranging capabilities.

NASA's Jet Propulsion Laboratory, Pasadena, California

Free-space optical communication holds great promise for future space missions requiring high data rates. For data communication in deep space, the current architecture employs pulse position modulation (PPM). In this scheme, the light is transmitted and detected as pulses within an array of time slots. While the PPM method is efficient for data transmission, the phase of the laser light is not utilized.

The phase coherence of a PPM optical signal has been investigated with the goal of developing a new laser communication and ranging scheme that utilizes optical coherence within the established PPM architecture and photon-counting detection (PCD). Experimental measurements of a PPM modulated optical signal were conducted, and modeling code was developed to generate random PPM signals and simulate spectra via FFT (Fast Fourier Transform) analysis. The experimental results show very good agreement with the simulations and confirm that coherence is preserved despite modulation with high extinction ratios and very low duty cycles.

A real-time technique has been developed to recover the phase information through the mixing of a PPM signal with a frequency-shifted local oscillator (LO). This mixed signal is amplified, filtered, and integrated to generate a voltage proportional to the phase of the modulated signal. By choosing an appropriate time constant for integration, one can maintain a phase lock despite long "dark" times between consecutive pulses with low duty cycle. A proof-of-principle demonstration was first achieved with an RF-based PPM signal and test setup. With the same principle method, an optical carrier within a PPM modulated laser beam could also be tracked and recovered. A reference laser was phase-locked to an independent pulsed laser signal with low-duty-cycle pseudo-random PPM codes. In this way, the drifting carrier frequency in the primary laser source is tracked via its phase change in the mixed beat note, while the corresponding voltage feedback maintains the phase lock between the two laser sources.

The novelty and key significance of this work is that the carrier phase information can be harnessed within an optical communication link based on PPM-PCD architecture. This technology development could lead to quantum-limited efficient performance within the communication link itself, as well as enable high-resolution optical tracking capabilities for planetary science and spacecraft navigation.

This work was done by David C. Aveline, Nan Yu, and William H. Farr of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-47994

High-Speed Edge-Detecting Line Scan Smart Camera

This circuit reduces size and system complexity while increasing processing frame rates.

John H. Glenn Research Center, Cleveland, Ohio

A high-speed edge-detecting line scan smart camera was developed. The camera is designed to operate as a component in a NASA Glenn Research Center developed inlet shock detection system. The inlet shock is detected by projecting a laser sheet through the airflow. The shock within the airflow is the densest part and refracts the laser sheet the most in its vicinity, leaving a dark spot or shadowgraph. These spots show up as a dip or negative peak within the pixel intensity profile of an image of the projected laser sheet. The smart camera acquires and processes in real-time the linear image containing the shock shadowgraph and outputting the shock location. Previously a high-speed camera