signature identification in a heterogeneous environment.

In this architecture, there are four basic blocks: input, output, processing, and storage. The input block consists of sensing devices including IR, lidar, radar, visual, chemical, and biosensors, at their various sampling data rates. Based on application scenario, selected sensory streams are sent by the input block to the subsequent "processing" block in a fully parallel fashion. Feature data is extracted from the analog/digital sensory streams and is accumulated in the storage block for enriching the "knowledge base" as a situation unfolds. The incoming raw data is not stored as is the usual approach in current computer architecture, and is reconstructed if required during the process in real time. The output block sends the output signal to various interfaces (actuating interfaces), such as other machines, humans, or RF devices. The processing block consists of several mathematical constructs including Principal Component Analysis (PCA), Independent Component Analysis (ICA), Neural Network (NN), Genetic Algorithm (GA), etc., and is controlled by a hierarchy of logical rules to enact reasoning, reconfiguring, and adapting as required when the target is changing in the dynamic environment. Therefore, the processing block can select an architecture for each particular application as needed, dynamically, and still remain compatible with a digital environment. The conceptualized architecture, capable of extracting knowledge from information and using the knowledge for reasoning, adapting, and reacting therefore qualifies as a cognitive architecture for real-time data fusion in a dynamic environment. Furthermore, its dynamic autonomous reconfigurability makes it versatile as a "general-purpose" intelligent system to accomplish the "searching for a source of food while avoiding the predator" function.

This work was done by Tuan A. Duong and Vu A. Duong of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Refer to NPO-46633, volume and number of this NASA Tech Briefs *issue, and the page number.*

Programmable Digital Controller

Goddard Space Flight Center, Greenbelt, Maryland

An existing three-channel analog servo loop controller has been redesigned for piezoelectric-transducer-based (PZT-based) etalon control applications to a digital servo loop controller. This change offers several improvements over the previous analog controller, including software control over proportional–integral–derivative (PID) parameters, inclusion of other data of interest such as temperature and pressure in the control laws, improved ability to compensate for PZT hysteresis and mechanical mount fluctuations, ability to provide pre-programmed scanning and stepping routines, improved user interface, expanded data acquisition, and reduced size, weight, and power.

The original analog servo controller only had the ability to correct for a single error term generated by the capacitive gap sensor. This was less than optimal when trying to return to the same gap position due to the hysteresis of the PZT motors and thermal drift in the electronics.

To overcome the limitations of the analog servo loop, it was decided that a control loop could be built around a microcontroller/central processing unit (CPU), i.e., a digital servo loop. The CPU would query various sensors such as a capacitive gap sensor or temperature sensor, among others, then based on reprogrammable control laws, provide a driving signal to a high-voltage driver that actuates the PZT motor on the etalon. The system is based on mostly COTS (commercial off-the-shelf) hardware and software.

The design is based around a new generation of direct capacitance to digital converters from Analog Devices, the AD7745. This integrated circuit (IC) allows the measurement of the capacitance of the gap capacitor at up to 90 Hz with resolutions down to 4 aF. This measurement is an absolute value whereas the previous analog design measured capacitance relative to a reference capacitor whose value had some uncertainty. The new design allows one to measure the gap directly, after calibration, thereby greatly improving overall control.

This work was done by Gregory J. Wassick of Michigan Aerospace Corporation for Goddard Space Flight Center. For further information, contact the Goddard Innovative Partnerships Office at (301) 286-5810. GSC-15524-1

Use of CCSDS Packets Over SpaceWire to Control Hardware

Goddard Space Flight Center, Greenbelt, Maryland

For the Lunar Reconnaissance Orbiter, the Command and Data Handling subsystem consisted of several electronic hardware assemblies that were connected with SpaceWire serial links. Electronic hardware would be commanded/controlled and telemetry data was obtained using the SpaceWire links. Prior art focused on parallel data buses and other types of serial buses, which were not compatible with the SpaceWire and the core flight executive (CFE) software bus.

This innovation applies to anything that utilizes both SpaceWire networks and the CFE software. The CCSDS (Consultative Committee for Space Data Systems) packet contains predetermined values in its payload fields that electronic hardware attached at the terminus of the SpaceWire node would decode, interpret, and execute. The hardware's interpretation of the packet data would enable the hardware to change its state/configuration (command) or generate status (telemetry).