

of a key distinguishing factor. EEMD adds noise to the signal under study whereas EDA mixes the signal with calibrated noise. It is mixing with calibrated noise that permits the measurement of temporal-functional variability of uncertainty in the underlying process.

The RGMC permits the evaluation of EDA by modulating the receiver gain using an external signal. Without the RGMC, samples of calibrated references from radiometers form an ensemble

data set of the natural occurring fluctuations within a receiver. By driving the gain of an otherwise stable receiver with an external signal, the conceptual framework and generalization of the mathematics of EDA can be tested. A series of measurements was conducted to evaluate and characterize the performance of the RGMC. Test signals stepped the RGMC across its dynamic range of performance using a radiometer that sampled four noise references; analysis

indicates that the RGMC successfully modulated the receiver gain with an external signal. Calibration algorithms applied to four noise references demonstrate the RGMC produced ensemble data sets of the external signal.

This work was done by Hollis Jones and Paul Racette of Goddard Space Flight Center and David Walker and Dazhen Gu of the National Institute of Standards and Technology. Further information is contained in a TSP (see page 1). GSC-16188-1

NEXUS Scalable and Distributed Next-Generation Avionics Bus for Space Missions

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A paper discusses NEXUS, a common, next-generation avionics interconnect that is transparently compatible with wired, fiber-optic, and RF physical layers; provides a flexible, scalable, packet switched topology; is fault-tolerant with sub-microsecond detection/recovery latency; has scalable bandwidth from 1 Kbps to 10 Gbps; has guaranteed real-time determinism with sub-microsecond latency/jitter; has built-in testability; features low power consumption (< 100 mW per Gbps); is lightweight with about a 5,000-logic-gate

footprint; and is implemented in a small Bus Interface Unit (BIU) with reconfigurable back-end providing interface to legacy subsystems.

NEXUS enhances a commercial interconnect standard, Serial RapidIO, to meet avionics interconnect requirements without breaking the standard. This unified interconnect technology can be used to meet performance, power, size, and reliability requirements of all ranges of equipment, sensors, and actuators at chip-to-chip, board-to-board, or box-to-box boundary.

Early results from in-house modeling activity of Serial RapidIO using VisualSim indicate that the use of a switched, high-performance avionics network will provide a quantum leap in spacecraft onboard science and autonomy capability for science and exploration missions.

This work was done by Yutao He, Eddy Shalom, Savio N. Chau, Raphael R. Some, and Gary S. Bolotin of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-47653

Digital Interface Board to Control Phase and Amplitude of Four Channels

A small set of short, high-level commands provides a simple programming interface for an external controller.

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An increasing number of parts are designed with digital control interfaces, including phase shifters and variable attenuators. When designing an antenna array in which each antenna has independent amplitude and phase control, the number of digital control lines that must be set simultaneously can grow very large. Use of a parallel interface would require separate line drivers, more parts, and thus additional failure points. A convenient form of control where single-phase shifters or attenuators could be set or the whole set could be programmed with an update rate of 100 Hz is needed to solve this problem.

A digital interface board with a field-

programmable gate array (FPGA) can simultaneously control an essentially arbitrary number of digital control lines with a serial command interface requiring only three wires. A small set of short, high-level commands provides a simple programming interface for an external controller. Parity bits are used to validate the control commands. Output timing is controlled within the FPGA to allow for rapid update rates of the phase shifters and attenuators.

This technology has been used to set and monitor eight 5-bit control signals via a serial UART (universal asynchronous receiver/transmitter) interface. The digital interface board controls

the phase and amplitude of the signals for each element in the array. A host computer running Agilent VEE sends commands via serial UART connection to a Xilinx VirtexII FPGA. The commands are decoded, and either outputs are set or telemetry data is sent back to the host computer describing the status and the current phase and amplitude settings.

This technology is an integral part of a closed-loop system in which the angle of arrival of an X-band uplink signal is detected and the appropriate phase shifts are applied to the Ka-band downlink signal to electronically steer the array back in the direction of the