https://ntrs.nasa.gov/search.jsp?R=20120000818 2019-08-30T18:44:51+00:00Z

A two-way asymmetric magic-T based power combiner for MMIC power amplifiers, which can take in unequal inputs, has been successfully designed, fabricated, and characterized over NASA's Deep Space Network (DSN) frequency range of 31.8 to 32.3 GHz. The figure is a transparent view of the asymmetric combiner that shows the 4-port configuration and the internal structure. The rod, post, and iris are positioned by design to achieve the desired asymmetric power ratio, phase equality, and port isolation. Although the combiner was designed for an input power ratio of 2:1, it can be custom-designed for any arbitrary power ratio and frequency range. The manufactured prototype combiner was precision machined from aluminum and is less than 2 in.^{3} (32.8 cm^3). Previously investigated rectangular waveguide unequal power combiners were based on shunt/series coupling slots, E-plane septums, or H-plane T-junctions. All the prior art unequal power combiners operated at or below X-band (10 GHz) frequencies and were primarily used in the feed network of antenna arrays. The only reported asymmetric magic-T was developed as a 2:1 power divider for operation at a much lower frequency, around 500 MHz.

The measured power ratio when tested as a power divider was very close to 2 and the phase balance was within 2.6°, resulting in near ideal performance. When tested as a combiner using two MMIC SSPAs with a 2:1 power output ratio, an efficiency greater than 90 percent was demonstrated over the 500 MHz DSN frequency range. The return loss at the combiner output port (1) was greater than 18 dB and the input port (2 and 3) isolation was greater than 22 dB. The results show the asymmetric combiner to be a good candidate for high-efficiency power combining of two or more SSPAs needed to achieve the 6 to 10 W required by space communications systems of future NASA missions.

This work was done by E.G. Wintucky, R.N. Simons, and J.C. Freeman of Glenn Research Center and C.T. Chevalier of QinetiQ North America Corp. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18590-1.

10–100 Gbps Offload NIC for WAN, NLR, and Grid Computing

Goddard Space Flight Center, Greenbelt, Maryland

An extremely fast offload engine system has been developed that operates at 60 Gigabits per second (Gbps), and has scalability to 100 Gbps full-duplex (f-d). This system is based on unique coding and architecture derived from splintered UDP (User Datagram Protocol) offload technology, resulting in unique FPGA (field programmable gate array) intellectual property core and firmware.

This innovation improves the networking speed of supercomputer clusters by providing an ultra-fast network protocol processing offload from a CPU (central processing unit) by inserting an offload engine into a host backplane and network connections. This runs on protocol firmware.

This work was done by Patricia Crowley of Gonzaga University, James Awrach of SeaFire, and Arthur Maccabe of the University of New Mexico for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15447-1

Pulsed Laser System to Simulate Effects of Cosmic Rays in Semiconductor Devices

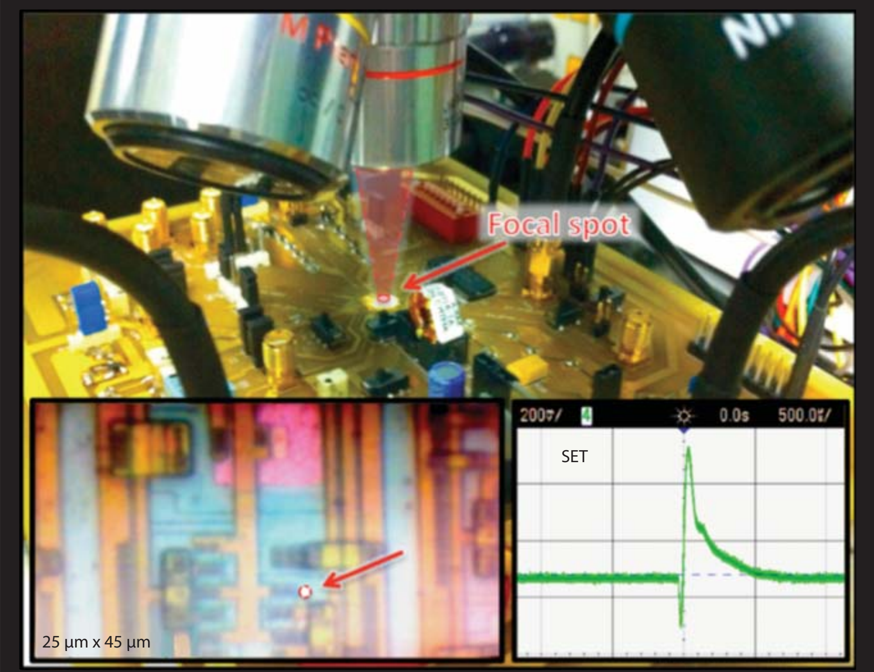
The system can measure the radiation sensitivity of microelectronic devices with high spatial and temporal resolution.

NASA's Jet Propulsion Laboratory, Pasadena, California

Spaceflight system electronic devices must survive a wide range of radiation environments with various particle types including energetic protons, electrons, gamma rays, x-rays, and heavy ions. High-energy charged particles such as heavy ions can pass straight through a semiconductor material and interact with a charge-sensitive region, generating a significant amount of charge (electron-hole pairs) along their tracks. These excess charges can damage the device, and the response can range from temporary perturbations to permanent changes in the state or performance. These phenomena are called single event effects (SEE).

Before application in flight systems, electronic parts need to be qualified and tested for performance and radiation sensitivity. Typically, their susceptibility to SEE is tested by exposure to an ion beam from a particle accelerator. At such facilities, the device under test (DUT) is irradiated with large beams so there is no fine resolution to investigate particular regions of sensitivity on the parts. While it is the most reliable approach for radiation qualification, these evaluations are time consuming and costly. There is always a need for new cost-efficient strategies to complement accelerator testing: pulsed lasers provide such a solution.

Pulsed laser light can be utilized to simulate heavy ion effects with the advantage of being able to localize the sensitive region of an integrated circuit. Generally, a focused laser beam of approximately picosecond pulse duration is used to generate carrier density in the semiconductor device. During irradiation, the laser pulse is absorbed by the electronic medium with a wavelength selected accordingly by the user, and the laser energy can ionize and simulate SEE as would occur in



This figure illustrates the ps-pulsed **Laser Beam Path** focused to a micron spot onto a semiconductor device. The lower left inset shows the magnified image through the microscope indicating the laser's focal spot. In the lower right inset, a single event transient (SET) was captured by the digital scope due to a single pulse of 20 nJ. The peak amplitude is ≈400 mV with ≈200-µs decay.

space. With a tightly focused near infrared (NIR) laser beam, the beam waist of about a micrometer can be achieved, and additional scanning techniques are able to yield submicron resolution. This feature allows mapping of all of the sensitive regions of the studied device with fine resolution, unlike heavy ion experiments. The problematic regions can be precisely identified, and it provides a considerable amount of information about the circuit. In addition, the system allows flexibility for testing the device in different configurations *in situ*.

JPL has built and tested a pulsed laser facility with a mode-locked Ti:sapphire cavity pumped by a 5-W diode-pumped solid-state laser at 532 nm. A laser beam with a pulse width of about 2 picoseconds is tightly focused through a microscope objective onto the DUT. The Ti:sapphire has a wavelength range of 720–850 nm, with average power ranging from about 500 mW to as high as 1 W at 780 nm. The cavity outputs an 80-MHz repetition rate of pulses, which are precisely selected by an acoustic-optical modulator (AOM). The beam power can be attenuated to deliver calibrated energy to the DUT, typically chosen in the range of 1 to 500 pJ. When focused to a micron-scale waist, the electromagnetic radiation intensity ionizes the silicon medium to a penetration depth determined by the wavelength, and induces SEE within the device medium, simulating a heavy ion penetrating into the part.

The laser system utilizes the tunable pulsed source along with a HeNe laser continuous wave source at 635 nm for alignment guidance. It also incorporates a motorized two-axis stage to move the DUT and scan the area with resolution down to 100 nm. With automated computer control of the pulses, stage, and digital oscilloscope, the system can record the voltage transient responses as it steps through a pre-set scanning area, thereby generating a functional map of the device sensitivity with extremely fine resolution.

While it cannot fully replace heavy ion testing, this pulsed laser technology is a necessary complementary tool that helps the radiation hardness assurance flow when qualifying electronics for space applications. It also offers high-resolution imaging of the device sensitivity to localize problematic areas of the integrated circuits under test. This spatial and temporal information allows parts to be analyzed and issues to be diagnosed for research and development, leading to more robust and better-performing electronics for space applications.

This work was done by David C. Aveline, Philippe C. Adell, Gregory R. Allen, Steven M. Guertin, and Steven S. McClure of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-47254