Electronics/Computers

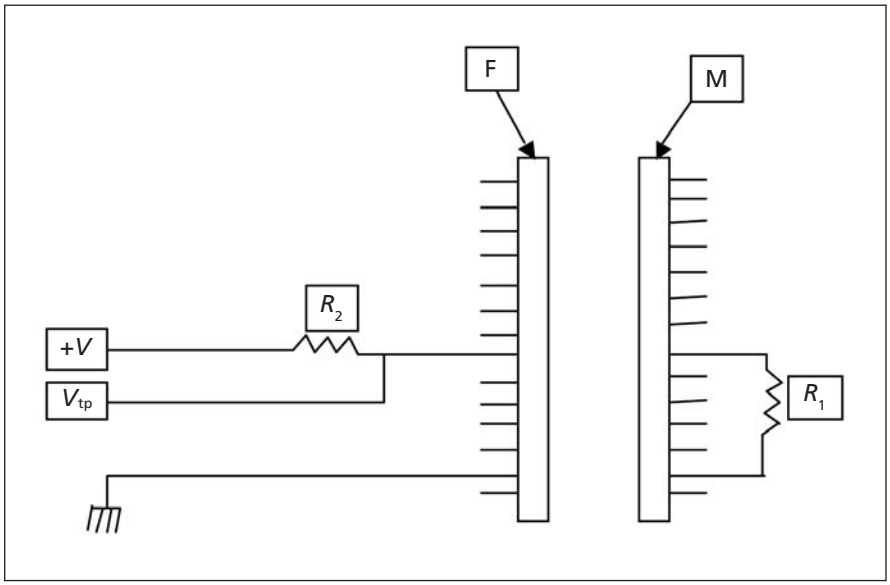
Positively Verifying Mating of Previously Unverifiable Flight Connectors

New approach ensures secure connections.

Goddard Space Flight Center, Greenbelt, Maryland

Current practice is to uniquely key the connectors, which, when mated, could not be verified by ground tests such as those used in explosive or non-explosive initiators and pyro valves. However, this practice does not assure 100-percent correct mating. This problem could be overcome by the following approach.

Errors in mating of interchangeable connectors can result in degraded or failed space mission. Mating of all flight connectors considered not verifiable via ground tests can be verified electrically by the following approach. It requires two additional wires going through the connector of interest, a few resistors, and a voltage source (see figure). The test-point voltage V_{tp} when the connector is not mated will be the same as the input voltage, which gets attenuated by the resistor R_1 when the female (F) and male (M) connectors are mated correctly and properly. The voltage at the test point will be a function of R_1 and R_2. Monitoring of the test point could be done on ground support equipment (GSE) only, or it can be a telemetry point. For implementation on multiple connector pairs, a different value for R_1 or R_2 or both can be selected for each pair of connectors that would result in a unique test point voltage for each connector pair. Each test point voltage is unique, and correct test point voltage is read only when the correct pair is mated correctly together. Thus, this design approach can be used to verify positively the correct mating of the connector pairs. This design approach can be applied to any number of connectors on the flight vehicle.



The basic **Circuit Diagram** for verifying secure connection.

This work was done by R.K. Chetty Pandipati and Marlon Enciso of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15896-1

Radiation-Tolerant Intelligent Memory Stack — RTIMS

RTIMS can be used in real-time data processing, reconfigurable computing, and memory-intensive applications.

Langley Research Center, Hampton, Virginia

This innovation provides reconfigurable circuitry and 2-Gb of error-corrected or 1-Gb of triple-redundant digital memory in a small package. RTIMS uses circuit stacking of heterogeneous components and radiation shielding technologies. A reprogrammable field-programmable gate array (FPGA), six synchronous dynamic random access memories, linear regulator, and the radiation mitigation circuits are stacked into a module of 42.7×42.7×13 mm. Triple module redundancy, current limiting, configuration scrubbing, and single-event function interrupt detection are employed to mitigate radiation effects. The novel self-scrubbing and single event functional interrupt (SEFI) detection allows a relatively "soft" FPGA to become radiation tolerant without external scrubbing and monitoring hardware.

RTIMS enables significant reductions in the size and mass of mission memory arrays, and is a radiation-tolerant memory suitable for both GEO and LEO space missions through the use of new package-level radiation shielding technology and triple modular redundancy (TMR) FPGA techniques. RTIMS also provides a simplified interface to a large SDRAM (synchronous dynamic random access memory) array with