Pressure-Sensor Assembly Technique

An essential underfilling step can be performed without compromising a diaphragm.

John H. Glenn Research Center, Cleveland, Ohio

Nielsen Engineering & Research (NEAR) recently developed an ultrathin data acquisition system for use in turbomachinery testing at NASA Glenn Research Center. This system integrates a microelectromechanical-systems- (MEMS-) based absolute pressure sensor [0 to 50 psia (0 to 345 kPa)], temperature sensor, signal-conditioning application-specific integrated circuit (ASIC), microprocessor, and digital memory into a package which is roughly 2.8 in. (7.1 cm) long by 0.75 in. (1.9 cm) wide. Each of these components is flip-chip attached to a thin, flexible circuit board and subsequently ground and polished to achieve a total system thickness of 0.006 in. (0.15 mm). Because this instrument is so thin, it can be quickly adhered to any surface of interest where data can be collected without disrupting the flow being investigated.

One issue in the development of the ultrathin data acquisition system was how to attach the MEMS pressure sensor to the circuit board in a manner which allowed the sensor's diaphragm to communicate with the ambient fluid while providing enough support for the chip to survive the grinding and polishing operations. The technique, developed by NEAR and Jabil Technology Services Group (San Jose, CA), is described below. In the approach developed, the sensor is attached to the specially designed circuit board, see Figure 1, using a modified flip-chip technique. The circular diaphragm on the left side of the sensor is used to actively measure the ambient pressure, while the diaphragm on the right is used to compensate for changes in output due to temperature variations. The circuit board is fabricated with an access hole through it so that when the completed system is installed onto a wind tunnel model (chip side down), the active diaphragm is exposed to the environment. After the sensor is flip-chip attached to the circuit board, the die is underfilled to support the chip during the subsequent grinding and polishing operations. To prevent this underfill material from getting onto the sensor's diaphragms, the circuit board is fabricated with two 25-micrometer-tall polymer rings, sized so that the diaphragms fit inside the rings once the chip is attached.

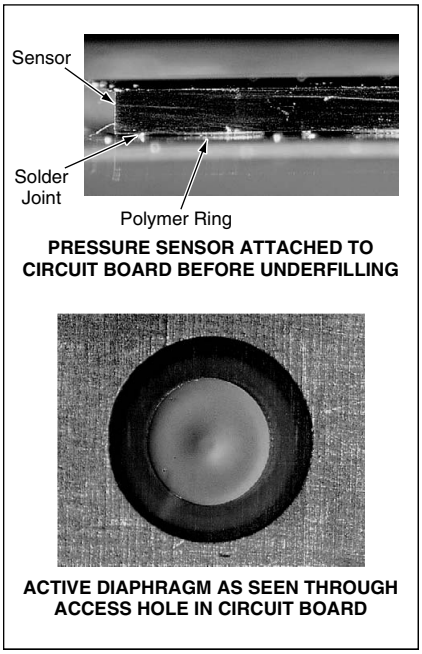

Figure 2. **Critical Components** of the instrument are shown here at two different stages in the assembly process.

During the reflow operation, the solder bumps on the chip melt and spread out over the circuit board's bond pads thus pulling the chip down until its face rests on the top of the two polymer rings. A series of experiments were conducted to determine the optimal size for the solder bumps so that the sensor chip seated properly on the rings while adequate solder joints were formed between the chip and the circuit board. A side view showing the chip and circuit board after soldering, but before underfilling, is provided in the upper part of Figure 2.

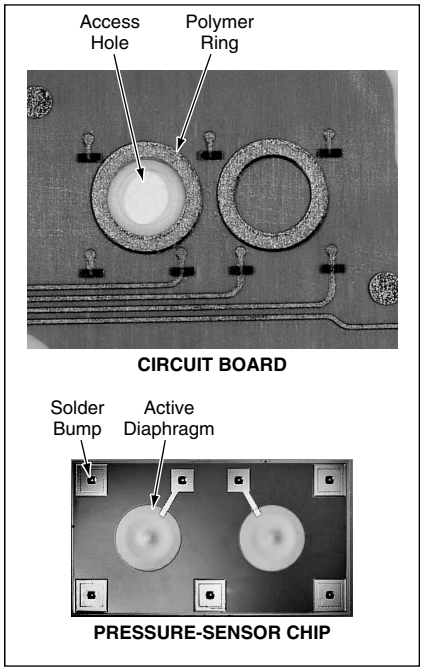

Figure 1. The **Pressure-Sensor Chip and Circuit Board** are shown here as they appear before they are put together by use of a modified flip-chip technique.

With the sensor resting on the polymer rings, the chip can be underfilled without the risk of contaminating the diaphragms. The active diaphragm is shown in the lower part of Figure 2, as seen through the access hole in the circuit board after the chip was attached and underfilled. The technique described provides a means for securely attaching and underfilling a MEMS-based pressure sensor to a circuit board while allowing the diaphragm access to the ambient fluid.

This work was done by Daniel A. Pruzan of Nielsen Engineering and Research for **Glenn Research Center**. *Refer to LEW-17212.*

Wafer-Level Membrane-Transfer Process for Fabricating MEMS

This process is well suited for structures fabricated on dissimilar substrates.

NASA's Jet Propulsion Laboratory, Pasadena, California

A process for transferring an entire wafer-level micromachined silicon structure for mating with and bonding to another such structure has been devised. This process is intended especially for use in wafer-level integration of microelectromechanical systems (MEMS) that have been fabricated on dissimilar substrates.

Unlike in some older membrane-transfer processes, there is no use of wax or epoxy during transfer. In this process, the substrate of a wafer-level structure to be transferred serves as a carrier, and is etched away once the transfer has been completed. Another important feature of this process is that two

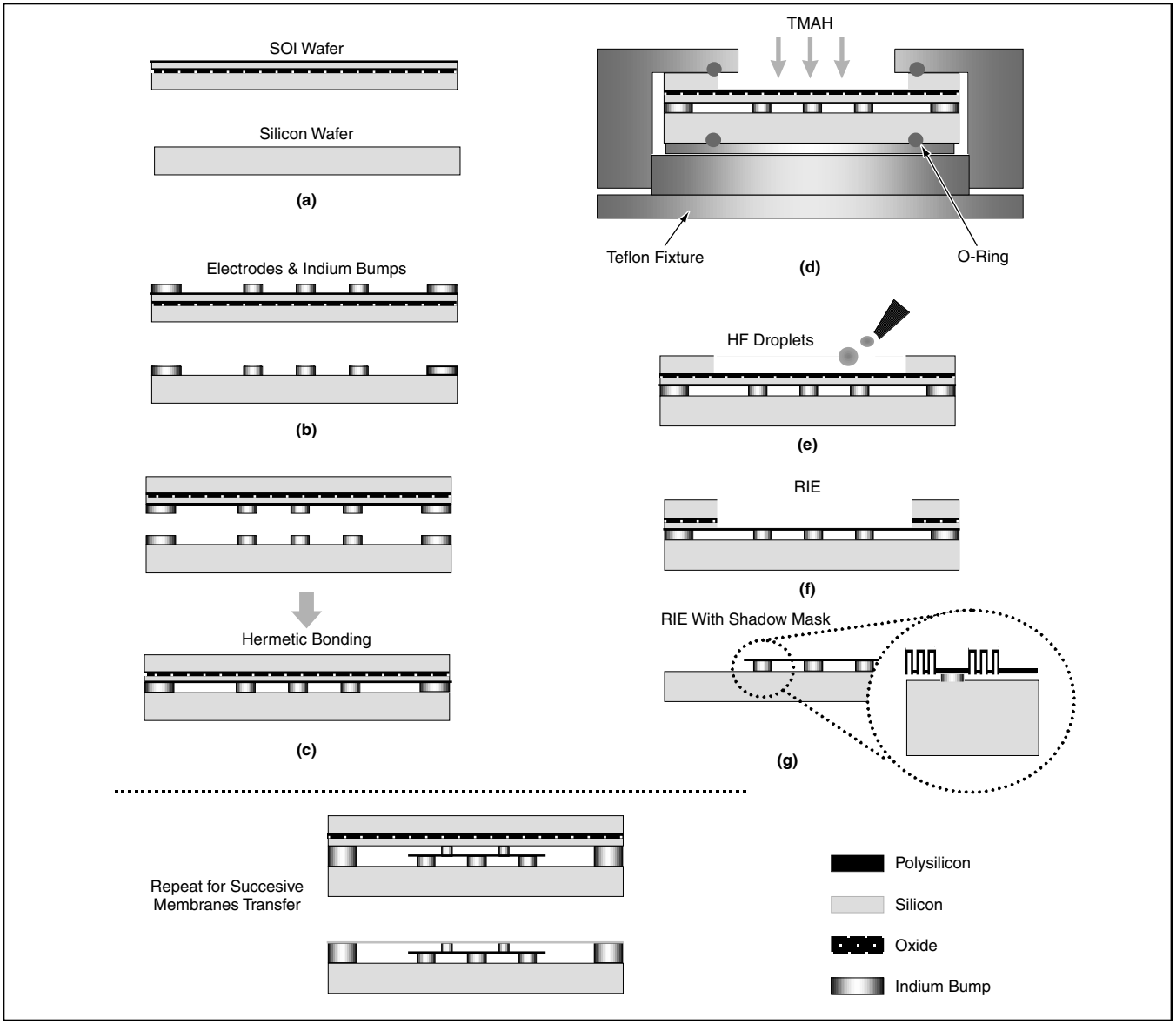

Figure 1. An **Outline of the Process** shows the key steps.

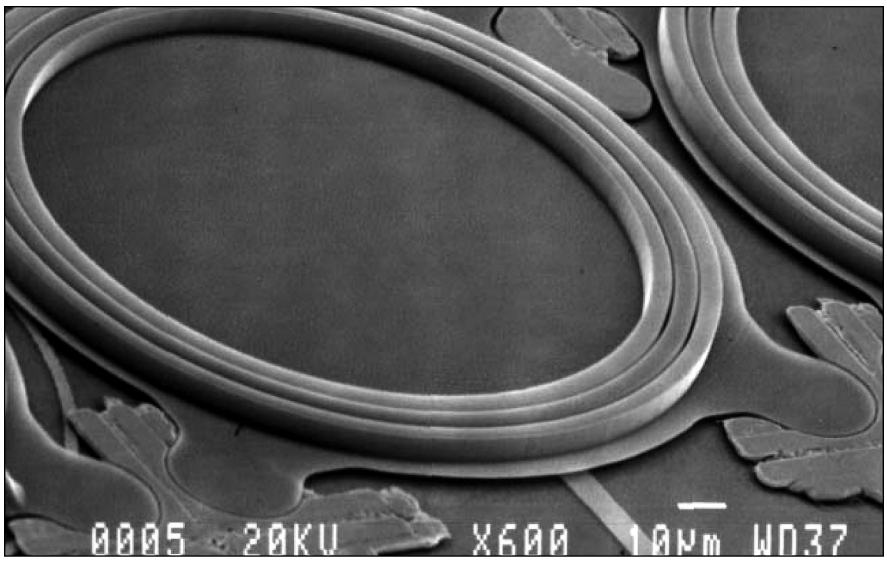

Figure 2. A **Corrugated Polysilicon Membrane**, only 1 µm thick, was transferred onto a silicon substrate to form an array of electrostatic actuators. The actuators were found to function as intended.

wafer-level structures to be integrated with each other are indium-bump-bonded together; this is advantageous in that it produces less (in comparison with other bonding techniques) stress during bonding of structures formed on two dissimilar wafers. Moreover, unlike in some older membrane-transfer processes, there is no incidental release of HF from the final structure — an advantage when indium, aluminum, or another soft metal is used for bonding.

This process was demonstrated by applying it to the joining of (1) a corrugated polycrystalline silicon (polysilicon) membrane that had been fabricated by patterning and etching on a silicon-on-insulator (SOI) wafer with (2) a silicon substrate. A 1-µm thick corrugated polysilicon membrane has been transferred onto an electrode wafer to show the feasibility of the proposed technique. The transferred membrane with underlying

electrodes constitutes an electrostatic actuator array. An SOI wafer and a silicon wafer (see Figure 1) are used as the carrier and electrode wafers, respectively. After oxidation, both wafers are patterned and etched to define a corrugation profile and electrode array, respectively. The polysilicon layer is deposited on the SOI wafer. The carrier wafer is bonded to the electrode wafer by using evaporated indium bumps. The piston pressure of 4 kPa is applied at 156 °C in a vacuum chamber to provide hermetic sealing. The substrate of the SOI wafer is etched in a 25 weight percent TMAH bath at 80 °C. The exposed buried oxide is then removed by using 49 percent HF droplets after an oxygen plasma ashing. The SOI top silicon layer is etched away by using an SF_6 plasma to define the corrugation profile, followed by the HF droplet etching of the remaining oxide. The SF_6 plasma with a shadow mask selectively etches the polysilicon membrane, if the transferred membrane structure needs to be patterned. Electrostatic actuators with various electrode gaps have been fabricated by this transfer technique. The gap between the transferred membrane and electrode substrate is very uniform (±0.1 μm across a wafer diameter of 100 mm, provided by optimizing the bonding control). Figure 2 depicts the finished product.

This work was done by Eui-Hyeok Yang and Dean Wiberg of Caltech for **NASA's Jet Propulsion Laboratory**. *For further information, access the Technical Support Package (TSP)* ***free on-line at www.nasatech.com***.

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A Reactive-Ion Etch for Patterning Piezoelectric Thin Film

Gaseous mixtures BCl_3 and Cl_2 are highly selective for etching $PbZr_{1-x}Ti_xO_3$ films.

NASA's Jet Propulsion Laboratory, Pasadena, California

Reactive-ion etching (RIE) under conditions described below has been found to be a suitable means for patterning piezoelectric thin films made from such materials as $PbZr_{1-x}Ti_xO_3$ or $Ba_xSr_{1-x}TiO_3$. In the original application for which this particular RIE process was developed, $PbZr_{1-x}Ti_xO_3$ films 0.5 μm thick are to be sandwiched between Pt electrode layers 0.1 μm thick and Ir electrode layers 0.1 μm thick to form piezoelectric capacitor structures. Such structures are typical of piezoelectric actuators in advanced microelectromechanical systems now under development or planned to be developed in the near future.

RIE of $PbZr_{1-x}Ti_xO_3$ is usually considered to involve two major subprocesses: an ion-assisted-etching reaction, and a sputtering subprocess that removes reactive byproducts. RIE is favored over other etching techniques because it offers a potential for a high degree of anisotropy, high-resolution pattern definition, and good process control. However, conventional RIE is not ideal for patterning $PbZr_{1-x}Ti_xO_3$ films at a thickness as great as that in the original intended application. In order to realize the potential benefits mentioned above, it is necessary to optimize process conditions — in particular, the composition of the etching gas and the values of such other process parameters as radio-frequency power, gas pressure, gas-flow rate, and duration of the process. Guidelines for determining optimum conditions can be obtained from experimental determination of etch rates as functions of these parameters.

Etch-gas mixtures of BCl_3 and Cl_2, some also including Ar, have been found to offer a high degree of selectivity as needed for patterning of $PbZr_{1-x}Ti_xO_3$ films on top of Ir electrode layers in thin-film capacitor structures. The selectivity is characterized by a ratio of ≈10:1 (rate of etching $PbZr_{1-x}Ti_xO_3$ ÷ rate of etching Ir and IrO_x). At the time of reporting the information for this article, several experiments on RIE in BCl_3 and Cl_2 (and sometimes Ar) had demonstrated the 10:1 selectivity ratio, and further experiments to enhance understanding and obtain further guidance for optimizing process conditions were planned.

This work was done by Eui-Hyeok Yang and Larry Wild of Caltech for **NASA's Jet Propulsion Laboratory**. *For further information, access the Technical Support Package (TSP)* ***free on-line at www.nasatech.com***.

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