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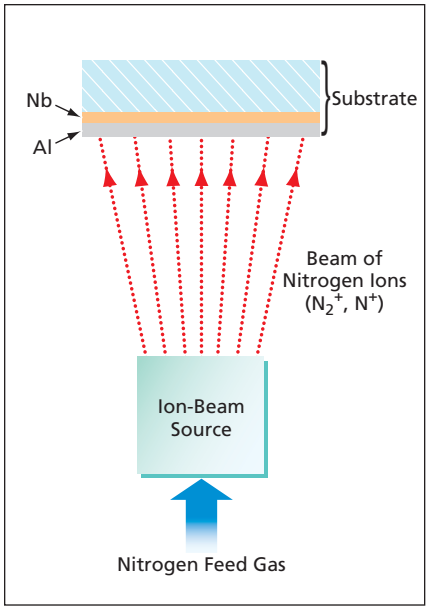

The **Beam of Nitrogen Ions** impinges on the aluminum substrate surface layer, forming an ultrathin layer of AlN_x.

ergy, flux, species, and direction promises more precise control of film characteristics such as stoichiometry and thickness than is the case with typical plasma processes. In particular, the background pressure during ion-beam nitride growth is 2 or 3 orders of magnitude lower, minimizing the formation of compounds with contaminants, which is critical in devices the performance of which is dictated by interfacial characteristics. In addition, the flux of incoming species can be measured *in situ* using ion probes so that the dose can be controlled accurately.

The apparatus used in the present ion-beam technique includes a vacuum chamber containing a commercial collimated-ion-beam source, a supply of nitrogen and argon, and an ion probe for measuring the ion dose. Either argon or nitrogen can be used as the feed gases for the ion source, depending on whether cleaning of the substrate or growth of the nitride, respectively, is desired. Once the Nb base electrode and Al proximity layer have been deposited, the N_2 gas line to the ion beam is vented and purged, and the ion-source is turned on until a stable discharge is obtained. The substrate is moved over the ion-beam source to expose the Al surface layer to the ion beam (see figure) for a specified duration for the formation of the nitride tunnel barrier. Next, the Nb counter-electrode layer is deposited on the nitride surface layer. The Nb/Al-AlN_x/Nb-trilayer-covered substrate is then patterned into individual devices by use of conventional integrated-circuit processing techniques.

A wide parameter space was investigated over which devices were fabricated reproducibly and with high quality. The hysteretic nature of the current-voltage characteristic along with the high subgap ratio indicate the incident nitrogen ions chemically reacted with the Al layer as expected, to form a continuous AlN_x barrier. Chemical analysis of the barrier performed using x-ray photoelectron-spectroscopy confirmed the presence of AlN_x. Critical current density J_c ranged from 550 to 9,400 A/cm^2 with subgap-to-normal resistance ratios ranging from 50 to 12.6. The J_c was found to decrease with increasing dose and increasing beam energy. The run-to-run reproducibility was determined to be very good. The spatial variation of the ion current density was also measured and correlated with J_c over a 76-mm Si wafer. The junctions were also found to be stable on annealing up to temperatures of 250 °C. This technique could be applied to form other metal nitrides at room temperatures for device applications where a high degree of control is desired.

This work was done by Anupama Kaul, Alan Kleinsasser, Bruce Bumble, Henry LeDuc, and Karen Lee of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).* *NPO-41297*

Making Wide-IF SIS Mixers With Suspended Metal-Beam Leads

Devices are fabricated on SOI substrates by use of silicon-micromachining techniques.

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A process that employs silicon-on-insulator (SOI) substrates and silicon (Si) micromachining has been devised for fabricating wide-intermediate-frequency-band (wide-IF) superconductor/insulator/superconductor (SIS) mixer devices that result in suspended gold beam leads used for radio-frequency grounding. The mixers are formed on 25-μm-thick silicon membranes. They are designed to operate in the 200 to 300 GHz frequency band, wherein wide-IF receivers for tropospheric-chemistry and astrophysical investigations are necessary.

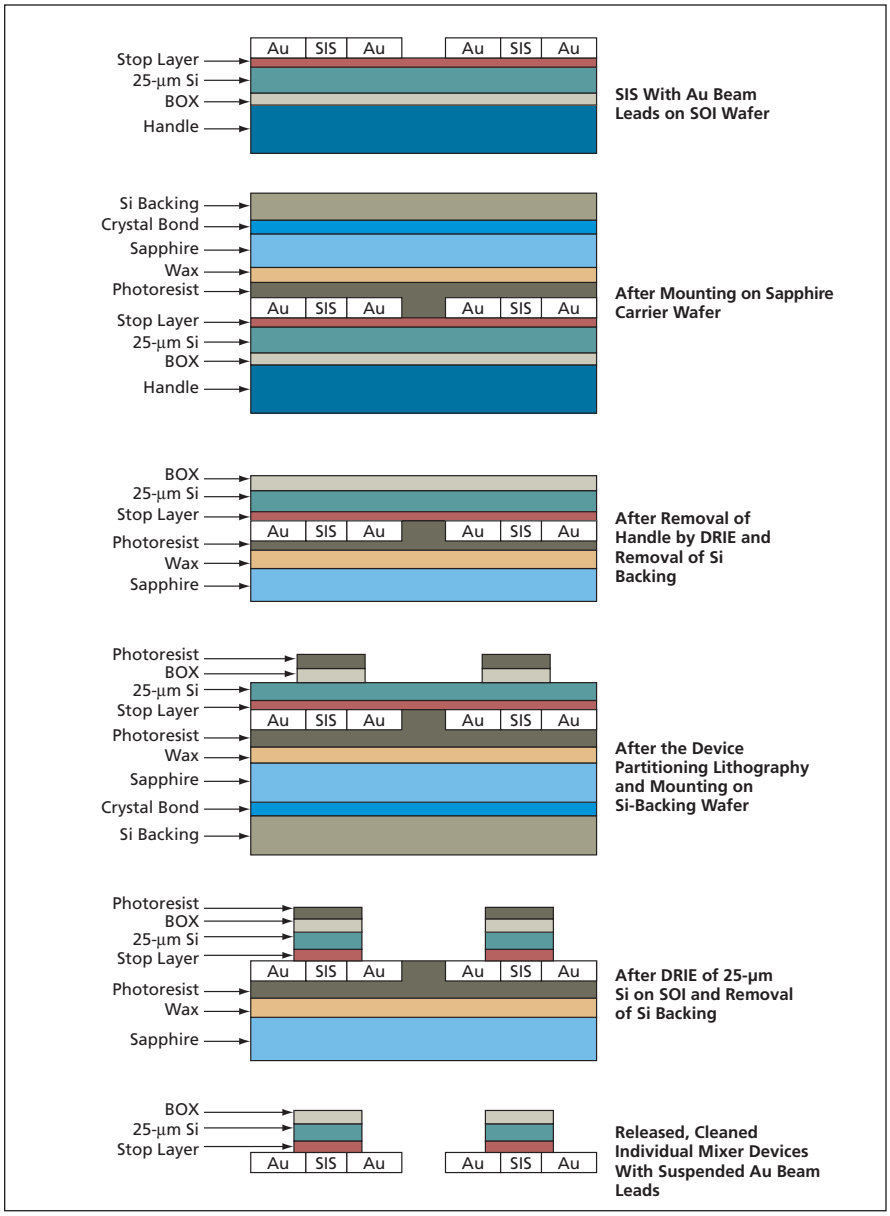
The fabrication process can be divided into three sections:

1. The front-side process, in which SIS devices with beam leads are formed on a SOI wafer;
2. The backside process, in which the SOI wafer is wax-mounted onto a carrier wafer, then thinned, then partitioned into individual devices; and
3. The release process, in which the individual devices are separated using a lithographic dicing technique.

The total thickness of the starting 4-in. (10.16-cm)-diameter SOI wafer includes 25 μm for the Si device layer, 0.5 μm for the buried oxide (BOX) layer, and 350 μm the for Si-handle layer. The front-side process begins with deposition of an etch-stop layer of SiO_2 or AlN_x, followed by deposition of a Nb/Al-AlN_x/Nb trilayer in a load-locked DC magnetron sputtering system. The lithography for four of a total of five layers is performed in a commercial wafer-stepping apparatus. Diagnostic test dies are patterned concurrently at certain locations on the wafer, alongside the mixer devices, using a different mask set. The conventional, self-aligned lift-off process is used to pattern the SIS devices up to the wire level.

The beam-leads are formed as extensions from the SIS devices by using a bilayer lift-off process with poly(methyl methacrylate) [PMMA] and photoresist. After defining the beam-leads, the interfacial layer between the PMMA and photoresist is etched in an oxygen plasma. Ultraviolet irradiation is used to expose the PMMA, which is then developed in chlorobenzene. The wafer is then placed in the sputtering system, where a seed layer of Nb/Au is deposited to enhance adhesion. The Au beam leads are grown to the desired thickness in an electron-beam evaporation system. After deposition, the unwanted gold is easily removed by lift-off in acetone.

In the next step, the backside process is initiated by wax mounting the SOI wafer onto a sapphire carrier wafer, as illustrated in the figure. The 350 μm Si-handle layer of the SOI wafer is removed by deep-trench reactive-ion etching (DRIE). Now further lithography is necessary on the 25 μm thick Si membrane layer that is held down onto a 4-in. (10.16-cm) wafer by a relatively high-melting-point wax. If the cooling on the DRIE system is not sufficient during the etching of the handle layer, the wax would start to flow at ~85 °C, causing the Si membrane to wrinkle, which would prevent any backside lithography to be performed. A contact aligner is used to pattern the now-exposed 25-μm thick Si layer in order to partition the devices into individual mixers. Since an anisotropic etch is desired for patterning the 25-μm thick Si membrane, the DRIE apparatus is operated in the pulsed mode where SF_6 and C_2F_4 are flowed intermittently. The devices are then released by dissolving the front-side protection resist in acetone, followed by soaking in an N-methyl-pyrrolidone-based solution, which removes any residual photoresist. The devices are finally dipped in IPA.



In the **Backside and Release Processes**, the SOI wafer is thinned and partitioned into individual devices, which are then released. Some of the layers depicted and subprocesses mentioned here are omitted from the main text for the sake of brevity.

Electrical measurements of the devices was performed at 4.2 K. Measurements were performed on devices that were on thinned 25-μm Si membranes and those devices where the handle layer was not removed. No change in device parameters such as current density (J_c), gap voltage, and sub-gap leakage current was observed, indicating the backside process did not introduce any thermal excursions, which would have been evident from increased leakage currents and reduced gap voltages. In addition, the J_c on the individual mixer chips correlated to the J_c that was measured on devices from the diagnostic chip. The data suggest that this wax-mounted backside lithography beam-lead process is compatible with conventional SIS device fabrication technology.

This work was done by Anupama Kaul, Bruce Bumble, Karen Lee, Henry LeDuc, Frank Rice, and Jonas Zmuidzinas of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).* *NPO-41296*