Failure Modes in Capacitors When Tested Under a Time-Varying Stress

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Abstract

Power-on failure has been the prevalent failure mechanism for solid tantalum capacitors in decoupling applications. A surge step stress test (SSST) has been previously applied to identify the critical stress level of a capacitor batch to give some predictability to the power-on failure mechanism [1]. But SSST can also be viewed as an electrically destructive test under a time-varying stress (voltage). It consists of rapidly charging the capacitor with incremental voltage increases, through a low resistance in series, until the capacitor under test is electrically shorted.

When the reliability of capacitors is evaluated, a highly accelerated life test (HALT) is usually adopted since it is a time-efficient method of determining the failure mechanism; however, a destructive test under a time-varying stress such as SSST is even more time efficient. It usually takes days or weeks to complete a HALT test, but it only takes minutes for a time-varying stress test to produce failures. The advantage of incorporating a specific time-varying stress profile into a statistical model is significant in providing an alternative life test method for quickly revealing the failure mechanism in capacitors.

In this paper, a time-varying stress that mimics a typical SSST has been incorporated into the Weibull model to characterize the failure mechanism in different types of capacitors. The SSST circuit and transient conditions for correctly surge testing capacitors are discussed. Finally, the SSST was applied for testing Ta capacitors, polymer aluminum capacitors (PA capacitors), and multi-layer ceramic (MLC) capacitors with both precious metal electrodes (PME) and base metal electrodes (BME).

The test results are found to be directly associated with the dielectric layer breakdown in Ta and PA capacitors and are independent of the capacitor values, the way the capacitors were built, and the capacitors' manufacturers. The test results also show that MLC capacitors exhibit surge breakdown voltages much higher than the rated voltage and that the breakdown field is inversely proportional to the dielectric layer thickness. The SSST data can also be used to comparatively evaluate the voltage robustness of capacitors for decoupling applications.

Introduction

Surge current testing has been widely applied to screen out potential power-on failures in solid tantalum capacitors. The test simulates the power supply's on and off characteristics. The solid tantalum capacitor can experience electrical breakdown, even below the rated voltage, due to the rapidly changing high-current turn-on pulses (surge currents). The set up and procedures for the surge test of chip tantalum capacitors has been described in MIL-PRF-55365.

A so-called surge step stress test (SSST) has also been described and applied to understand the failure mechanism in tantalum capacitors [1]. The SSST consists of rapidly charging the capacitor with incremental voltage increases. A capacitor is charged to a voltage value, held at that voltage for a constant time, and then discharged through a low resistance for the same period of time. The sequence is typically repeated five times. After the fifth pulse, the

voltage setting is increased to the next higher level. This five-pulse cycle is repeated at incrementally higher voltages until the capacitor under test is electrically shorted.

During SSST, at each voltage level, the capacitor experiences five cycles of a regular surge test, per MIL-PRF-55365. The purpose of the SSST is to distinguish the voltage level for each capacitor that failed under a high-surge current application. It is believed that the voltage across the dielectric layer is the trigger mechanism for the breakdown and that the current pushes the collapse to a catastrophic failure. In addition, an SSST profile is almost identical to the power supply's on and off characteristics in a decoupling application for capacitors. The author believes that the SSST can be extended to the characterization of other types of capacitors to reveal the dielectric breakdown mechanism under a high-surge current.

From a reliability stand point of view, SSST can be considered as a means of testing the short-term survivability under a time varying stress. This test is of equal importance to the long-term reliability testing, such as the commonly used highly accelerated life testing (HALT). However, the two tests reveal quite different failure mechanism for capacitors. In general, HALT is used to reveal the dielectric wearout failure mechanism, and SSST is used to reveal the overstress failure mechanism.

Time-Varying Stress and Weibull Distribution

In order to establish a theoretical function for time-varying stress testing, a detailed test methodology for SSST is described here; the details of the method has already been clearly described elsewhere [1]. When test begins, the capacitor is charged to a set voltage, held at that voltage for ½ second, and then discharged through a low resistance (<0.5 Ω) for ½ second. This sequence is repeated five times. After the fifth pulse, the voltage setting is increased slightly for the next set of pulses. This five-pulse cycle is repeated at incrementally higher voltages until the capacitor breaks down.

The voltage for the first pulse train V_0 is set to an experimentally determined value. The step voltage ΔV is based on the starting and anticipated failure voltage, such that a full test will take place within a limited-step sequence. Step increments of 10% of the rated voltage may be selected based on the starting voltage and range.

Figure 1 illustrates a typical SSST voltage profile as described above. The time-dependent function that defines the SSST voltage profile can thus be expressed as:

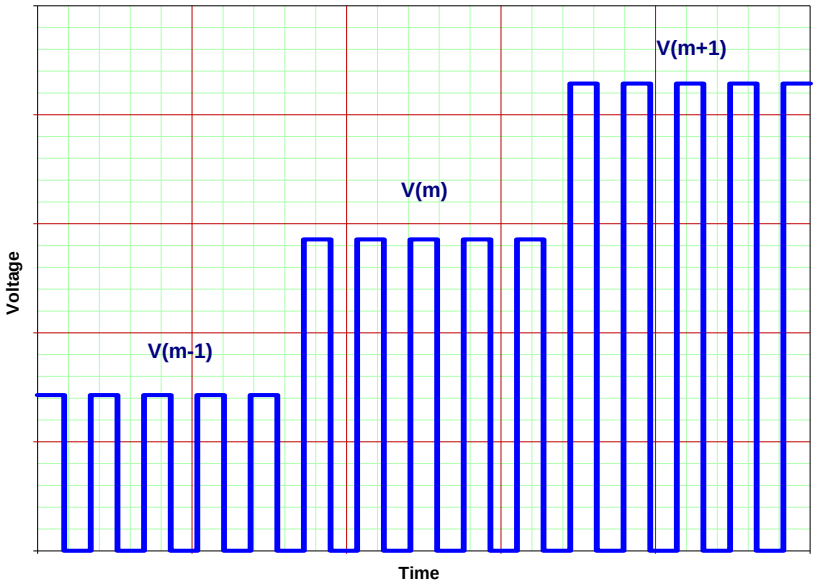


Figure 1. Illustration of a surge step voltage profile with an incremental voltage pulse.

$$\begin{cases} V_m = V_0 + m \cdot \Delta V & l-1 \le t \le l-\frac{1}{2} \\ V_m = 0 & l-\frac{1}{2} \le t \le l \end{cases} \quad l = 1,2,3,4; \quad m = 1,2,3, \ldots \ldots \tag{1}$$

Where V_0 is the initial stress, $m \cdot \Delta V$ is the *m-th* voltage level at which the capacitor failed, and l is the number of cycles at a given V_m where the capacitor failed. All of these parameters can be experimentally determined during an actual time-varying stress test.

Assuming the life distribution follows the widely used *2*-parameter Weibull, the cumulative distribution function (CDF) that provides the probability of failure at time *t* is given as:

$$F(t) = 1 - e^{-(\frac{t}{\eta})^{\beta}} \tag{2}$$

where *e* is the base for natural logarithms, *t* the failure time, β the slope or shape parameter, and η the characteristic life or scale parameter. The reliability *R(t)*, which is the probability that a failure will not occur up to time *t*, is:

$$R(t) = e^{-(\frac{t}{\eta})^{\beta}} = 1 - F(t) \tag{3}$$

When the applied stress is a voltage *V*, a power law relationship is usually assumed between the stress and the Weibull distribution scale parameter η, or:

$$\eta[V_m(t)] = [\frac{V_m(t)}{a}]^n , \tag{4}$$

where *a* is the model parameter and *n* the voltage accelerating factor. The capacitor reliability function $R(t)$ under a single stress $V_m(t)$ can be given by:

$$R[t, V_m(t)] = e^{-\left\{\frac{t}{\eta[V_m(t)]}\right\}^{\beta}} = e^{-[I(t,x)]^{\beta}}, \tag{5}$$

where:

$$I(t,x) = \int_0^t \left[\frac{V_m(t)}{a}\right]^n dx.$$

For the purpose of simplicity, the power law relationship in Eq. (4) can be expressed as:

$$\eta[V_m(t)] = [\frac{V_m(t)}{a}]^n = e^{\alpha_0 + \alpha_1 \ln [V_m(t)]} \tag{6}$$

$$\begin{cases} \alpha_0 = -\ln (a^n) \\ \alpha_1 = n \end{cases} \tag{7}$$

The estimation of Weibull parameters β and accelerating factor *n* and power law constant *a* can be accomplished using maximum likelihood estimation (MLE) method. This is a mathematically complicated approach, but it allows the determination of Weibull model parameters with limited availability of data points. The MLE method has thoroughly been described by Nelson [2].

Once the parameters in Eqs. (5) and (7) are determined, all other characteristics of interest can be obtained using the Weibull statistical properties definitions (e.g. mean time to failure, failure rate, etc.). One of the very interesting statistical properties in this study is the reliable life, t_R of a capacitor for a specified reliability at a use level of room temperature and of rated voltage:

$$t_R = \eta \cdot \{-ln[R(t_R)]\}^{1/\beta}. \tag{8}$$

Furthermore, t_R is the life for which the capacitor will function successfully with a reliability of $[1 - F(t_R)]$. If $[1 - F(t_R)] = 0.5$, then t_R = the median life.

Transient Characteristics of the Surge Step Stress Test

A typical LRC circuit for testing a capacitor's capability to withstand a surge current stress is shown in Figure 2. The input to each capacitor is isolated and buffered with a capacitor bank C_{bank} to assure high charge currents. The actual capacitance of C_{bank} must be 50,000 μF for surge testing tantalum capacitors, according to MIL-PRF-55365. The same value of C_{bank} is also selected for surge testing PA capacitors. When surge testing ceramic capacitors that have much smaller capacitance, the values of C_{bank} vary depending on the capacitance of the capacitor under test. The current limit resistor R which consists of line resistance, the equivalent series resistance (ESR) of the test capacitors is typically set between 0.001 to 0.5 Ohms.

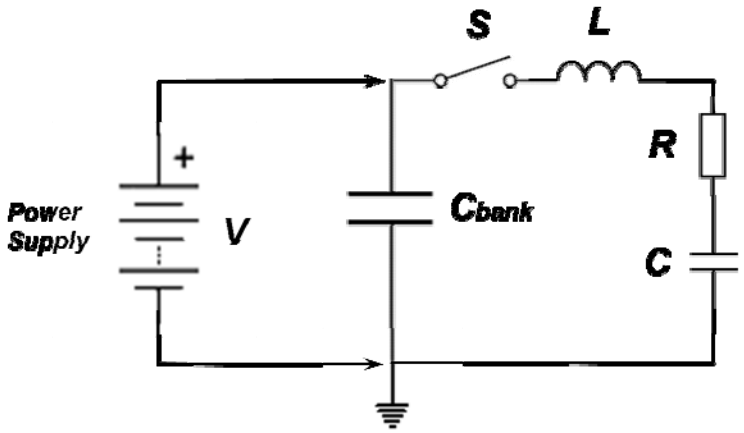


Figure 2. SSST set-up used in this study.

As has been noted, when the LRC circuit shown in Figure 2 is used for surge testing capacitors, a different test set-up may give different test results due to a different characteristic inductance that may change the surge current waveform [1]. The inductance L in Figure 2 is composed of the inductance of the switch device, the lead wires of the test circuit set-up, and the equivalent series inductance (ESL) in the test capacitors.

The bank capacitor is charged to a preset test voltage level V before the switch is closed. After the switch is closed, the charges stored in capacitor bank C_{bank} are dumped into test capacitor C. Assuming that the capacitance of the test capacitor is not changed during the charging cycle, then the charge in the test capacitor as a function of time, $\Delta C(t)$, can be easily derived from Kirchhoff's voltage law:

$$\frac{d^2\Delta C(t)}{dt^2} + \frac{R}{L} \cdot \frac{d\Delta C(t)}{dt} + LC \cdot \Delta C(t) = \frac{V}{L} \tag{9}$$

This is a typical 2nd-order non-homogeneous differential equation and its solution can be found easily in a circuit analysis textbook [3].

The general solutions of Eq. (9) can be divided into three cases based on the value of a characteristic parameter ξ. All three possible solutions for Eq. (9) have been summarized in Table I, where the critical resistance $R_{cr} = 2\sqrt{L/C}$, the dumping ratio $\xi = R/R_{cr}$, and the characteristic frequency $\omega_n = 1/\sqrt{LC}$.

Based on previous studies [4.5], the underdamped circuit condition ($\xi > 1$) represents the most severe test among all the three cases, so all of the capacitors should be surge tested with ($\xi > 1$). In this underdamped case, assuming the

capacitance in transient voltage is independent, the transient voltage built up in the capacitor can then be expressed as $V(t) = \frac{\Delta C(t)}{C}$, and the current that flows into the capacitor is $I(t) = \frac{d\Delta C(t)}{dt}$, the transient voltage and current generated by the capacitor during surge test can be further expressed as:

$$\begin{cases} V(t) = \frac{\Delta C(t)}{C} = V[1 - \frac{e^{-\frac{t}{\tau}}}{\sqrt{1-\frac{LC}{\tau^2}}} \sin\left(\sqrt{\frac{1}{LC} - \frac{1}{\tau^2}} \cdot t + \theta\right)] \\ I(t) = \frac{d\Delta C(t)}{dt} = \frac{V}{L} \cdot \frac{e^{-\frac{t}{\tau}}}{\sqrt{1-\frac{LC}{\tau^2}}} \sin\left(\sqrt{\frac{1}{LC} - \frac{1}{\tau^2}} \cdot t\right) \end{cases} \quad (10)$$

where $\tau = 2L/R$ and $\theta = tan^{-1}\frac{\sqrt{1-\xi^2}}{\xi}$ are related to circuit elements *L, R*, and *C* only.

Table I. General solutions for differential equation (10) based on three-case circuit parameters

Testing Conditions	$\xi = 0.5R/\sqrt{L/C}$	Solutions of Eq. (10) $\Delta C(t) =$
Overdamped	$\xi > 1$	$CV + e^{-\xi\omega_n t}[K_1 cosh(\omega_n\sqrt{\xi^2-1}\cdot t) + K_2 sinh(\omega_n\sqrt{\xi^2-1}\cdot t)]$
Critically damped	$\xi = 1$	$CV + (K_1 + K_2 t)e^{-\omega_n t}$
Underdamped	$\xi < 1$	$CV + e^{-\xi\omega_n t}[K_1 cos(\omega_n\sqrt{\xi^2-1}\cdot t) + K_2 sin(\omega_n\sqrt{\xi^2-1}\cdot t)]$

According to Table I, in order to surge test the capacitors in an underdamped condition, the values of *L, R,* and *C* must be estimated carefully. Since each test circuit may have different values for the circuit elements, different test set-ups may give different test results. Methods to calculate circuit elements, particularly the circuit inductance *L*, to ensure that the testing is underdamped, have been widely reported previously [5-7].

In the actual surge testing of capacitors, the determination of an underdamped condition can be performed relatively easy. As showing in Table I, only $V(t)$ and $I(t)$ exhibit a unique ringing waveform when under an underdamped testing condition. Therefore, an oscilloscope (Agilent MSO9254A, mixed signal Oscilloscope) is used to constantly monitor the transient voltage and current during the surge testing. Also shown in Figure 3, the transient is typically in a microsecond range for all capacitors.

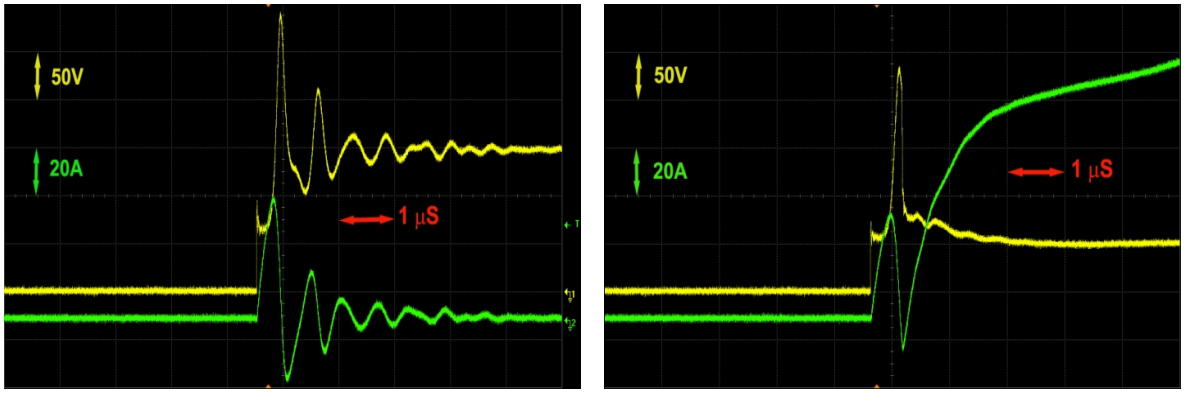


Figure 3. Typical transient voltage and current waveforms under an underdamped test condition: waveforms during a surge test cycle (left) and after a capacitor failure (right). The transient time is typically in the microsecond range.

Surge Step Stress Test Results and Discussion

1. Surge Testing of Tantalum Capacitors

A 20-unit printed circuit testing board (PCB) was used for the surge testing of capacitors throughout this study. All capacitors were solder-reflow attached on the PCB card prior to testing. The soldering reflow condition of Ta

capacitors follows MIL-PRF-55365, paragraph 4.7.10. No-clean solder paste with RMA flux was used. Only one reflow cycle was applied.

The surge step stress testing follows the procedure described by Marshall and Primak [1]. The capacitor bank C_{bank} is set at 50.000 μF, as specified in MIL-PRF-55365. The value of discharge resistor R was ranged between 0 and 0.5 Ω.

Figure 4 shows the Weibull plots of SSST data for Ta capacitors. The use level time-to-failure data points were extrapolated using Eq. (8). The time-to-failure is represented on the X-axis, and cumulative percent failed is presented on the Y-axis. The Weibull parameters β and η in Eq. (2), and the voltage accelerating factor n in Eq. (4) can be determined when the maximum likelihood estimation (MLE) approach is applied to solve Eq. (5) and (7). Corresponding Ta capacitor cathode structures and calculated *2*-parameter Weibull results are summarized in Table II. The negative values obtained for voltage accelerating factor n indicate the power law relationship expressed in Eq. (4) is in fact an inverse power law behavior.

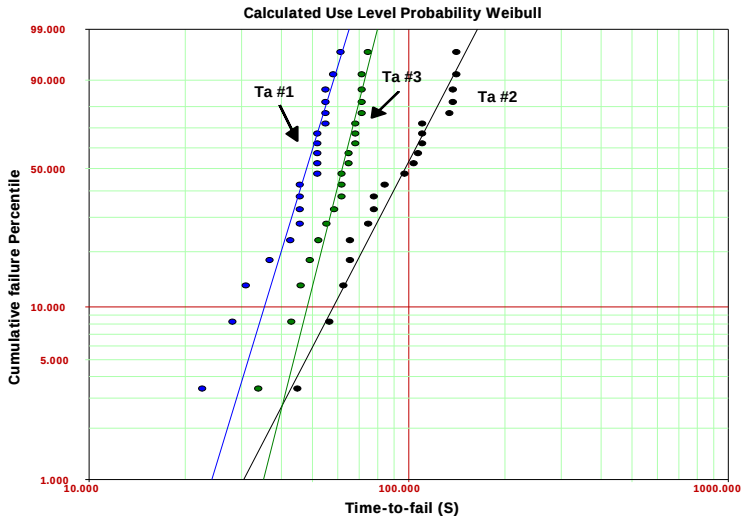


Figure 4. Calculated use level Weibull probability of SSST data for tantalum capacitors

Three groups of commercial-off-shelf Ta capacitors were selected for the surge testing. The regular MnO_2 solid tantalum capacitors (Ta#2) are from manufacturer B. The MnO_2 solid tantalum capacitors with a fuse design (Ta#1) are from manufacturer D. And the polymer tantalum capacitors that were constructed to minimize the equivalent series inductance (ESL) (Ta#3) are also from manufacturer B. Although the tantalum capacitor for SSST are quite different in their electrical values, construction, cathode structures, and manufacturers, the Weibull plots of the three groups of capacitors reveal a similar failure mode, characterized by the fairly close Weibull slope parameter β, scale parameter η and the voltage accelerating factor n. This consistency in the failure mode indicates that the dielectric breakdown is the root cause for the surge voltage testing failure, since all of the Ta capacitors have one thing in common; they all have anodized tantalum peroxide dielectric layers.

Table II. Summary of Ta Capacitor Specifications and Weibull Modeling Data

PCB ID	Cap (μF)	Rated Voltage (V)	Cathode/Structure	Mfg.	β	η	n
Ta #1	100	10.0	Solid Ta, Fused	D	4.91	95.63	-0.246
Ta #2	220	4.0	Solid Ta (MnO_2)	B	3.98	192.10	-0.247
Ta #3	220	6.0	Ta Polymer	B	6.11	112.01	-0.179

2. Surge Testing of Aluminum Polymer Capacitors

The same sample preparation and testing procedures that were previously described for tantalum capacitors were also used for polymer aluminum (PA) capacitors. The Weibull plots of SSST data are shown in Figure 5. The plot

format is the same as Figure 4 for tantalum capacitors. Table III summarizes the characteristics of the cathode structures of PA capacitors and corresponding Weibull parameters.

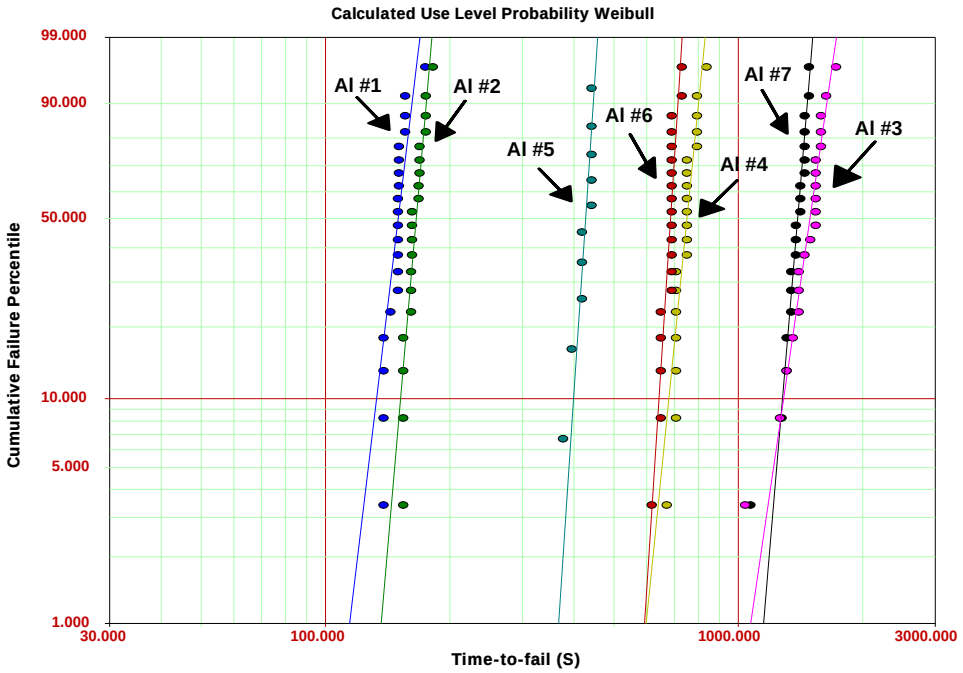


Figure 5. Weibull Plots of SSST data for Polymer Aluminum Capacitors

Again, the negative values of voltage accelerating factor n indicate an inverse power law relationship in all PA capacitors. As was reported previously [8], polymer aluminum capacitors can be divided into three groups with respect to their structures, i.e., stacked, laminated, and traditional wound. The electrical performance of polymer aluminum capacitors has been found to be highly dependent on the capacitor structures. However, the SSST data shown in Table III and Figure 5 clearly suggest that all these PA capacitors share a similar failure mechanism and similar voltage accelerating factors. The only common feature among these PA capacitors is their dielectric structure: an oxidized thin aluminum layer in a porous aluminum foil. Therefore, the identity in Weibull parameters can only be attributed to the electrical breakdown in the oxidized thin aluminum layers.

Table III. Summary of PA Capacitor Specifications and Weibull Modeling Results

PCB ID	Cap (μF)	Rated Voltage (V)	Cathode/Structure[8]	Mfg.	β	η	n
Al #1	180	6.3	Al Polymer/Stacked	A	18.62	153.61	-0.236
Al #2	150	6.3	Al Polymer/Stacked	A	22.65	168.73	-0.253
Al #3	100	12.0	Al Polymer/Stacked	B	12.81	1535.03	-0.245
Al #4	220	6.3	Al Polymer/Stacked	B	19.48	766.19	-0.254
Al #5	470	6.3	Al Polymer/Wound	C	28.19	432.36	-0.191
Al #6	100	4.0	Al Polymer/Laminated	E	29.10	694.14	-0.256
Al #7	100	2.0	Al Polymer/Laminated	E	22.30	1415.44	-0.261

Finally, a comparison of SSST data in Table II and III suggests a possible different failure mechanism in Ta and PA capacitors since the values of β are quite different for the two capacitors. The steep values in Weibull slope parameter β indicate that the dielectric layer breakdown under a surge step stress test in PA capacitors exhibits very tight and predictable time-to-failure distributions. The smaller values of β obtained for Ta capacitors, on the other hand, may be attributed to the tantalum peroxide thickness variations in Ta capacitors and may result in a relatively diversified distribution in surge breakdown voltage. This failure mechanism difference for Ta and PA capacitors can be further illustrated by the combined contour plots shown in Figure 6.

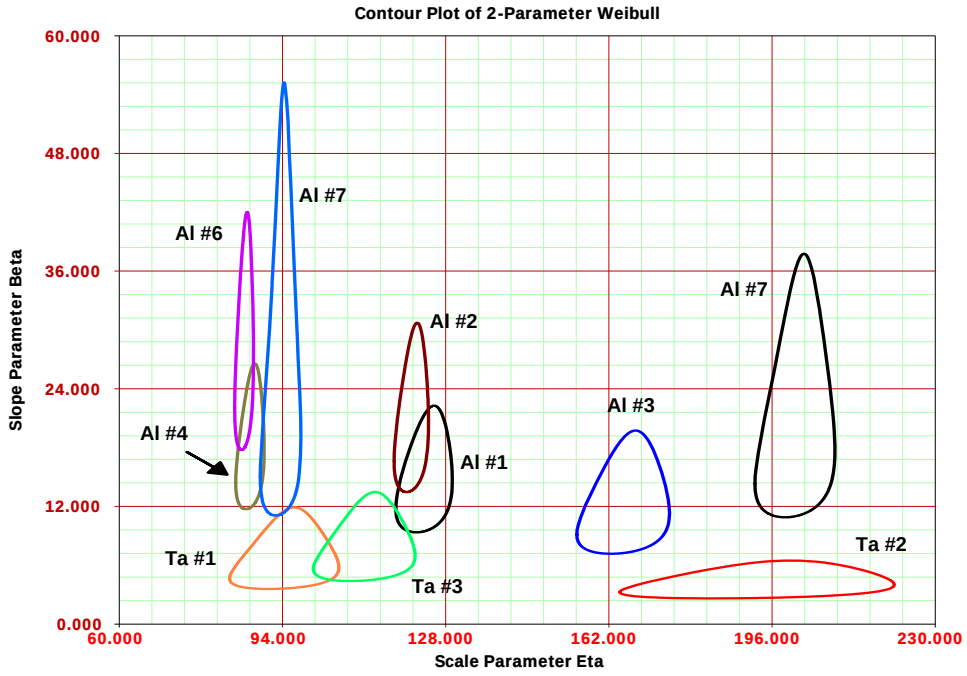


Figure 6. Contour plot with 95% confidence bound for tantalum and PA capacitors in this study.

A contour plot is a visual picture of confidence bounds on the β and η of a *2*-parameter Weibull distribution for a certain confidence level (typically 95%). Plot is often applied to compare different data sets for distinguished failure modes and to determine whether two sets are significantly different. When sample size is small (<20), a reduced bias adjustment is usually required to ensure contour plot accuracy [9].

When a horizontal line, which represents a constant value of β, is drawn in a contour plot and can cross all of the contours; it indicates the failure mode cannot be distinguished among all these data sets. In Figure 6, each data set is represented by a contour. When a horizontal line is drawn around β=5, the line will cross all three contours for Ta capacitors and will not cross any contour of PA capacitors. On the other hand, the line of β=19 will cross all of the contours for PA capacitors but not any of contours from Ta capacitors. This result indicates that SSST is a viable testing method that can successfully distinguish the failure modes between Ta and PA capacitors.

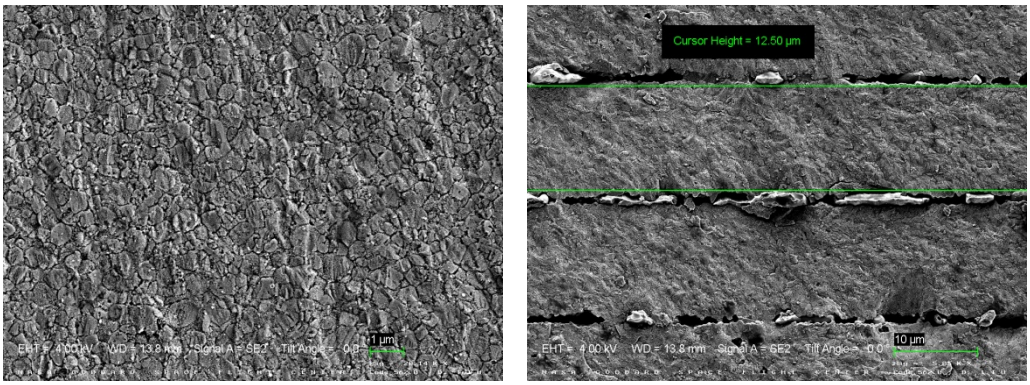
Steep, narrow contours are preferred, as they offer more predictable reliability than broad contours. It is clear in Figure 6 that most PA capacitors exhibit steeper and narrower contours than that of Ta capacitors. However, some contour overlaps between Ta and PA capacitors around β=10 indicate that the failure modes in Ta and PA capacitors are not completely irrelevant.

3. Surge Testing of MLC Capacitors

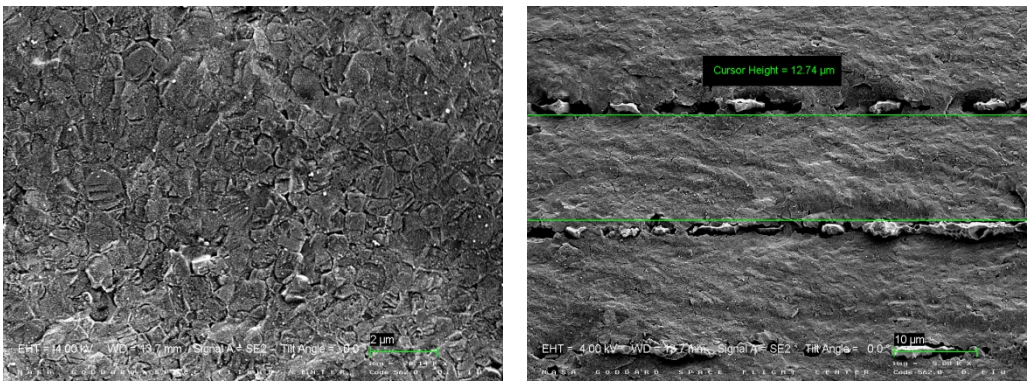
During surge testing of MLC capacitors, the value of capacitor bank C_{bank} shown in Figure 2 may not be kept at 50,000μF for all capacitors, mainly due to the fact that the capacitance of most ceramic capacitors to be surge tested is much smaller than that of Ta and PA capacitors. In practice, an underdamped condition can be readily attainable if the C_{bank} /C ratio is kept at 300-500, where C is the specified capacitance of a ceramic capacitor.

Since the dielectric strength of an MLC capacitor is highly dependent on the microstructure of dielectric materials, one sample of each type of ceramic capacitor used for surge testing in this study was subjected to a cross-section scanning electron microscope (SEM) examination for information on average grain size and dielectric layer thickness.

Figure 7 compares cross-section SEM images of a BME and a PME capacitor. The microstructure of the BME capacitor reveals a very dense grain matrix structure that is nearly the theoretical density of the $BaTiO_3$. The very uniform grain structure also indicates there was only limited degree of grain growth during the ceramic sintering. The microstructure shown in Figure 7(a) is typical of all of BME capacitors that were investigated in this study. On the other hand, the microstructure of the PME capacitors is very different from that of the BME capacitor. The most significant difference is the presence of a liquid phase in the PME microstructure. This is due to the requirement to reduce the sintering temperature so that a palladium/silver alloy can be used as an internal electrode material. The presence of a liquid phase also promotes the material transport rate during sintering and results in relatively larger grain sizes in PME capacitors. The microstructure shown in Figure 7 for PME capacitors is typical for all PME capacitors that were examined in this study.



(a). Cross-section SEM images for a BME capacitor of 0.01µF, 0805, made by manufacturer A.



(b). Cross-section SEM images of a PME capacitor of 0.01µF, 0603, made by manufacturer F.

Figure 7. Cross-section SEM images of a BME capacitor (a) and a PME capacitor (b). The microstructure and average grain size appears to be very different for the two capacitors.

For the purpose of revealing the failure mode more quickly, only those ceramic capacitors that have a 6.3 V voltage rating (5 V for a ceramic capacitor with precious metal electrode (PME)) were selected for this destructive SSST under a time-varying voltage. The ceramic capacitor specifications and the microstructure analysis data on grain size and dielectric layer thickness are summarized in Table IV.

When the transient voltage and current were confirmed to be in an underdamped condition (as shown in Figure 3), all MLC capacitors were surge tested to failure, one at a time. The test results are presented in a use level Weibull probability plot and a contour plot, shown in Figure 8. The contour plot at β=3 indicates a unique failure mode in CC-6, which is the only PME capacitor in the group. A horizontal line with β=15 can cross most of the contours for BME capacitors, except for CC-3, which indicates a possible failure mode transition among these BME capacitors during a surge test.

Table IV. Microstructure Information on the Ceramic Capacitors under an SSST

PCB ID	Cap (μF)	Chip Size	Electrode/ Mfg.	Dielectric Thickness (μm)	Avg. Grain Size (μm)	No. of Stacked Grains
CC-1	0.0056	0402	BME/B	3.0	0.44	6.82
CC-2	0.10	0603	BME/B	2.6	0.45	5.78
CC-3	1.00	0805	BME/G	2.0	0.33	6.06
CC-4	0.22	0805	BME/B	3.3	0.46	7.17
CC-5	0.01	0805	BME/A	12.5	0.59	21.2
CC-6	0.01	0603	PME/F	12.4	0.77	16.1
CC-7	0.022	0603	BME/B	4.0	0.43	9.30

Since BME and PME capacitors revealed different microstructure, as shown in Figure 7, the difference in failure modes shown in the contour plot in Figure 8 can be attributed to the revealed micro-structural difference between BME and PME capacitors.

Table V summarizes the Weibull modeling parameters β, η, and surge voltage accelerating factor n, and dielectric strength E_{50}. E_{50} is the calculated electrical breakdown field (voltage divided by dielectric layer thickness) at which 50% of the samples failed.

Table V. Results on Weibull Parameters, Voltage Accelerating Factor, and Dielectric Strength

PCB ID	Capacitance (μF)	Electrode	Dielectric Thickness (μm)	β	η	n	$E_{50}(V/\mu m)$
CC-1	0.0056	BME/B	3.0	11.91	755.77	-0.631	38.44
CC-2	0.10	BME/B	2.6	15.02	1550.21	-0.665	58.66
CC-3	1.00	BME/G	2.0	7.02	1037.44	-0.645	63.73
CC-4	0.22	BME/B	3.3	10.03	1706.22	-0.660	48.22
CC-5	0.01	BME/A	12.5	8.18	1957.02	-0.606	14.68
CC-6	0.01	PME/ F	12.4	3.11	913.30	-0.495	10.52
CC-7	0.022	BME/B	4.0	16.57	1631.19	-0.620	41.29

The negative values of voltage accelerating factor n indicate an inverse power law relationship as defined in Eq. (4). In addition, the n values for MLC capacitors are much smaller than those reported from the highly accelerated life test (HALT), which typically have an n value of 3~6 [13]. This is because the failure mechanism for SSST is quite different from that in HALT. SSST generally represents the short-term survivability of capacitors damaged due to an overstressed failure mechanism, and HALT represents the long-term reliability of capacitors due to a wearout failure mechanism.

However, the surge voltage accelerating factor n for MLC capacitors is more than twice that of the Ta and PA capacitors (see Table III and IV). This is because the dielectric material in all ceramic capacitors is ferroelectric $BaTiO_3$, which is more voltage-dependent than non-ferroelectricTaO_5 in Ta capacitors and Al_2O_3 in PA capacitors. This may also suggest the voltage accelerating factor n is a characteristic parameter for a specific dielectric material.

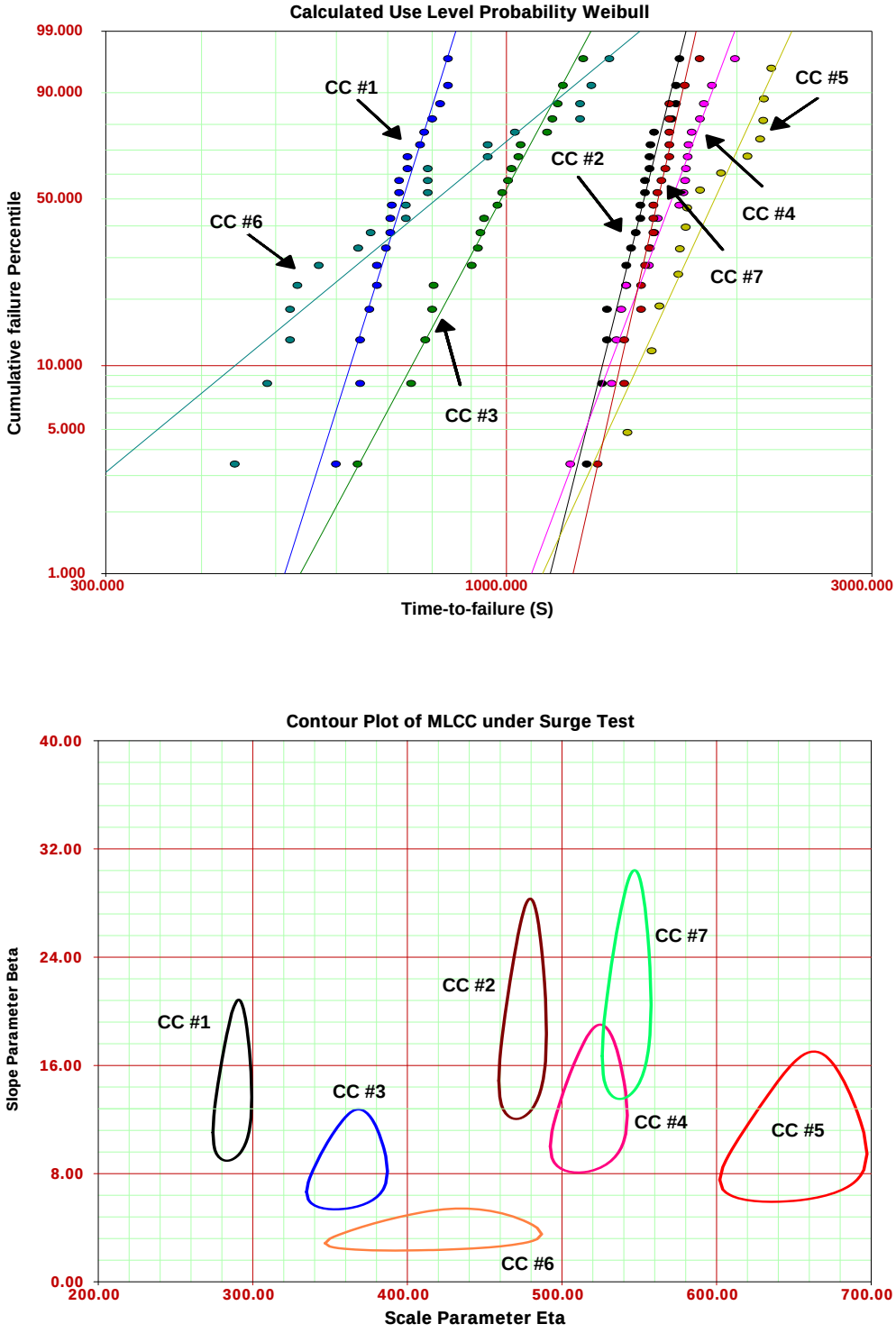


Figure 8. Use level Weibull plot as a function of time-to-failure (above) and corresponding contour plots (below) for MLCCs under a time-varying voltage. The samples are labeled according to the PCB ID shown in Table V.

When electrical breakdown filed E_{50} are plotted as a function of dielectric layer thickness, an interesting behavior is revealed, as shown in Figure 9. It is evident that the electrical strength of $BaTiO_3$ dielectric material increases as the

dielectric layer thickness decreases. Similar behavior has been previously reported [10]. In Figure 9, the data point at a dielectric layer thickness of 0.5 μm (as indicated by the arrow) was from the electrical strength measurement of thousands of integrated thin film ferroelectric capacitors [11]. The trend shown in Figure 9 is advantageous for ceramic capacitor manufacturers because BME capacitors with thinner dielectric layers should be able to sustain higher levels of electrical strength without breakdown, although the thinner dielectric layer has been reported as being a primary concern for the deteriorating long-term reliability of BME ceramic capacitors [12].

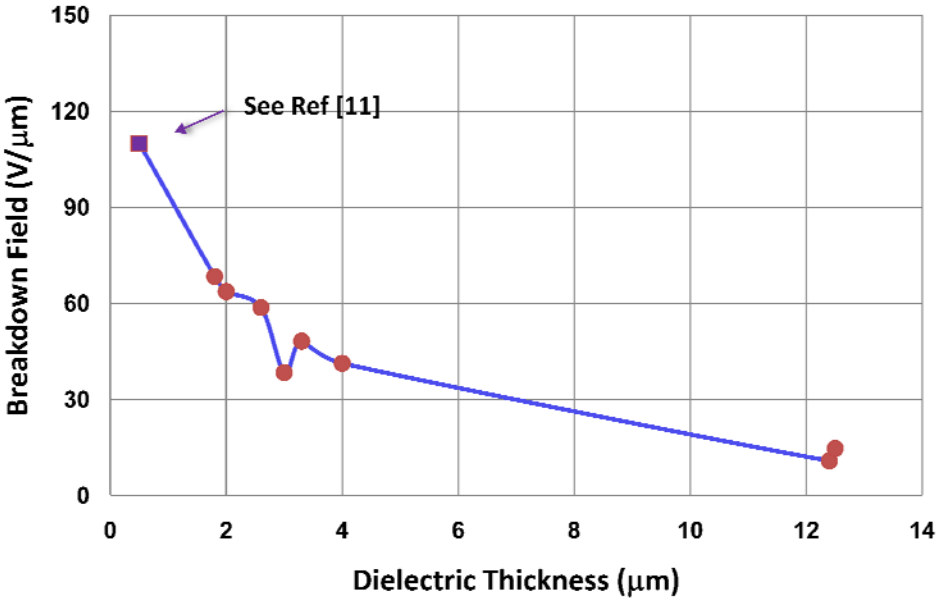


Figure 9. Electrical breakdown field E_{B50} as a function of dielectric thickness for all of the capacitors under SSST test. The point indicated by the arrow is based on test results for thousands of 0.5 μm ferroelectric capacitors fabricated using an integrated thin film technology [11].

4. Voltage Robustness in Capacitors during Surge Testing

Up to this point, all of the SSST data have been represented in a time-to-failure format. This makes it possible to use Weibull shape parameters β and η to characterize the failure modes in the capacitors, and some of the important statistical parameters, such as use level reliability and mean-time-to-failure, can be determined.

However, SSST data are often presented in a Weibull plot that uses the measured failure voltage V_{br} instead of the time-to-failure data [1]. One of the most widely used applications for capacitors is the input filtering of a power supply (decoupling). This application requires a clear understanding of the surge voltage failure process in capacitors. The SSST profile shown in Figure 1 simulates the power supply's on and off characteristics. If different types of capacitors are surge tested under a time-varying stress with the same profile and the same test set-up, the results can be used for comparative evaluation of voltage robustness in the different capacitors.

Figure 10 is a Weibull plot of SSST data, where failure voltage is presented on the horizontal scale and cumulative percent failed is presented on the vertical scale. A *2*-parameter Weibull is used to best fit the failure results. From this plot, an important failure voltage parameter called breakdown voltage at a failure rate of 100 part per million (ppm), $V_{br}(100ppm)$, can be calculated and used to estimate the rated voltage de-rating. In general, if the calculated $V_{br}(100ppm)$ is greater than the rated voltage, the capacitor de-rating will not be required. If the value of $V_{br}(100ppm)$ is less than the rated voltage, the capacitor will be de-rated accordingly [1].

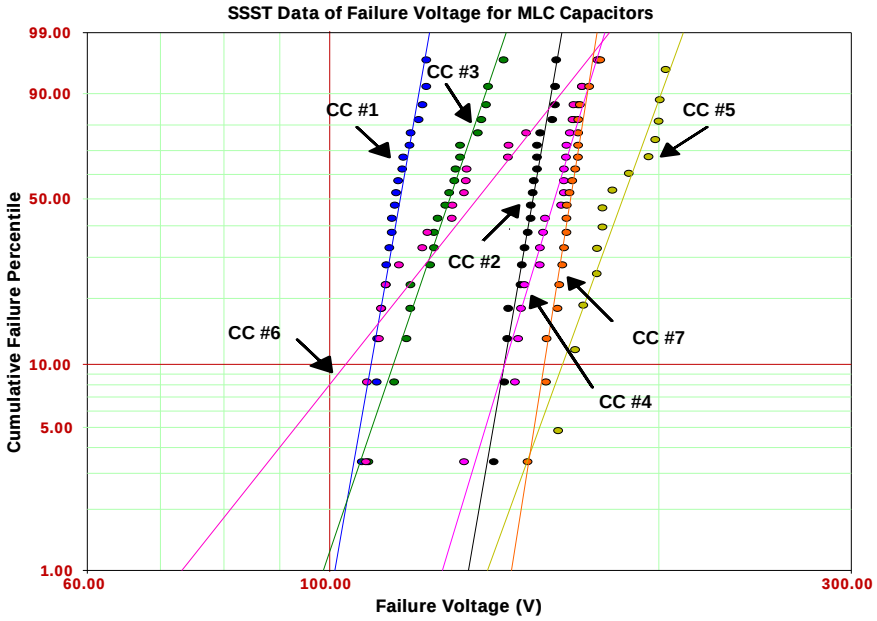


Figure 10. Weibull plot of SSST data of failure voltage V_{br} for MLC capacitors.

The calculated results of $V_{br}(100ppm)$ for all of the capacitors that were surge tested is this study are summarized in Table VI. The results clearly show that all of the tantalum capacitors need at least de-rating to 50% of rated voltage. The worst case is for Ta #2, a solid MnO_2 tantalum capacitor, where nearly 80% de-rating appears to be needed. On the other hand, no voltage de-rating is needed for the PA or ceramic capacitors. The calculated results of $V_{br}(100ppm)$ for ceramic capacitors were at least five times greater than the rated voltage, indicating a significant

Table VI. Summary of Calculated Breakdown Voltage at 100 ppm Failure Rate [$V_{br}(100ppm)$]

Capacitor ID	Rated Voltage (V)	Cathode/Electrode Structures	$V_{br}(100ppm)/V_{rated}$	$V_{br}(100ppm)$
Ta #1	10.0	Solid Ta, Fused	**0.42**	4.2
Ta #2	4.0	Solid Ta (MnO_2)	**0.27**	1.08
Ta #3	6.0	Ta Polymer	**0.57**	3.42
Al #1	6.3	Al Polymer/Stacked	1.46	9.20
Al #2	6.3	Al Polymer/Stacked	1.58	9.95
Al #3	12	Al Polymer/Stacked	1.25	15.00
Al #4	6.3	Al Polymer/Stacked	1.79	11.28
Al #5	6.3	Al Polymer/Wound	1.22	7.69
Al #6	4.0	Al Polymer/Laminated	1.83	7.32
Al #7	2.0	Al Polymer/Laminated	2.27	4.54
CC-1	6.3	Ceramic/BME	12.81	80.70
CC-2	6.3	Ceramic/BME	17.03	107.28
CC-3	6.3	Ceramic/BME	10.14	63.86
CC-4	6.3	Ceramic/BME	13.67	86.12
CC-5	6.3	Ceramic/BME	13.89	87.52
CC-6	5.0	Ceramic/PME	5.30	26.50
CC-7	6.3	Ceramic/BME	18.98	119.60

superior surge voltage robustness over both Ta and PA capacitors. Furthermore, the results of $V_{br}(100ppm)$ of all BME capacitors were at least 10 times greater than rated voltage, but only five times better for the PME capacitors. Again, this difference can be attributed to the difference in the capacitors' microstructures.

Conclusions

A time-varying stress profile that mimics a typical surge step stress test (SSST) has been implemented into a 2-parameter Weibull model. This makes it possible to characterize the failure mechanism in capacitors under a time-varying stress.

The SSST set-up and its transient characteristics were described and analyzed. The realization of underdamped surge testing conditions is discussed. Tantalum, polymer aluminum, and ceramic capacitors with various capacitances and rated voltages, different structures, and different manufacturers were surge tested using the same circuit set-up. It appears that all testing results, either time-to-fail or failure voltage, are directly associated with the dielectric layer overstress damages.

The Weibull shape parameter β is only distinguishable for different types of capacitors. The β for PA capacitors, which is relatively steeper than the β for tantalum capacitors, indicates that the PA capacitors have a tighter distribution in failure voltage and a better predicted reliability. The values of voltage accelerating factor n are nearly identical to both Ta and PA capacitors.

Among all of the capacitors that were surge tested, ceramic capacitors exhibited the highest failure voltage, at least 16 times greater than the rated voltage. The contour plots confirm that all the ceramic capacitors share an indistinguishable failure mode, with the exception of the capacitors with precious metal electrode (PME). This difference in the failure mode is attributed to the difference in the capacitors' microstructures. The dielectric strength in ceramic capacitors, as represented by E_{50}, is inversely proportional to the dielectric layer thickness, which is consistent with previous results for MLC capacitors.

The calculated results on surge breakdown voltage at 100 ppm failure rate, $V_{br}(100ppm)$, also indicates that more than 50% voltage de-rating is needed for tantalum capacitors, but not required for PA and ceramic capacitors. SSST provides a useful and relatively quick method for determining capacitor failure modes, which appear to be associated with dielectric materials and which appear to be independent of other factors, such as capacitor values, capacitor constructions, and manufacturer processing, etc.

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