Component-Level Electronic-Assembly Repair (CLEAR) Synthetic Instrument Capabilities Assessment and Test Report

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Summary

The role of synthetic instruments (SIs) for Component-Level Electronic-Assembly Repair (CLEAR) is to provide an external lower-level diagnostic and functional test capability beyond the built-in-test capabilities of spacecraft electronics. Built-in diagnostics can report faults and symptoms, but isolating the root cause and performing corrective action requires specialized instruments. Often a fault can be revealed by "emulating" the operation of external hardware. This implies complex hardware that is too massive to be accommodated in spacecraft. The SI strategy is aimed at minimizing complexity and mass by employing highly reconfigurable instruments that perform diagnostics and emulate external functions. In effect, SI can "synthesize' an instrument on demand.

The SI architecture section of this document summarizes the result of a recent program diagnostic and test needs assessment based on the International Space Station. The SI architecture addresses operational issues such as minimizing crew time and crew skill level, and the SI data transactions between the crew and supporting ground engineering searching for the root cause and formulating corrective actions. SI technology is described within a teleoperations framework.

The remaining sections describe a lab demonstration intended to show that a single SI circuit could synthesize an instrument in hardware and subsequently clear the hardware and synthesize a completely different instrument on demand. An analysis of the capabilities and limitations of commercially available SI hardware and programming tools is included. Future work in SI technology is also described.

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1.0   Introduction

The Component-Level Electronic-Assembly Repair (CLEAR) project is a task under the NASA Constellation Exploration Technology Development Program (ETDP) Supportability Project. The intent is to develop the capability to perform component-level repairs of electronic circuits in space. For an effective repair capability, designers will flank the repair process with a diagnostic capability to locate and isolate faults and a postrepair functional test capability to determine that the circuit is safe to return to service.

For the International Space Station (ISS), system telemetry can locate electrical faults down to the box or orbital replaceable unit (ORU). Each ORU has built-in-test capability that can refine the isolation down to a specific circuit-card assembly. Isolating a problem down to a single component usually requires external diagnostic equipment.

External fault diagnostics and functional test equipment may require sophisticated hardware depending on the complexity of the circuit. For a functional test, in particular, the test station used for an ORU may occupy multiple equipment racks. The volume and weight of this equipment is well beyond the foreseeable accommodations, even for a large space facility like ISS. Furthermore, this equipment is normally operated by highly trained engineers and technicians that have a thorough understanding of the equipment's operation and analysis capability. For space applications, the flight crew cannot be expected to have system diagnostic and test skills.

A strategy developed by the U.S. Navy to simplify diagnostics in the field by employing comparative characterization techniques has been used successfully. The approach used in the Navy's Gold Disk program allows relatively unskilled users to distinguish good circuits from faulty circuits by simply comparing a faulty test signature against a "known good" or "gold" signature. This approach works well for certain types of hardware faults. However, since many systems rely on a combination of software and hardware, this approach may have limited effectiveness.

Functional tests are more effective when there is software-hardware fault ambiguity. These tests, however, demand that the hardware operate in an environment where all the external interfaces are connected and are interacting with other systems. Much of the bulky automated test equipment (ATE) used in NASA's depots and integration facilities exists because of the need to emulate system interfaces. These emulators inject signals and respond to output signals from the test circuit. A circuit's external interfaces need to be emulated to reveal subtle transient problems or errors in software or communications protocols. Isolating a fault's root cause may require special equipment to stress the component and expose a stress-related anomaly.

The incorporation of all the preceding techniques in a weight- and volume-constrained environment compounded by low crew availability is driving the design toward a highly reconfigurable architecture called a synthetic instrument (SI, see "Component-Level Electronic-Assembly Repair (CLEAR) System Architecture," CLEAR–DOC–008). The objective of this report is to assess the capabilities of SI technology as a solution to the need for in situ diagnostic and test capability in the highly constrained spacecraft environment.

Section 3.0 in this report, CLEAR Synthetic Instrument Architecture, describes a strategy where instrumentation is split between real-time measurement and control functions and support for data-processing functions. Data analysis functions are offloaded to a crew workstation and to the ground-based

engineers. This strategy allows the SI to be optimized for real-time performance. Sections 4.0 and 5.0 describe the near-term approach used to demonstrate SI technology, and Sections 6.0 and 7.0 describe the SI, using a commercially available software and hardware combination, and assess the capabilities of this technology in detail. Acronyms used in this document are defined in the appendix.

2.0 Documents

The following documents contain supplemental information related to the CLEAR task.

2.1 Reference Documents

Document number	Document title
CLEAR–DOC–006	Component-Level Electronic-Assembly Repair (CLEAR) Assessment of Constellation Program In-Space Electronic Diagnostics and Repair Needs
CLEAR–DOC–008	Component-Level Electronic-Assembly Repair (CLEAR) System Architecture

2.2 Applicable Documents

Document number	Document title
CLEAR–ANA–001	Component-Level Electronic-Assembly Repair (CLEAR) Life-Cycle Cost Impacts of Different Approaches for In Situ Maintenance of Electronics Hardware
CLEAR–ANA–002	Component-Level Electronic-Assembly Repair (CLEAR) Noncontact Coupling Techniques for Performing Signature Analysis
CLEAR–DOC–001	Component-Level Electronic-Assembly Repair (CLEAR) Component Repair Experiment 1 (CRE–1) Flight System Requirements Document
CLEAR–DOC–002	Component-Level Electronic-Assembly Repair (CLEAR) Component Repair Experiment 1 (CRE–1) Concept and Hardware Summary
CLEAR–DOC–003	Component-Level Electronic-Assembly Repair (CLEAR) Recommendations for the Design of Electronic Assemblies for NASA's Exploration Program
CLEAR–DOC–004	Component-Level Electronic-Assembly Repair (CLEAR) Trade Study: Current Technologies and Instruments for Electronic Fault Diagnosis and Repair
CLEAR–DOC–005	Component-Level Electronic-Assembly Repair (CLEAR) Analysis of the Problem Reporting and Corrective Action (PRACA) Database of the International Space Station On-Orbit Electrical Systems
CLEAR–DOC–006	Component-Level Electronic-Assembly Repair (CLEAR) Assessment of Constellation Program In-Space Electronic Diagnostics and Repair Needs
CLEAR–DOC–007	Component-Level Electronic-Assembly Repair (CLEAR) Operational Concept
CLEAR–DOC–008	Component-Level Electronic-Assembly Repair (CLEAR) System Architecture
CLEAR–DOC–009	Component-Level Electronic-Assembly Repair (CLEAR) Recommendations for Enabling Manual Component-Level Electronic Repair for Future Space Missions
CLEAR–RPT–001	Component-Level Electronic-Assembly Repair (CLEAR) Component Repair Experiment 1 (CRE–1) System Requirements Review (SRR) Panel Report
CLEAR–RPT–002	Component-Level Electronic-Assembly Repair (CLEAR) Soldering in Reduced Gravity Experiment (SoRGE) Mission Test Report
CLEAR–RPT–003	Component-Level Electronic-Assembly Repair (CLEAR) Spacecraft Circuit Diagnostics by Analog and Complex Signature Analysis

3.0 CLEAR Synthetic Instrument Architecture

3.1 Diagnostic and Test Needs

The driving requirements for SIs are based on the needs described in "Component-Level Electronic-Assembly Repair (CLEAR) Assessment of Constellation Program In-Space Electronic Diagnostics and Repair Needs" (CLEAR–DOC–006). Figure 1 and Figure 2 and indicate the diagnostic and test capabilities needed to support in situ repair of ISS electronics.

For analog circuits, there are three primary performance factors that determine the innate complexity of the instrumentation required to diagnose problems: bandwidth, channel count, and dynamic range. These parameters have been used as axes on Figure 1, where these three factors are plotted for selected electronics ORUs. Figure 1 shows that there is a wide range of analog signals and corresponding instrument capabilities required.

Because digital circuits have a fixed voltage range, they are characterized by channel count and speed (frequency) as shown in Figure 2. Lunar systems can be expected to have similar signal types and comparable channel counts. However, the digital systems on lunar systems are expected have higher data rates than shown here by at least an order of magnitude.

Each distinct coordinate on these charts could require a separate instrument with distinct data-processing needs. The resulting capability would require multiple equipment racks and associated upmass and launch cost penalties. Since such accommodations are not feasible for lunar operations, an alternative strategy is required.

ATU   Audio Terminal Unit
CVIU   common video interface unit
IF   intermediate frequency
I/O   input/output
MDM   Multiplexer/Demultiplexer Module
RF   radiofrequency
RPCM   Remote Power Controller Module
SGTRC   Space-to-Ground Transmitter Receiver Controller
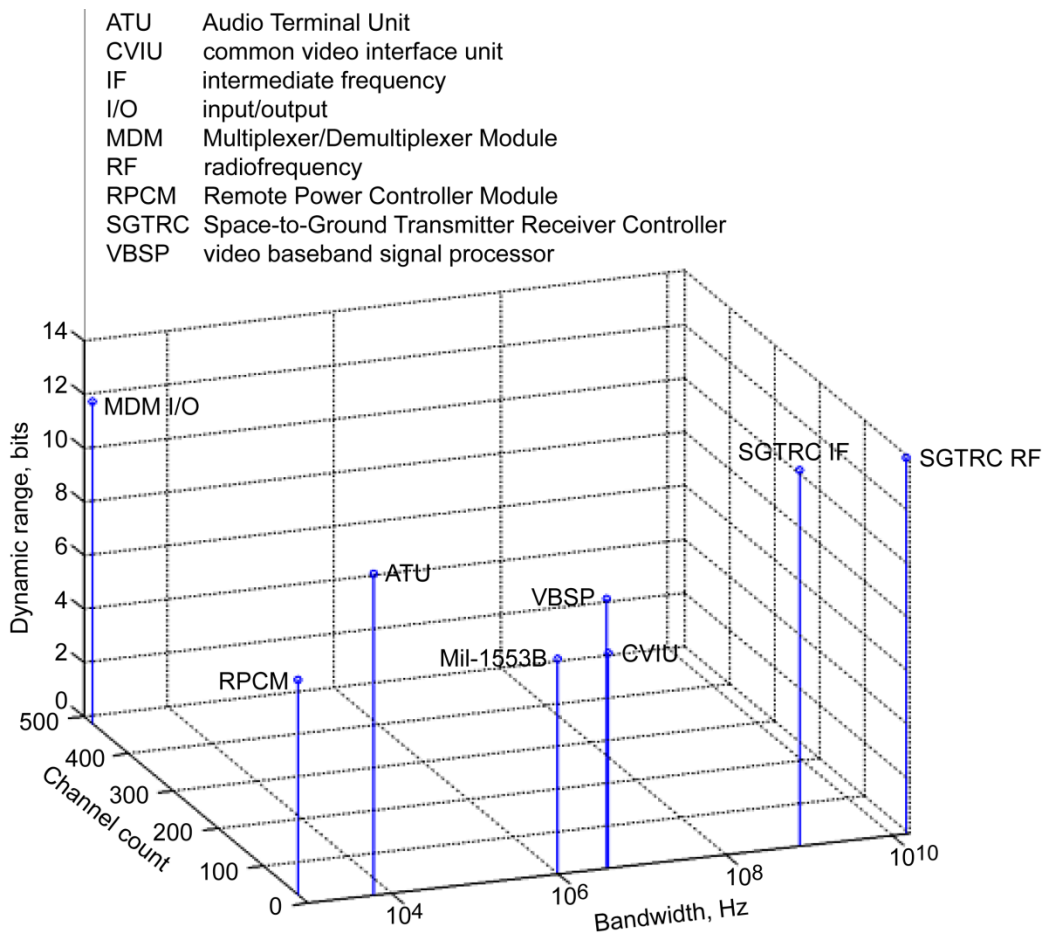VBSP   video baseband signal processor

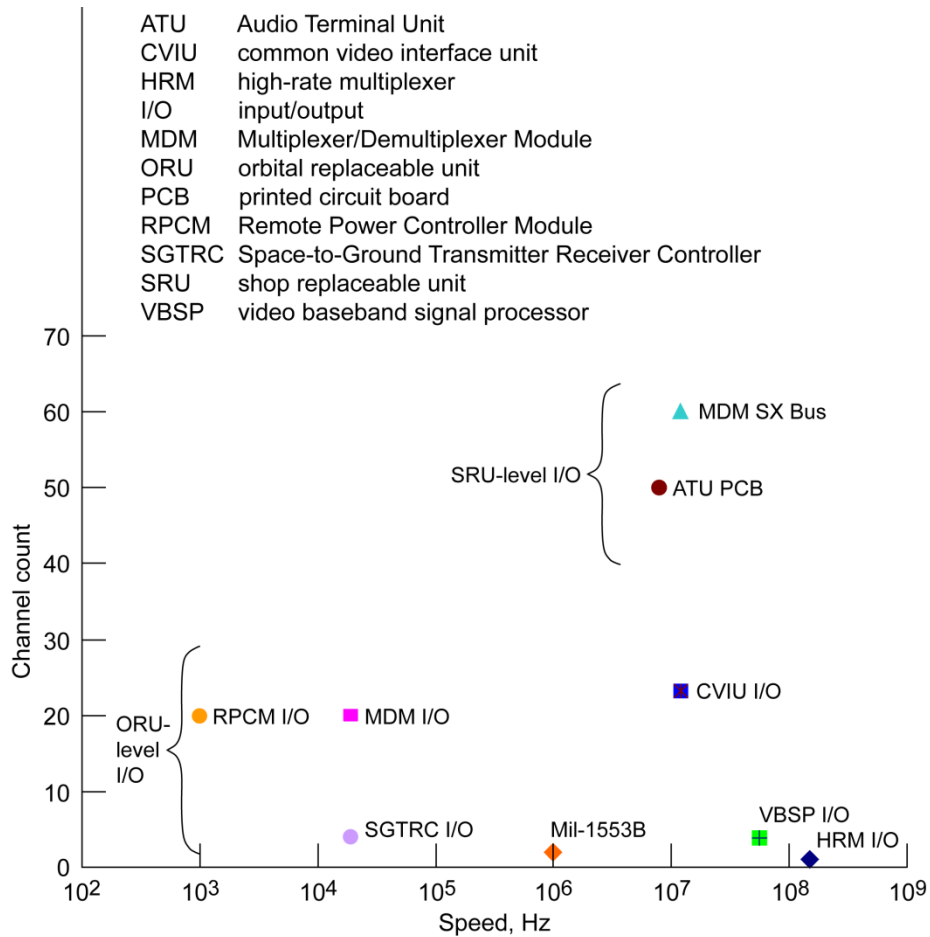Figure 1.—Analog signals for International Space Station (from CLEAR–DOC–006).

Figure 2.—Digital signals for International Space Station (from CLEAR–DOC–006).

3.2   Defining Synthetic Instruments

Most automated test equipment is composed of conventional instruments and is managed by a central controller or computer. Many ATE systems have a set of data acquisition boards alongside the conventional instruments. For discussion, we will refer to conventional benchtop instruments as "true instruments." These instruments must be "deterministic," that is, they must respond instantly within very predictable time frames. Display and user control functions are handled separately or as a low-priority process. A true instrument exploits specialized signal processing and parallel data architectures. True instruments also have a high-performance analog front end that provides very high speed measurement capturing and incorporates filtering, calibration, scaling, and digital conversions. True instruments achieve high performance through specialized design and hardware selection to meet a specific measurement objective. CLEAR SIs will be composed of application-specific integrated circuits (ASICs) that are custom designed at the silicon level. Furthermore, they are being designed as stand-alone instruments that provide their own control panels and displays. Even though they have high performance, because of their customized designs they lack flexibility. The duplication of controls, displays, power supplies, cooling, data processing, and even enclosures results in an ATE system that is physically large and that uses mass and volume inefficiently.

A virtual instrument (VI) employs software that interacts with plug-in digital and analog input/output (I/O) boards. The VI approach attempts to replace hardware functions with software functions that rely on a personal computer (PC) central processing unit (CPU) to perform the bulk of the timing, control, and data handling. The CPU must also support operating system functions and manage user interfaces. The

penalty is relatively low performance in comparison with a true instrument. PC software VIs are easy to reconfigure and can be loaded on demand to support varied applications, but the plug-in I/O hardware limits flexibility.

SIs are aimed at reducing mass, volume, and power by exploiting the strengths of VI and true instrument architectures. CLEAR SI will exploit software to provide general-purpose user interfaces and eliminate dedicated manual controls, fixed displays, and redundant features. For performance, SI will deploy data-processing algorithms in hardware capable of much higher performance than software executed by a CPU. The concept of an SI is based on the premise that test instrument algorithms reside in a field-programmable gate array (FPGA). Because FPGAs are reprogrammable, a unit programmed to perform a specific function can be erased and subsequently reprogrammed to perform a completely different function with a completely different architecture. The FPGA SI can act independently of a user's PC and exploit parallel processing to assure high performance. SI, therefore, combines the flexibility of software with high-performance hardware. Furthermore, an SI can synthesize an instrument on demand.

3.3   Synthetic Instrument Strategy

SI is a scheme to create a general-purpose ATE that can accommodate a wide range of test articles and test procedures. Flexibility and programmability are its primary objectives. SI also appears to be the best option for achieving a compact, lightweight system that is versatile and easier to update by remote uploads.

Normally an ATE is composed of a mix of equipment. This includes emulators of specific external equipment, programmable power supplies, and rack-mounted signal generators, scopes, and analyzers. Each test circuit needs a custom configuration, and supporting many different circuit diagnostic and test needs implies a large set of equipment. To assure a wide range of utility for a minimum-sized package, it is necessary to devise a system where instruments can be created, or "synthesized," on demand.

Virtually all instruments are composed of a mix of analog and digital devices. Most modern instruments have a relatively small analog front end that is supported by many digital control and data-processing functions. So that the instrument hardware can be distilled into a smaller package, designers offload many data-processing functions to an external computer. Certain high-speed, real-time digital functions that are vital to the instrument's performance are best performed by hardware. The latest generation of programmable devices can perform complex high-speed data processing. Since these devices are reprogrammable, they also can be reconfigured into completely new instruments.

It is the ability to configure a high-performance instrument in hardware that distinguishes SI from other software or VI approaches. The ability to synthesize the digital portion of an instrument is demonstrated and discussed in detail later in this report. The technical issues related to the design of a flexible analog front end and signal routing also are discussed, but development is a future effort.

In addition to the need for a flexible compact system for testing a wide array of spacecraft electronics, the system must not create a substantial workload for the flight crew or significantly increase training requirements. The CLEAR approach to SI offloads a number of data processing and user interface functions to portable computers. In addition, it offloads some functions to remote ground support. The software tools required to synthesize an instrument design are also part of the ground-support functions. Therefore, elements of the SI approach are distributed over a communications network. This, in turn, requires an overall strategy.

The CLEAR SI strategy involves

- Partitioning functions between Space and Earth segments
- Allocating (offloading) data-processing and analysis functions to the Earth segment
- Employing analog front-end hardware with the greatest possible range and bandwidth
- Exploiting digital functions instead of analog functions where possible
- Employing FPGA technology to synthesize digital functions
- Employing signal routing to match instruments to specific circuit connections
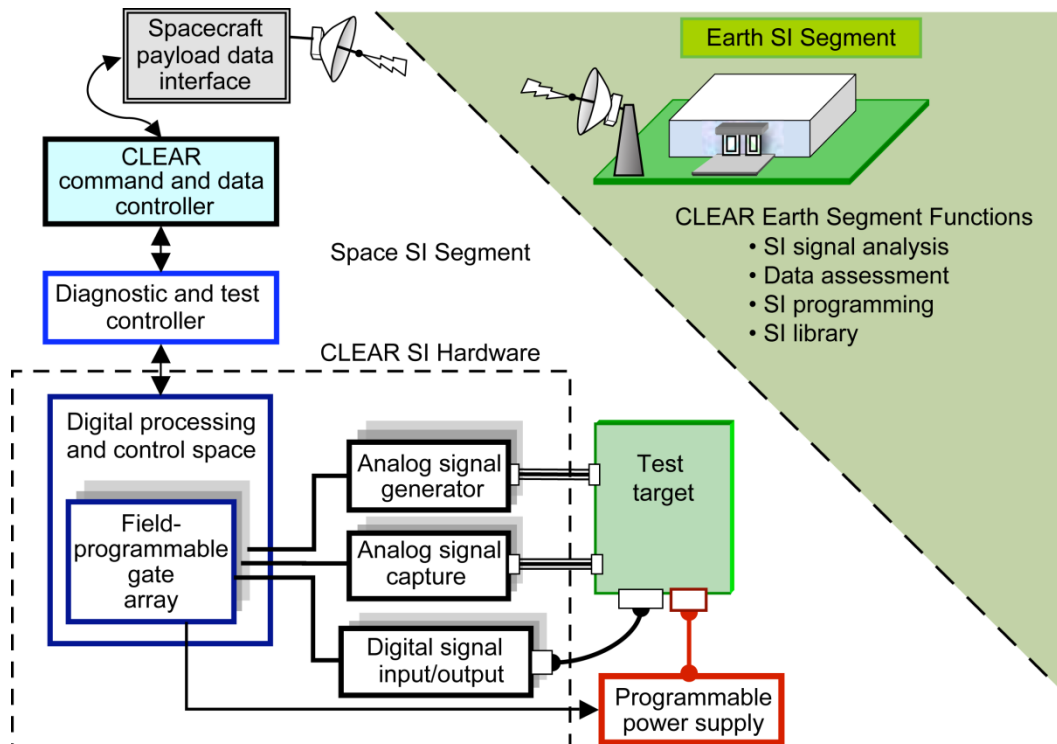
Figure 3.—The synthetic instrument (SI) architecture is partitioned into Space and Earth segments.

3.4   Allocating Synthetic Instrument Functions to Space and Earth Segments

The CLEAR system architecture (CLEAR–DOC–008) is composed of a Space and an Earth segment for both hardware and software (Figure 3). CLEAR SI also is partitioned in that manner. The intent is to provide the essential signal capture and generation capability on orbit and to offload the signal processing related to analysis and display to the Earth segment.

The Earth segment, or CLEAR Teleoperations Engineering Support Team (TEST) Center, will process the raw data sent by the Space segment and perform the analyses, assessment, decisionmaking, and action planning for the next phase of the process. This segment is well within the current technology base.

3.4.1   Earth Segment Functions

The following functions will be part of the Earth segment (CLEAR TEST):

- Data processing and storage
- Data analysis
- Data assessment
- SI control programming
- SI library (database management)

3.4.2   Space Segment Functions

The space segment can be considered to be the front end of a diagnostic and test system. That is, it provides the interface with the test target and acquires the raw data. However, for a complete solution including the postrepair functional tests, the Space segment will need to provide the supporting emulation capability. The following functions will be part of the Space segment.

- Measurement capture including signal conditioning and analog-to-digital converter (ADC) conversions
- Stimulus generation including digital-to-analog converter (DAC) conversions and filtering
- Timing and triggering
- I/O interface emulation
- Signal routing
- Crew and spacecraft interfaces

3.5 Synthetic Instrument Functions

3.5.1 Space Segment Analog Front End

Although SI relies on exploiting digital domain capabilities, instrumentation and measurements start in the analog domain. Analog hardware is the primary restriction on SIs, and the sooner signals are converted to digital, the easier it is to exploit SIs. The analog front end refers to both analog input and output. For an all-purpose system, these devices must have an inherent ability to be configured over a wide range of parameters. Figure 4 and Figure 5 illustrate the differences between analog and digital signal capture and signal generation.

When a specific application cannot be accommodated by a reconfigurable or programmable device, then add-on modules may be inserted into the system as a temporary means of extending capability. Generally the add-on approach is how CLEAR SIs will handle variations of physical connectors and wiring or will accommodate special external sensors. For example, a high-voltage measurement that is beyond the safe range of the analog front end may be required for a specific instance. An add-on solution would be to provide a high-voltage probe that preconverts the voltage down to a safe level. Similarly, it is common to use radiofrequency (RF) upconverters and downconverters to convert extremely high RFs to a range that common equipment can handle and to avoid extremely expensive RF instruments.
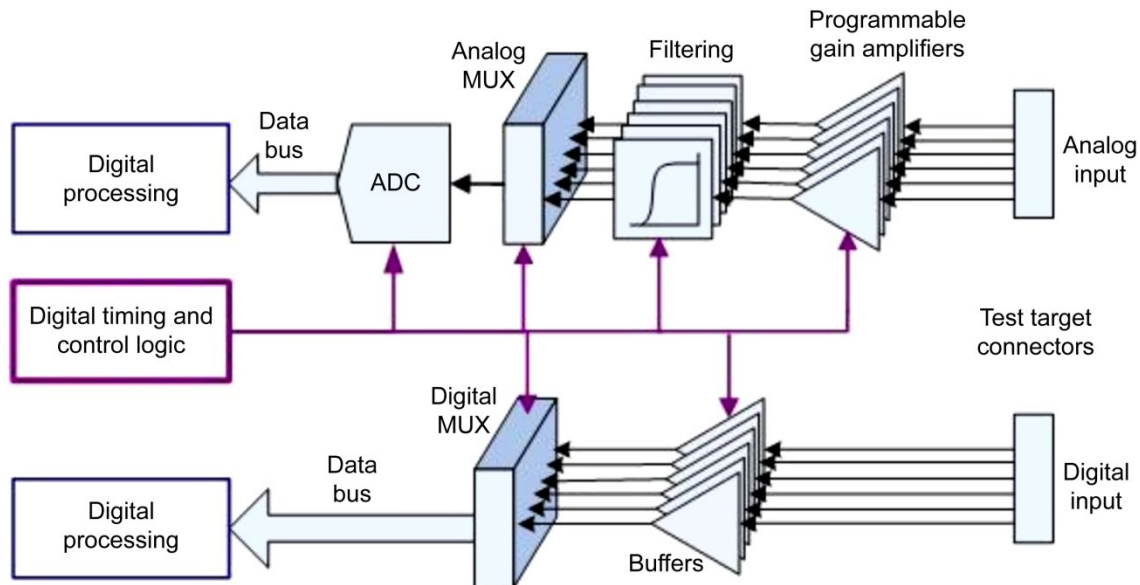

Figure 4.—Synthetic instrument signal capture for analog and digital signals. Analog signals must be digitized by an analog-to-digital (A/D) converter (ADC). The A/D conversion may consume from 8 to 24 digital channels for every single analog channel. The multiplexer (MUX) is used to select which individual channel is to be converted.
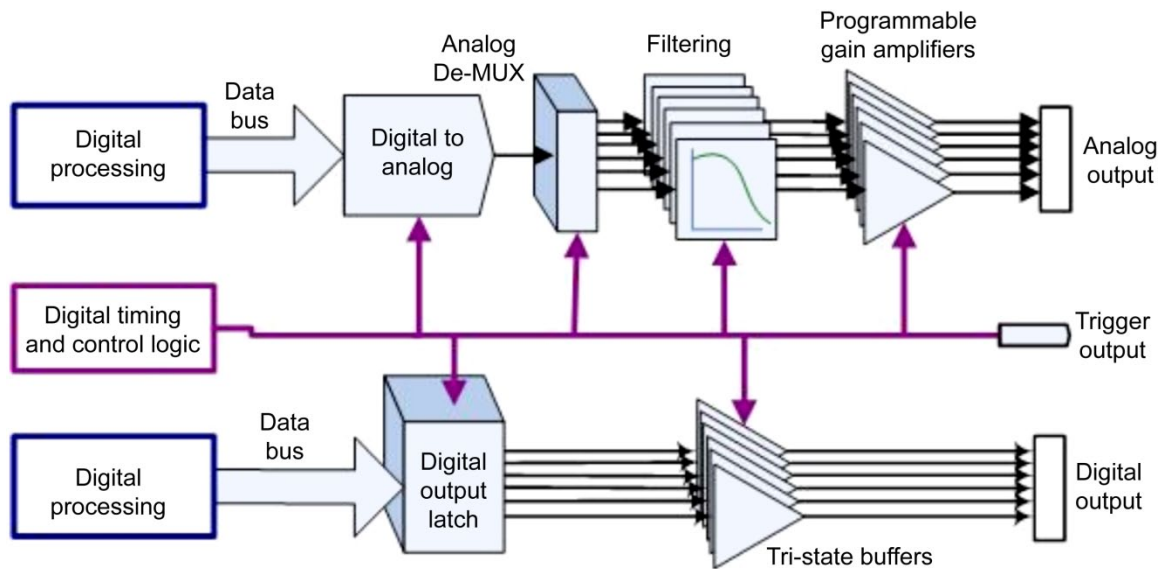
Figure 5.—Analog and digital signal generation. Analog signals are constructed by the digital-to-analog converters. The demultiplexer (De-MUX) routes the analog signal to the appropriate output channel.

3.5.2 Analog Signal Conditioning

Signal conditioning involves the analog manipulation of the signal to make it suitable for measurement by electronic devices. Raw signals may include low-voltage thermocouple measurements, high-voltage power measurements, high-impedance logic signals, or 50-Ω impedance frequency RF signals. Each type of measurement requires specific input conditions to prevent signal distortion or even damage to the instruments. The input signal must be preconditioned for the measurement instrument. Signal conditioning involves signal amplification or attenuation and filtering. For flexibility, the instruments must have a fully programmable signal-conditioning section.

As shown in Figure 4, signal amplification improves the signal-to-noise ratios of measurements and increases the resolution and sensitivity of measurements by matching signal magnitudes to the acquisition ranges. Signal filtering will allow signal shaping and rejection of unwanted noise from power lines and will prevent signal aliasing. In many cases, signal isolation may be built in to remove common-mode voltage errors caused by differences in grounding potentials. The sample-and-hold function is the last point where the signal is analog. This function samples the continuous signal and holds it, upon triggering, at a steady value so that the ADC can read it in and convert it to digital. Once the sample is read into the converter, the sample-and-hold circuit is retriggered to capture another sample. In many systems, the ADC is also multiplexed to sample many signal inputs where all channels are simultaneously sampled (and held) and the ADC converts each channel in a rapid sequence. As a result, all analog channels have a synchronized signal capture and conversion process.

3.5.3 Analog-to-Digital Conversion

The ADC receives the preconditioned signal and converts it to digital data. The digital word generated depends on the device but is typically an 8-, 10-, 12-, or 16-bit word. The word size defines the resolution of the measurement. Once the signal is converted to digital format, the remaining processes are handled in the digital domain.

3.5.4 Digital Signal Processing

Data can be stored in both a raw form and a processed form. Storing raw unprocessed data is important since there may be many different ways of processing data to reveal different signal properties.

For conventional instruments, considerable computational power is dedicated to processing, formatting, and presenting the data to the user in an understandable format. For CLEAR, most of the digital data formatting process is allocated to the Earth segment. If data are to be viewed by the crew, the format processing for analysis and display may be performed by the crew's interface computer. This allows the Space segment to focus on controlling the analog section, routing signals, packaging data, and transmitting raw diagnostics data.

For the ground-based CLEAR TEST, data analysis involves processing and presentation of diagnostics data. In addition, CLEAR TEST can employ analysis tools to extract characteristics not easily visible in the raw data.

3.5.5   Digital Control of Analog Functions

There are several instances where a digital device can enhance the range and function of a dedicated analog device.

- Amplifier gain and attenuation control
- Absolute voltage and differential voltage
- Input impedance
- Temperature compensation
- Voltage reference (calibration)
- Input filter frequency band
- Sample rate, sample resolution, and sample hold time
- Signal multiplexing control
- Trigger source, trigger delay, and trigger level

Virtually any adjustment that can be made on the front panel of an instrument can be handled by digital control of an analog device. In some cases, an analog function can be replaced completely by a digital function. For example, certain forms of digital filtering can eliminate equivalent analog filtering. The digital filter may actually be a mathematical algorithm that filters digitized data in a digital signal processor. Again, CLEAR would handle this digital process on the ground.

3.5.6   Digital Input/Output and Interfaces

Most avionics ORUs have a mix of analog and digital input and output signals. At the ORU level, the digital signals may take the form of a serial data bus. For ISS, the standard is the MIL–STD–1553 bus that was developed and deployed in the 1970s for aircraft avionics and fly-by-wire control systems. For the Constellation program, the current data bus is a local area network known as the time-triggered gigabit Ethernet (TTGbE), which is described in the "Data Backbone" section of CLEAR–DOC–008. These interfaces, though physically simple, have complex and redundant protocols and driver software. A specialized TTGbE digital network analyzer with preprogrammed test functions may be the simplest option.

At the SRU level (usually the CCA) digital input/output (DIO) interfaces are likely to require large backplane connections with dozens of data, address, and I/O lines. The SI approach is easily adopted for parallel data bus applications where all channels are digital. Digital signals do not need analog signal conditioning and only require digital buffers or isolators to protect the instrument from circuit faults. The SI can bypass the analog section and link directly to the digital test target. As shown in the SI signal capture diagram (Figure 4), digital signal capture does not require amplifiers, filters, or analog-to-digital (A/D) converters.

The SI also can be set up as a traditional logic analyzer to test DIO. The most common application will likely be to serve as a digital emulator. The emulator could be programmed to interact with the target by emulating a device that would be attached to the target in normal operations. Emulators are frequently used in embedded computer development. The emulator transmits signals and interacts like the original

device, but it has added instrument capabilities to capture detailed measurements. This technique can capture timing and triggering errors down to nanosecond resolution. In addition, it can capture handshake or protocol errors and detect abnormal transients or slow I/O faults.

3.5.7   Stimulus Signal Generation

For every signal type used, there is a signal generation need. Signals are generally categorized as analog, digital, or RF. Digital signals are based on binary logic state voltages, which are nominally 0 to 5 V for transistor-transistor logic (TTL). Analog signals can range from simple alternating current (AC) waves to waves with complex amplitude and frequency content, such as audio. RF signals are analog signals with high enough frequency to be transmitted effectively via antenna. Each signal type has its own signal modulation techniques and impedance characteristics.

SI can generate digital and analog signals as shown in Figure 5. RF signals are more difficult to measure and produce because of the extremely wide range of frequency and power levels. RF systems employ antenna technology to transmit across space where voltage and current measurements are meaningless.

3.5.8   Field-Programmable Gate Array Technology

In SI, the FPGA is an enabling capability because it provides the user a "sea" of available logic gates that can be programmed to synthesize the desired digital functions. Because these gates can be arranged to provide highly parallel pipeline processing, they can achieve very high performance. In contrast, a PC-microprocessor-controlled data-acquisition instrument performs many sequential functions and must perform memory fetches as well as support operating system overhead. As a result, microprocessor-controlled instruments usually have poor performance. The FPGA can provide signal-processing performance near that of a bench-top instrument.

Ultimately, CLEAR SI will support low to moderate frequency (baseband) analog signals, high-frequency (RF) analog signals, and digital signals. For RF, the frequency required for radio transmission is normally well beyond the internal data rates, and it is normal to use RF upconversion and RF downconversion.

3.5.9   Signal Routing

The signal router will route all signals going to and from the test target. It is a means in which signals will be aligned to pin outs of each target. This routing function is needed to accommodate large ORU connectors and circuit-card backplane connectors. Unless the target circuit is part of a standard backplane assembly, each target is expected to have unique pin-out arrangements that may mix input, output, analog and digital signals, and power in a single connector. In conventional automatic test systems, it is common to employ a customized set of test cables to attach the ORU to multiple instruments. A similar scheme can be employed for CLEAR, but there are crew time and stowage penalties for this approach.

For DIO connections, bidirectional buffers can change data direction on command, and data can be routed via software control. This is possible because digital signals conform to a very simple binary standard. Analog I/O, however, must deal with a wide range of analog signal types and voltages. There are practical limits to the range an analog device can accommodate. Therefore, it is important that the signal be routed to an analog input or output device that is designed for that type of signal. Therefore, routing analog input and output signals requires external routing capabilities.

Analog switches can be used to route a signal to the appropriate analog input or output. Digital timing and control logic can configure the analog front end and switching to reassign channels. The generic SI block diagram, shown in Figure 6, includes a signal routing connector adapter and a front signal routing matrix. Recent studies regarding plug-and-play satellites indicate that microelectromechanical systems (MEMS)-based reconfigurable manifolds may be best suited to flexible signal routing (Ref. 1).

Alternatively, FPGAs, with large-field open gates, can relocate or resynthesize an SI into a location that is more accessible for a given signal channel. This is equivalent to physically relocating and reattaching an instrument to different connections of the test circuit.
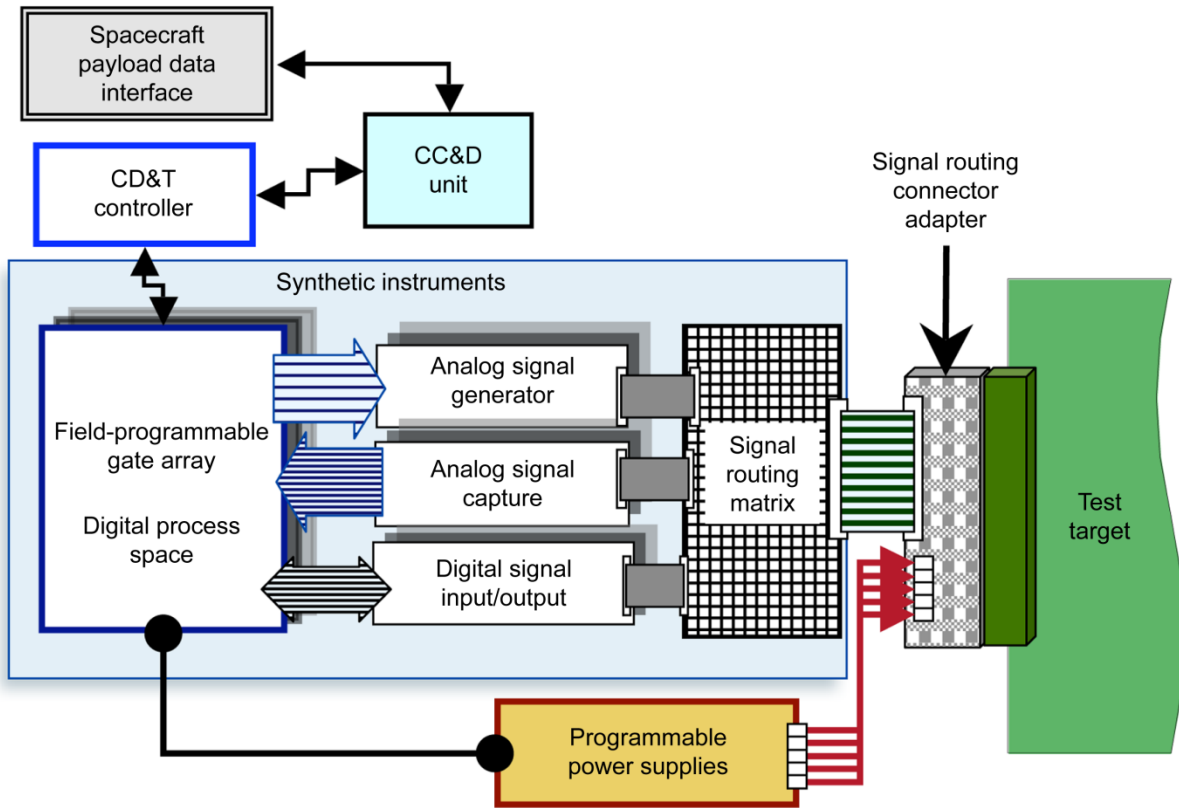

Figure 6.—Signals may be routed from various test targets by combining an internal signal routing matrix and an intermediate hardwired signal routing connector adapter. CD&T, CLEAR Diagnostics and Test; CC&D, CLEAR Control and Data.

4.0 CLEAR Synthetic Instrument Demonstration

4.1 Test Objectives

As described earlier, the SI concept is intended to provide a versatile instrument capability to support both diagnostics and functional testing while minimizing upmass and crew time. This demonstration is intended to reduce the concept to practice and provide a practical way of gauging the capabilities. The important and distinct capability is the ability to synthesize high-performance instruments on demand.

This SI demonstration is intended to demonstrate the following operational sequence:

- Create SI codes for two distinctly different applications
- Store the SI as data files
- Call up the first SI on demand
- Synthesize an instrument by porting the SI code to hardware
- Execute the SI in an actual test setup to inject the stimulus signal and acquire data
- Erase the initial SI
- Synthesize the second SI
- Execute the second SI in an actual test setup to inject a stimulus signal and acquire data

To minimize development cost and effort, researchers used an off-the-shelf instrument card that provided ease of use as well as FPGA technology. A National Instruments (NI) multifunction intelligent data acquisition card (RIO0, PCI–7831R,) described in References 2 and 3, and supporting software were employed. NI LabView software served as a development platform for creating the pseudocode that, in turn, was converted to FPGA code. The PCI–7831R card provided the FPGA device and the ability to import the SI code.

The outcome of the demonstrator effort is to validate SI principles in real hardware and assess the effectiveness of the approach in terms of

- Overall SI performance
- Capacity and performance of the FPGA device
- The level of effort required to create an SI application
- The ease of SI deployment and ease of use
- The turnaround time required to convert SI from one instrument to another

The demonstration will be followed by an analysis of the FPGA technology that considers—

- FPGA real estate consumed relative to real estate available
- The level of effort required in development of FPGA code
- The level of effort and resources required to compile and download code to the device
- The relative complexity and capability of the demonstrator relative to the flight system

4.2 Synthetic Instrument Test Hardware

Data acquisition (DAQ) systems consist of hardware and software that work fairly well together, providing a relatively powerful instrumentation control system. These systems offer software-programmable control of the input and output signals, permitting a target to be interfaced with a stimulus or data to be acquired and/or displayed. DAQs typically involve signal processing and analysis and may require signal conditioning to and from the target.

A user-defined Peripheral Component Interconnect (PCI) intelligent data acquisition board (RIO0, PCI–7831R, NI, see Figure 7) was used for this technology assessment. It is a multifunction data-acquisition board with onboard processing and flexibility over I/O timing and triggering. This DAQ can be used for a wide variety of development applications such as discrete and analog control, hardware-in-the-loop testing, digital emulation, bit-error-rate testing, and other applications requiring timing and control.
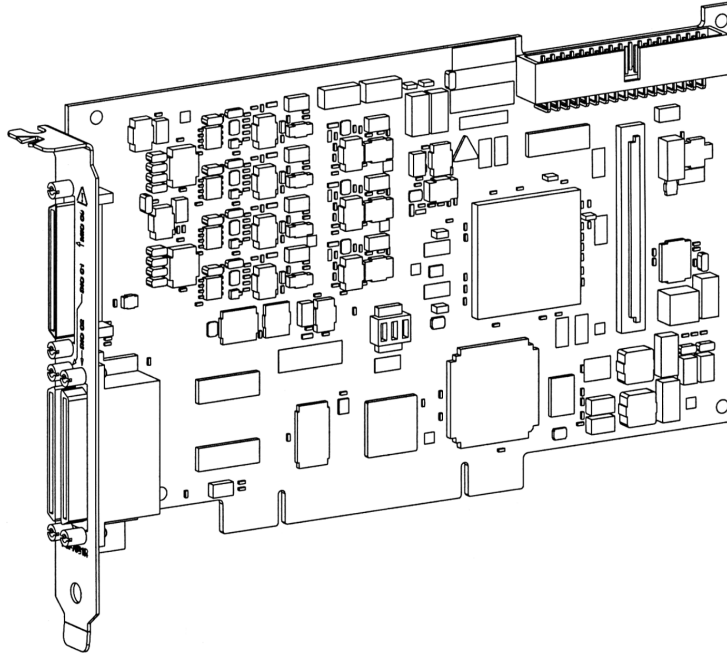
Figure 7.—National Instruments 7831R Peripheral Component
Interconnect (PCI) digital acquisition board (from Ref. 3).
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In place of the standard ASIC for controlling device functionality, this DAQ uses an FPGA-based system controller to make all onboard analog and DIOs configurable. The versatility of the FPGA makes this DAQ very flexible for application-specific designs giving users, through programming, direct and immediate control over all I/O signals.

Example applications follow:

- Data acquisition with flexible triggering and onboard processing
- High-speed analog and discrete control loops
- Pulse-width modulation (PWM) and encoder interfacing
- User-defined digital communication protocols
- Custom counters with up to 64-bit resolution
- Hardware-timed decisionmaking at 40 MHz

This DAQ has dedicated ADCs and DACs on every analog I/O channel, offering multirate sampling (up to 750 kHz) and individual channel triggering (up to 1 MHz). The DAQ also has onboard flash memory to support auto-loading and execution of compiled FPGA applications at power up.

4.3   Data Acquisition Specifications

The data acquisition specifications for CLEAR SIs follow:

- PCI computer bus backplane
- Xilinx, Virtex-II 1M gate reconfigurable I/O FPGA for parallel processing power
- Ninety-six DIO lines configurable as inputs, outputs, counters, or custom logic at rates up to 40 MHz
- Eight analog inputs (AIs), independent sampling rates up to 200 kHz, 16-bit resolution, ±10 V
- Eight analog outputs (AOs), independent update rates up to 1.0 MHz, 16-bit resolution, ±10 V
- User-defined triggering, timing, and onboard decisionmaking with 25-nsec resolution
- Direct memory access channels for high-speed data streaming

4.4 Data Acquisition Functionality

Functionally all AIs are sent directly to the ADC section where the signals are routed through the input MUX to instrumentation amplifiers and converted to digital signals by the ADCs (see Figure 8). The converted analog inputs and the other digital inputs (DIs) are sent directly to the user-configurable FPGA for user-defined processing. The FPGA provides bridging between the fixed I/O and bus interface and flexibility for custom I/O functions. Also, the DAQ can send and receive triggers through the real-time system integration (RTSI) bus to synchronize several measurement functions to a common triggering or timing event.

|	
ADC	analog-to-digital converter
AI	analog input
AIGND	analog input ground signal
AISENSE	analog input sense signal
DAC	digital-to-analog converter
DIO	digital input/output
FPGA	field-programmable gate array
I/O	input/output
MIO	multifunction input/output
MUX	multiplexer
NI	National Instruments
PCI	Peripheral Component Interconnect
PXI	PCI eXtensions for Instrumentation
RIO	reconfigurable input/output
RTSI	real-time system integration
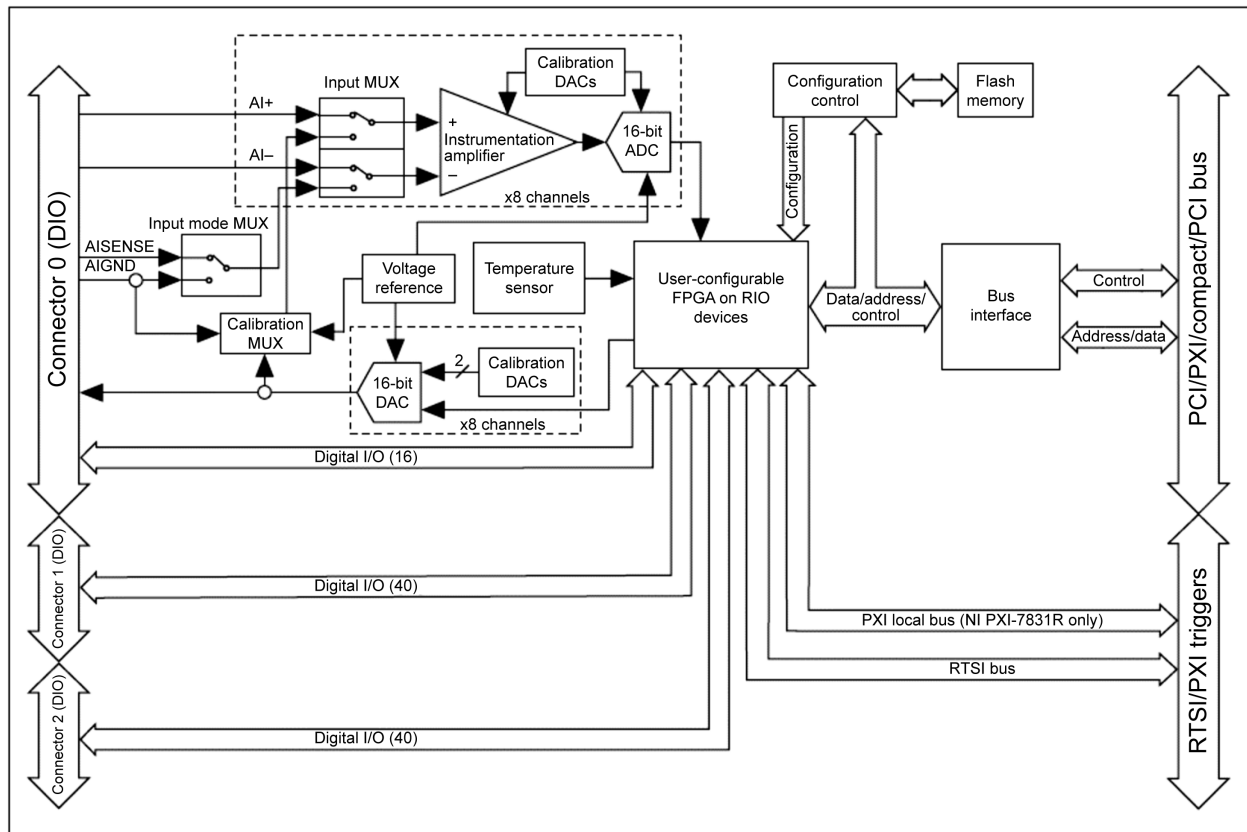
Figure 8.—NI 7831R block diagram from National Instruments user manual (Ref. 2). Copyright National Instruments; used with permission.

5.0   Synthetic Instrument Demonstrator Application Development

5.1   Synthetic Instrument Application

The concept of SI is based on the premise that test instrument algorithms reside in a reconfigurable environment and are supported by a diagnostics and test controller (DTC). In the flight system, the DTC manages multiple instruments—synthetic and conventional. The unit may support a local user workstation computer to allow the crew to control the instrument and monitor data. For the demonstration, a conventional PC serves as both the DTC and the crew workstation. Because the demonstration unit employs a PC backplane bus, the board is dependent on the PC for its power and data management. The actual flight system will likely be a stand-alone unit that uses a network interface. The flight version of the SI unit will have greater independence.

Each of the demonstration SIs was composed of PC-based LabView VI software residing in the PC and FPGA code residing in the SI board. In the actual flight application, the user interface portion of the VI software would be located in the crew workstation or in the ground-based support center. The FPGA code, known as the hardware description language (HDL), defines how the internal logics gates are connected inside the device, and that, in turn, defines the device's logical functions. HDL code is developed and compiled as a bit file. This compiled HDL code is burned into the FPGA device, and the logical functions become permanent. With software now converted to hardware, the FPGA device can operate with the high-speed performance and deterministic behavior of a conventional hardware logic design. The primary difference is that the FPGA logic can be erased and new code burned in when needed.

To keep the size of the SI equipment compact and performance high, the user control and display functions are handled by the software VI that resides in the lower speed PC host. The windows-based VI software can be used to set parameters for the SI before a test is executed. The VI also provides the user with a "front panel" where displayed data are drawn from data files; and, thus, VI has processing delays. Therefore, the data viewed by the user are not truly real time. To preserve real-time responsiveness to the test circuit, the SI unit responds to user inputs as a low priority until its measurements are complete. In this way, lower priority front panel updates have no affect on hardware execution rates, leaving the hardware to perform in a deterministic manner.

5.2   Synthetic Instrument Library Function

Consistent with the concept of an SI application library, the host computer can be used to store a library of precoded SIs. Among other things, the SI library is intended to contain reusable control codes and setup parameters. Much like an industrial computer numerical control (CNC) library, it will contain the programming code (SI applications) for diagnostic operations. This test program simulated part of the library's function of storing the instrument applications, which are called and loaded on an as-needed basis.

5.3   Synthetic Instrument Verification Emulator

An emulator is a software simulation of a hardware target that runs on the development computer. The emulation feature is an effective tool for SI application developers to test and verify instrumentation products before they are compiled, downloaded, and run on the hardware target. This feature allows developers to use standard debugging techniques like breakpoints, single-stepping, and probes, but not functions like timing.

5.4   Analog Synthetic Instrument

For an analog demonstration of an SI, a single-output, single-input analog generator and display was developed. The signal generation side of this instrument is an AC signal generator, producing a sine wave whose frequency ranges between 1 Hz to 50 kHz. The input of this instrument was developed as a graphical interface and acquires data at a sample rate up to 200 kilosamples per second. These two I/O channels operate independently and simultaneously.
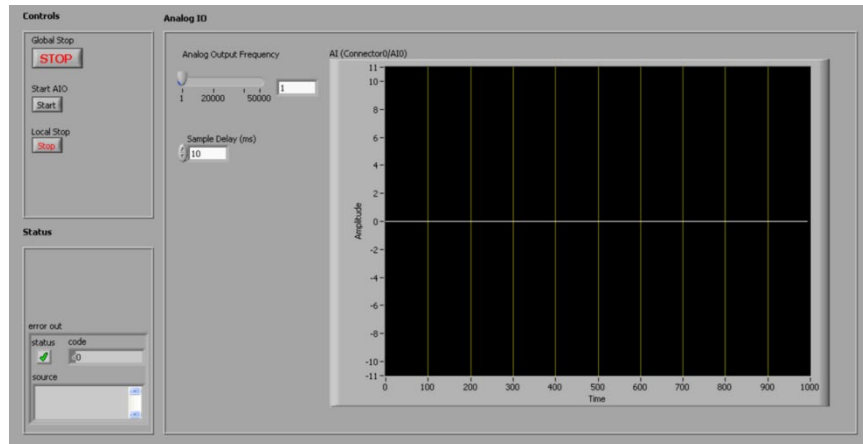
Figure 9.—Analog demonstration control and display panel. AI, analog input.

The output signal and input sample rate controls reside on the host computer and are presented within a software control and display panel (Figure 9). This panel emulates the functions performed by the front panel of a conventional instrument. The host program is tasked with providing a means to start and stop the signal generation and data output, while providing an interface for the user to control, input the sample rate, and graphically display the sampled data.

The hardware portion of the application was written to be interactive with the host computer and vice versa; however, the host program and the hardware parts of the application operate independently of each other. The two parts of the application interact through the use of a buffer where data are written to and read from. Although this program is basic in its functionality, it demonstrates the basic capabilities of an analog SI. In effect, the SI has synthesized an analog signal generator and an analog oscilloscope. The instrument can simultaneously collect and generate analog data while being reconfigurable on the fly.

The next step in developing this analog instrument could be to implement a more complicated analog signal generator—possibly by adding arbitrary signal-generation capabilities, additional analog input and output channels, or complex signal analysis for the analog input channels. Any and all of these capabilities could be added while keeping the instrument easily reconfigurable. One could further enhance the analog input capabilities of the instrument by adding a more advanced analog-to-digital/digital-to-analog (AD/DA) front end to the board. This could allow for faster sampling rates or higher resolution data.

5.5   Digital Synthetic Instrument

For the SI assessment of a digital SI, a combination of a single 8-bit generator and a single 8-bit DAQ was created. The DIO rate is variable; however, it is only configurable at startup through the host program front-panel control window (Figure 10). The host program is tasked with providing a means to start and stop the data output and data input, and with providing an interface for the user to control the data rate, set the digital data to be output, and graphically display the sampled data (Figure 11). The target program simultaneously outputs and inputs the digital data. The interaction between the host and target is via an interrupt set by the target program after each I/O operation. The host program reads and clears the interrupt.

Although this program is basic in its functionality, it demonstrates the basic capabilities of a digital SI. The instrument can simultaneously collect and generate digital signals. In effect, this digital SI application emulates a digital signal generator and an oscilloscope or, in combination, could be considered a logic analyzer. The next step in developing this digital instrument could be to increase the number of DIO channels used. There are a total of 96 digital channels that can be used for DIO. Expanding the number of digital channels in this example would be trivial. Although the two examples that were generated were exclusively analog or digital, there is nothing to preclude the creation of a mixed-signal SI.

Figure 10.—Digital demonstration control panel.
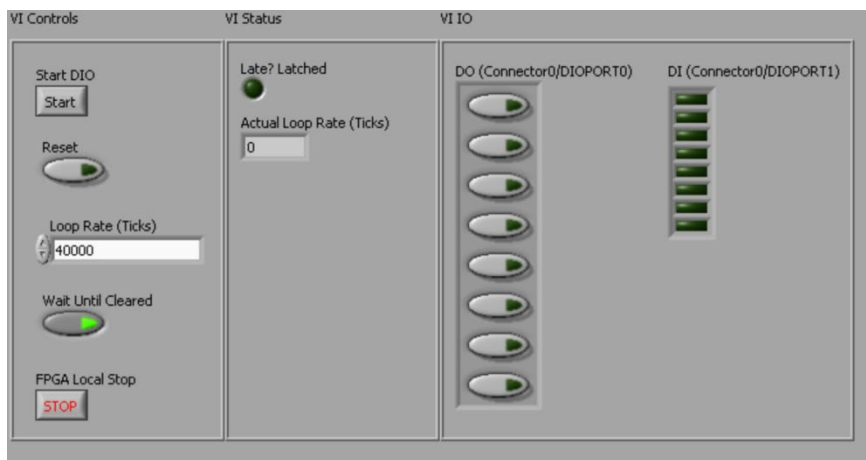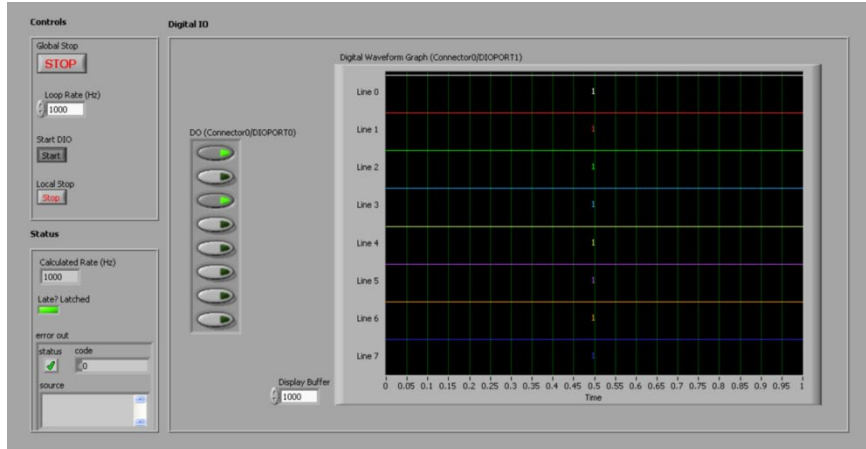
DI   digital input
DIO digital input/output
DO digital output
IO   input/output
VI   virtual instrument

Figure 11.—Digital demonstration graphics display panel.

DIO digital input/output
DO digital output
IO   input/output

6.0   Field-Programmable Gate Array Architecture

6.1   Virtex-II Overview

This section defines some basic concepts and terms that will be needed in interpreting the compilation summary. The primary building block of the FPGA is the configurable logic block (CLB) (Figure 12). The input/output blocks (IOBs) serve as the interface between the chip package pins and the CLBs. The random access memory (RAM) blocks serve as the local data storage. Digital clock managers (DCMs) control the timing and synchronization within the FPGA. These features are described in more detail in Virtex-II data sheets (Refs. 4 and 5).

6.2   Configurable Logic Blocks

CLB elements contain four interconnected slices, shown in Figure 13, and are the main logic and register resource for building logic designs. Each slice, in turn, is composed of function generators, a storage element, arithmetic logic gates, multiplexers, and various logic elements. As shown in Figure 13, each slice is tied to input and output multiplexers that act like a matrix of switches that connnect any CLB to other CLBs, to IOBs, or to RAM.

Depending on the desired function, the function generator can be set up to act as a four-input look-up table (LUT), as a 16-bit shift register, or as a 16-bit memory register. In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches. These elements are used to provide logic, arithmetic, read-only-memory (ROM) and RAM functions, and registers.
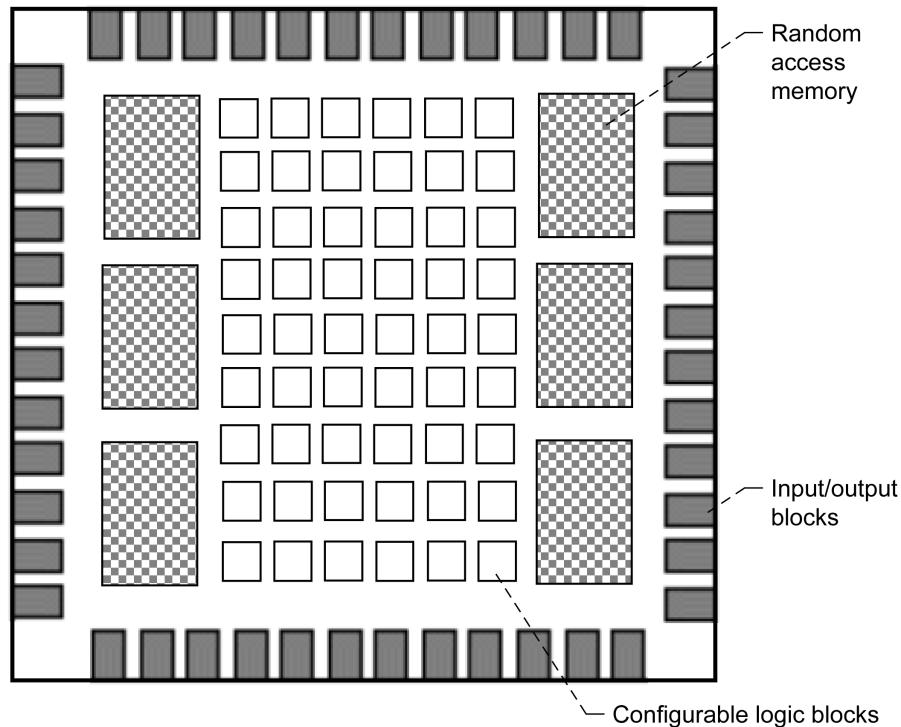

Figure 12.—This illustrates a highly simplified architecture of the Xilinx field-programmable gate array.
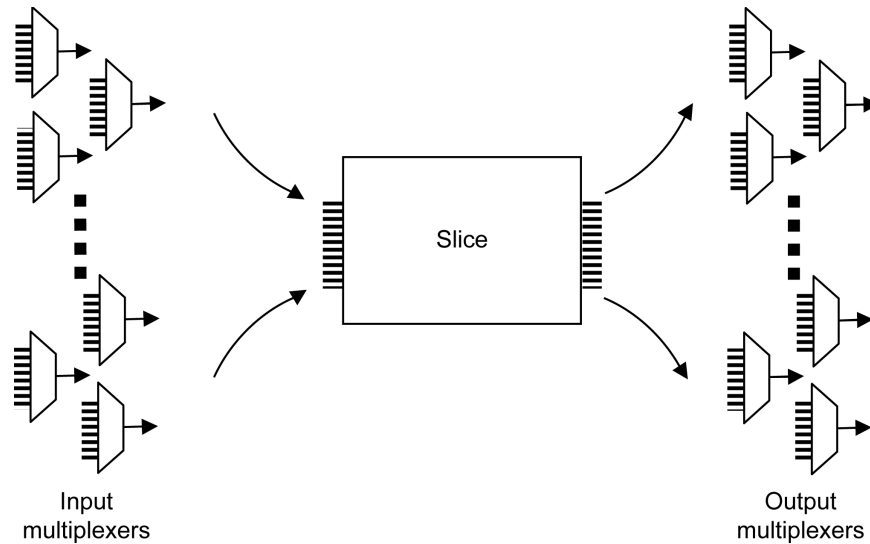
Figure 13.—Configurable logic blocks are composed of "slices" that contain logic
elements with an array of input and output multiplexers that serves as a
switch matrix.

6.3   Look-Up Tables

The concept of a LUT is to replace the function of normal fixed logic gates with a configurable device. Conventional combinatorial logic arranges logic gates that will always yield a specific output for a given combination of inputs. To change the combinatorial logic, a designer must add, remove, or substitute different logic gates. By using a LUT, the designer can set up an arbitrary output for a given input simply by loading a desired pattern in the LUT register. This allows the LUT to emulate the same capabilities that equivalent logic gates provide. This includes emulating the functions of shift registers, simple math functions, frequency dividers, delay lines, state inverters, and other functions.

6.4   Input/Output Blocks

IOBs are functional blocks that handle internal and external signaling. They are located at the perimeter of the device. IOBs provide the means to connect components internal to the FPGA to circuitry external to the device. IOBs can improve performance by increasing the number of routing paths. Each IOB contains storage registers and can support edge triggering or level sensing. Input signals are routed directly to internal logic or through the double-data-rate (DDR) input registers. The output signals can be routed directly from internal logic or through a three-state latch.

7.0   Synthetic Instrument Compilation

Developers of CLEAR SI applications will use a software design environment for code creation. Once finished, the higher level application code will be interpreted into code suitable for the target, in this case, bit files. Along with this process of compiling, the software design tools will report some basic findings concerning design and resource utilization through the use of a device utilizations summary report.

To simplify the inherently complex process of FPGA application design, the tool lets the user "bound" the design by setting the design constraints. The designer simply establishes the constraints to meet the goals of the application. Constraints are interpreted by the implementation tool, which in turn, maps the design, pin assignments, logic, and timing guidelines. This avoids the tedious process of connecting a huge number of individual logic gates and registers.

The design constraints are the primary tool the user has to convert an SI model into hardware. This approach is desirable for user simplicity, provided that the implementations do not become constricted by available FPGA resources. It is, however, undesirable if the user requires tight control over resource allocations. As in many software tools, the details on how the implementation tools allocate resources are hidden from the user. For SI applications, where a single FPGA may be programmed to accommodate multiple instruments, the lack of insight into how resources are allocated becomes apparent when reading compilation summary reports.

The summaries, shown in Table I and Table II, are excerpts from the compilation report. It is difficult to use resource utilization statistics to correlate the perceived complexity of the SI. Part of the problem lies with the way the tool initially seeks to optimize performance rather than minimize resource consumption. Most FPGA applications are permanent and the need to change the design on demand or reserve space for additional applications is abnormal. Therefore, the tool will tend to create a high-performance design that has a relatively inefficient use of capacity. As a result, the capacity consumed will appear to be high even for apparently simple applications. The user will interpret the results as indicating that little capacity remains. This makes it confusing for a user who is trying to estimate what other instruments the FPGA can accommodate on the fly.

In summary, for SI development, the user will need to be trained in greater depth and employ more complex tools in SI design. Alternatively, new design and compilation tools may be needed that are specially optimized for SI applications.

TABLE I.—DIGITAL INSTRUMENT
DEVICE SUMMARY

Device	Number used	Total	Percent
BUFGMUXs[a]	2	16	12
External IOBs[b]	216	324	66
Slices	709	5120	13

	Clock rate, MHz
Onboard base clock	40
Requested rate[c]	40.408938
Theoretical maximum	77.839184

[a]BUFGMUX, global clock buffer multiplexer.
[b]IOB, input/output block.
[c]Requested rates are adjusted for jitter and accuracy.

TABLE II.—ANALOG INSTRUMENT
DEVICE SUMMARY

Device	Number used	Total	Percent
BUFGMUX[a]	2	16	12
External IOB[b]	217	324	66
RAMB16[c]	2	40	5
Slice	588	5120	11

	Clock rate, MHz
Onboard base clock	40
Requested rate[d]	40.408938
Theoretical maximum	136.109977

[a]BUFGMUX, global clock buffer multiplexer.
[b]IOB, input/output block.
[c]RAMB16, block random access memory library primitive.
[d]Requested rates are adjusted for jitter and accuracy.

8.0   Conclusions

In general, the role of synthetic instruments (SIs) for Component-Level Electronic-Assembly Repair (CLEAR) is to provide an external instrument capability for performing lower-level diagnostics and functional tests beyond the built-in-test capabilities of most spacecraft electronics. Built-in diagnostics can report faults, but the reported symptoms may have multiple potential root causes that cannot be isolated. External diagnostics is essential for exposing a fundamental root cause so that engineers can devise a corrective action. To avoid the mass, volume, and inherent complexity of a full set of lab equipment, the CLEAR SI strategy exploits a highly reconfigurable instrumentation architecture that can synthesize a solution to meet a specific need. SI technology within a teleoperations framework is also intended to relieve the technical burden and training on flight crews. This lab demonstration was intended to assess the state of the art and measure how effective existing programmable real-time data-acquisition systems are in achieving the overall SI goals.

The project employed a commercial-off-the-shelf (COTS) data acquisition board with a built in FPGA. Two distinct SI designs including an analog instrument and a digital instrument were created. Because of funding constraints, these were limited to simple instruments that only took a few weeks to develop. These were developed to assess the practicality of the SI development process and to determine if loading an instrument and subsequently erasing and loading a new instrument in rapid succession was feasible. The experiment showed that FPGA technology makes the SI concept viable.

Overall, the benefit of the National Instruments (NI) development package was its ease of use, which allowed someone with previous NI LabView experience, but no direct experience with FPGA programming tools, to successfully create a synthetic instrument. The effort is not linearly proportional to the instrument complexity or number of channels. Certain "boilerplate" or commonly used user and data handling overhead functions are needed regardless of the apparent complexity of the measurement. Download time and compile time increases with code complexity. For this demonstration, the compile time for these instruments only took 10 to 15 min. Therefore, once instruments have been developed, the turnaround time of reloading an application into hardware will be only a matter of minutes. The main constraint on SI does not appear to be the digital FPGA device. Rather, SI is restricted by the analog portion of the instrument where the hardware flexibility is limited.

The project attempted to gauge the low-level (integrated-circuit level) complexity and performance of the FPGA device. However, as a high-level software development tool, many of the details are hidden from the developer. Combined with the "boilerplate" features required for the user interfaces and the data handling overhead, it is quite difficult to gauge how much capacity is still available on the FPGA. That is, an instrument with twice as many channels does not consume twice as much FPGA capacity. At this point, the project cannot predict how much hardware and software will be needed to meet all the potential SI applications.

It must be left to future work to characterize the SI development process and to identify specific parameters that can be used as capacity and performance measurements. A likely next step is to develop and characterize a series of SIs of increasing complexity. The FPGA utilization reports provided by the NI tools were inadequately described to support a rigorous analysis. The NI-Xilinx tools tend to allocate resources with an emphasis on performance at the expense of capacity. The software does not optimize capacity until the device's capacity limits are reached. Development of actual flight SI units will require more sophisticated development tools with greater control over FPGA resources. These tools will make it easier for SI designers to measure available capacity and to optimize the number of SI units that a single FPGA device can support. FPGA technology is widely used and continues to advance; therefore, CLEAR will not need to invest substantially in this aspect of SI.

FPGA technology is required, but not sufficient, to meet the objectives of the CLEAR SI strategy. Creating analog circuits that can easily accommodate the wide range of bandwidth, dynamic range, and channel count is a considerable challenge. SI will require significant investment in resolving the limitations on the analog front-end portion of SI.

Future work should include—

- Improved SI programming tools to ensure system flexibility and to maximize the combination of performance and digital resource utilization
- Development of a highly flexible analog front end that expands bandwidth, dynamic range, and channel count
- Development of signal routing techniques to further extend flexibility particularly as a means of accommodating the wide variety of connector configurations

Appendix.—Acronyms and Abbreviations

AC	alternating current
A/D	analog to digital
ADC	analog-to-digital converter, conversion
AD/DA	analog-to-digital/digital-to-analog
AI	analog input
AIGND	analog input ground signal
AISENSE	analog input sense signal
AO	analog output
ASIC	application-specific integrated circuit
ATE	automated test equipment
ATU	Audio Terminal Unit
BUFGMUX	global clock buffer multiplexer
CC&D	CLEAR Control and Data
CD&T	CLEAR Diagnostics and Test
CLB	configurable logic block
CLEAR	Component-Level Electronic-Assembly Repair
CNC	computer numerical control
COTS	commercial off the shelf
CPU	central processing unit
CRE–1	Component Repair Experiment 1
CVIU	common video interface unit
DAC	digital-to-analog converter, conversion
DAQ	data acquisition
DCM	digital clock manager
DDR	double-data-rate multiplexer
De-MUX	demultiplexer
DI	digital input
DIO	digital input/output
DO	digital output
DTC	diagnostics and test controller
ETDP	Constellation Program Exploration Technology Development Program
FPGA	field-programmable gate array
HDL	hardware description language
HRM	high-rate multiplexer
IF	intermediate frequency
IO	input/output
I/O	input/output
IOB	input/output block
ISS	International Space Station
LUT	look-up table

MDM	Multiplexer/Demultiplexer Module
MEMS	microelectromechanical systems
MIO	multifunction input/output
MUX	multiplexer
NI	National Instruments
ORU	orbital replaceable unit
PC	personal computer
PCB	printed circuit board
PCI	Peripheral Component Interconnect
PWM	pulse-width modulation
PXI	PCI eXensions for Instrumentation
RAM	random access memory
RAMB16	block random access memory primitive
RF	radiofrequency
RIO	reconfigurable input/output
ROM	read-only memory
RPCM	Remote Power Controller Module
RTSI	real-time system integration
SGTRC	Space-to-Ground Transmitter Receiver Controller
SI	synthetic instrument
SoRGE	Soldering in Reduced Gravity Experiment
SRR	System Requirements Review
SRU	shop replaceable unit
TEST	Teleoperations Engineering Support Team
TTGbE	time-triggered gigabit Ethernet
TTL	transistor-transistor logic
VBSP	video baseband signal processor
VI	virtual instrument

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13. SUPPLEMENTARY NOTES

14. ABSTRACT The role of synthetic instruments (SIs) for Component-Level Electronic-Assembly Repair (CLEAR) is to provide an external lower-level diagnostic and functional test capability beyond the built-in-test capabilities of spacecraft electronics. Built-in diagnostics can report faults and symptoms, but isolating the root cause and performing corrective action requires specialized instruments. Often a fault can be revealed by "emulating" the operation of external hardware. This implies complex hardware that is too massive to be accommodated in spacecraft. The SI strategy is aimed at minimizing complexity and mass by employing highly reconfigurable instruments that perform diagnostics and emulate external functions. In effect, SI can "synthesize' an instrument on demand. The SI architecture section of this document summarizes the result of a recent program diagnostic and test needs assessment based on the International Space Station. The SI architecture addresses operational issues such as minimizing crew time and crew skill level, and the SI data transactions between the crew and supporting ground engineering searching for the root cause and formulating corrective actions. SI technology is described within a teleoperations framework. The remaining sections describe a lab demonstration intended to show that a single SI circuit could synthesize an instrument in hardware and subsequently clear the hardware and synthesize a completely different instrument on demand. An analysis of the capabilities and limitations of commercially available SI hardware and programming tools is included. Future work in SI technology is also described.

15. SUBJECT TERMS Space operations; Space logistics

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