Avionics For A Small Satellite

Dr. Larry Abbott, David Jochim, Robert Shuler
NASA-JSC, 2101 NASA Road 1, Houston, Texas, 77058
281-483-8593, labbott@ems.jsc.nasa.gov

Abstract – This paper discusses a small, seven and a half (7.5) inch diameter, satellite that NASA-JSC is developing as a technology demonstrator for an astronaut assistant free flyer. The Free Flyer is designed to off load flight crew work load by performing inspections of the exterior of Space Shuttle or International Space Station. The Free Flyer is designed to be operated by the flight crew thereby reducing the number of Extra Vehicle Activities (EVA) or by an astronaut on the ground further reducing crew work load. The paper focuses on the design constraint of a small satelite and the technology approach used to achieve the set of high performance requirements specified for the Free Flyer. Particular attention is paid to the processor card as it is the heart and system integration point of the Free Flyer.

INTRODUCTION

In 199_ NASA flight tested a free flyer called "Sprint". Sprint was thirteen (13) inches in diameter and used a 1 MIPS processor with 32Kbytes of memory to perform simplified, integer flight control laws. Sprint also provided a propulsion system, dual analog video and uplink/downlink capability.

It is an irony that as technology improves, system requirements increase just enough to offset the gain in technology. The technology available in 2000 allows a smaller Sprint to be easily developed, but the requirements for the second generation of the Astronaut assistant Free Flyer far exceed those of Sprint. Not only must the size be reduced to a seven and a half inch sphere, but Sprint's simplified integer control laws are being replaced with sophisticated, floating point control laws, position hold is to be added, and digital GPS filtering is being added to the processor load. Sprint's two analog cameras are being replaced with three digital camera's and accompanying video compression capability, Sprint's propulsion system is being replaced with a harmonized propulsion system, and Sprint batteries are being replaced with Li-ion technology. All the above technologies rely, to varying degrees, on the power of the new processor.

Design Constraints

Although the requirements for the free flyer have grown, the physics of space flight and the volume of the seven inch sphere dictate that the power, mass, and of course volume can not grow. In fact it is preferable that power and mass be reduced.

TABLE 1. Comparison of Power, Weight, & Volume

Constraints	Sprint	Free flyer
Power	20 watts	18.21 watts
Weight	35.5 lbm	10.38 lbm
Volume	1150 in^3	65.95 in^3

There are several major design constraints that drive the internal configuration and packaging of the Free Flyer vehicle. In particular, the placement and configuration of the avionics are driven by the size, shape, and thermal characteristics of the vehicle shell.

The spherical vehicle geometry required for a "safe" vehicle impacts every facet of subsystem design. First of all, the spherical packaging volume poses strict dimensional and geometric constraints on individual components. In addition, the Free Flyer packaging volume has been reduced over 80% from the Sprint vehicle while functional capability has been significantly increased. This large decrease in internal volume and surface area for heat rejection naturally leads to a vehicle with a much higher packaging efficiency and to concerns about local and bulk thermal stability.

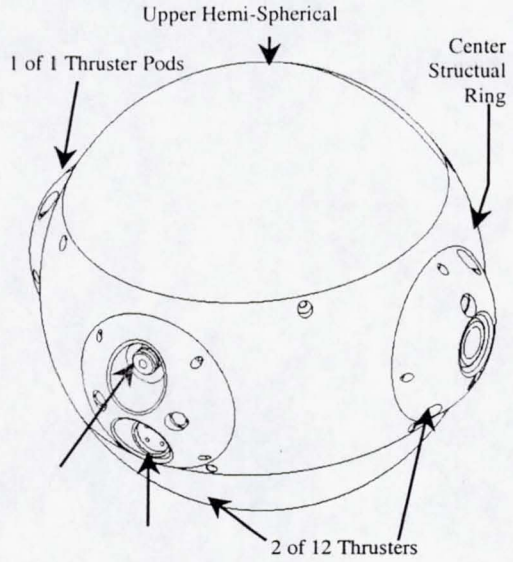

Figure 1: External View of Free Flyer (Left) and cutaway view (Right)

Preventing individual components from exceeding their specified temperature limits is a major packaging challenge for this vehicle. The vehicle's high power and small size, coupled with its operational thermal environment, make it prone to localized overheating. Current vehicle architecture does not include active cooling for thermal conditioning. Therefore, it is extremely important that the packaging account for heat flow through and away from the vehicle. Preliminary analysis has shown that steady state bulk average temperatures should not exceed component operational limits even in the worst-case environments. The bulk thermal temperature is highly dependent on operational scenario and environment, both of which can be readily altered if temperatures become marginal. Therefore, the temperature will be monitored. Analysis and Sprint flight experience shows that localized temperatures can exceed the bulk average temperature by 40 degrees Fahrenheit. The design locates major heat sources away from the avionics and close to the outer radiating surfaces.

Getting heat away from the boards and to the vehicle radiating surfaces is the second issue to be addressed. The avionics utilizes high efficiency DC/DC switching converter to reduce power consumption and waste heat. The converters are mounted on the top side of the processor board where thermal transfer foam and direct contact to a metallic plate transfers heat way from the converters and the processor board directly to the outer shell. The processor board transfers additional heat to a thermal strip on the outer edge of the borard which also has a thermal interface to the outer structure. Proximity to other radiation heat sources is also a concern. Therefore distributing the heat sources around the ball and as far from each other becomes important. Adjacent heat sources include the batteries, a GPS receiver, and a video compression card. Each of these components is similarly provided with a direct heat path to the outer shell and should not significantly contribute to heating of the avionics.

Given the fact that the Free Flyer has a higher packing density, accessibility is a significant problem. To address accessibility, the primary structure and internal configuration has been simplified. The power and propulsion systems occupy the center structural ring, communications and GNC occupy the top hemisphere, and avionics occupies the lower hemisphere. Each of these systems is accessible independently from the rest simply by removing one of the hemispheres.

Unfortunately, the requirement that the heat generating components be distributed for thermal reasons makes the physical connectivity to the processor difficult. Connection between subsystems will be managed by routing wire-runs from the subsystems into and along the perimeter of the central ring and then into the processor board. Proper management of these numerous wire-runs will assure desired accessibility.

Technology

Putting all the performance required for the Free Flyer into a seven and a half (7.5) inch sphere requires state-of-the-art (SOA) technology, but even given SOA technology. Over the last twenty years, improving technology has usually meant designing more performance into electronics components, which in turn packs more performance into the same size, weight and power package. When memory density quadruples the package is not cut to one quarter size; rather the package size remains the same and the amount of memory is quadrupled. As a result, processors get faster and memories get denser, but the size of the packages stays roughly the same. Therefore it has been difficult to control volume and mass with silicon technology alone. This is particularly true for minimal systems like the Free Flyer, since the opportunity for combining 4 or even 2 items into one item doesn't exist, i.e. combining four banks of memory into 1 higher density bank.

The integrated circuit packaging technology played the largest role in reducing the size and weight of the Free Flyer's avionics. On the Free Flyer, most of the weight and volume gains came from much denser packing of the integrated circuit boards and the almost exclusive use of Surface Mount Technology (SMT) to allow both sides of the circuit board to be populated.

Improved chip design does reduce the power consumption of chips through the increased use of low power technologies such as CMOS and reduced power consumption sleep modes. In the case of the Free Flyer versus Sprint, the improved processor technology produces a high performance PowerPC which is projected to be awake less than 10% of the time. As a result of spending 90% of the time spent in sleep mode, the Free Flyer processor compares favorably with the Sprint's 1 MIPS processor in terms of power consumption while still producing nearly fifty (50) MIPS. The SDRAM memory, while much larger in terms of bits than Sprint's SRAM, consumes much less power on a bit for bit basis. Due to these improvements in processor and memory technology the Free Flyer's performance far exceeds Sprint's performance while its avionics is roughly the same size and consumes roughly the same power.

ARCHITECTURE

The Free Flyer's avionics architecture went through a series of evolutionary stages to meet its requirements. In the first stage NASA sought not only to retain as much of its investment in the UMC [1,2] as possible, but to retain as well, the modularity and re-use philosophies built into UMC through its use of the PC-104 bus standard. In its initial stage the architecture was envisioned as a stripped down version of the PC-104 used on the UMC. The adaptability and universality of the standard PCI and ISA buses were sacrificed to reduce power and space. Instead, the processor's Front Side Bus (FSB) was extended for use as a local bus interface to external peripheral functions. The size of the stackable cards reduced and the size of the corresponding connectors were reduced. However, early in the design it became apparent that the operational requirements would not allow everything to fit onto neat little rectangular cards organized in an orderly stack. The stack was rejected because of the needs of the various systems, such as propulsion, GPS and Uplink/Downlink antennas, and video, to be located in specific locations within the vehicle.

As the operational requirements forced changes to the architectural concept, at first the extended FSB was supplemented with serial buses to those parts of the architecture that could not be located adjacent to the Processor Card. In the next stage, the use of the extended FSB for external interfaces to the Processor Card was abandoned altogether. Instead, all peripherals, adjacent or not, connect to the processor card via serial buses. In the final stage, modular, re-usable rectangular cards were abandoned, and as much of the adjacent avionics as possible was integrated onto a single, circular processor card for overall packaging efficiency and thermal transfer reasons. The remaining avionics is interfaced to the processor cards through serial buses. The use of the extended FSB as an external interface is gone, and now the processor's FSB connects directly and exclusively to the FPGA. The FPGA in turns implements the functionality of the memory controller, interrupt controller, timers, serial ports, and memory and thruster interfaces.

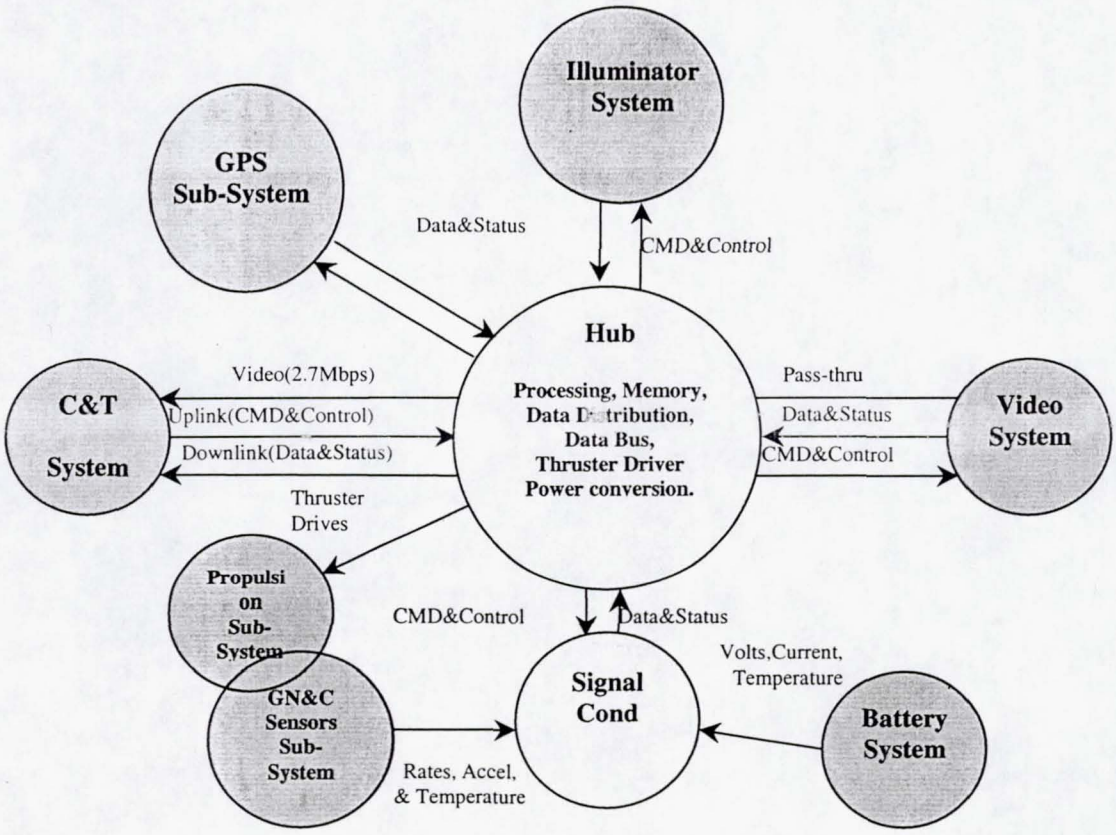

Figure 2: STAR architecture for free flyer

On many levels the architecture has evolved into a star architecture, with the processor card is at the hub of the new architecture. The processor, memory, and serial buses are on the hub, thus making the architecture a star in terms of data, and command and control. The processor card is also a star in terms of vehicle secondary power because all of the vehicle's DC/DC conversion is also in the hub.

The Processor

The need to minimize power consumption while retaining a high performance, floating point capability demands a processor with a high MIPS to watt ratio and the ability to scale the MIPS and therefore the power to the problem at hand. The PowerPC provides this capability. The predecessor to the Free Flyer's processor, the UMC processor card, has a 166 MIPS 603e, 8 Mbytes Flash, 32 Mbytes SDRAM, PCI bus, and ISA bus. It consumes 4 watts at 100% capability and 1.3 watts when it is in sleep mode. The removal of the ISA and PCI buses and the associated bridge from will offset the increased power consumption from the upgrade to the PowerPC 750. The incorporation of the rest of UMC's functionality into the processor board's FPGA (with the except of the clock generation and reset circuitry) is expected to actually reduce the power consumption below UMC levels. At 3 times the MIPS, the PowerPC 750 will be in sleep mode much more than would have been the case for a 603e based design further reducing the power consumption. In addition to the power consumption advantages of the PowerPC, radiation hardened versions of the 603e and 750 are nearing availability.

The design approach for the project requires flexibility and developer friendliness to be designed into the engineering prototype. Later, in the port of the fully developed engineering prototype to the flight article, achieving radiation tolerance and lowest power will become more important. At that time the reprogrammable FPGA used for the engineering prototype will replaced with a suitable low power, radiation tolerant, fusible link FPGA that will become available in the summer of 2001.

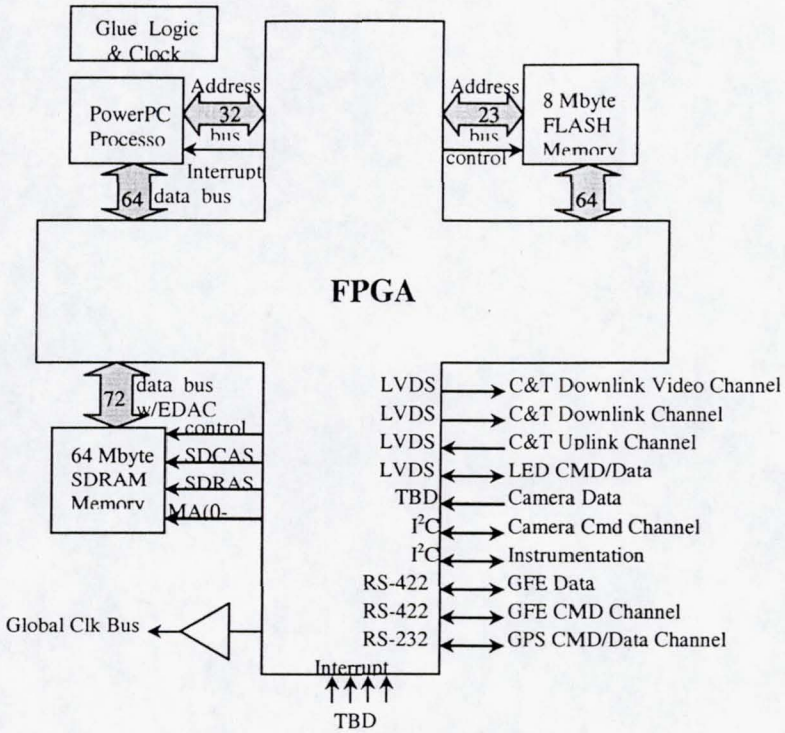

Figure 4: The processor

FPGA

The FPGA used on the free flyer is in fact quite large, but it is input/output (I/O) bound; not logic bound. It must provide the 72 bit wide SDRAM controller function, the Hamming code EDAC function, the interrupt controller function, the Flash memory interface, LVDS serial ports, legacy serial ports (for ground support equipment and integrated circuits with existing interfaces), thruster driver logic, timers, and counters. Unique among these functions is the thruster driver logic which fires the thruster continuously for 4 msec. In order to reduce power consumption any thruster firing beyond initial 4 msec is performed with a 25% duty cycle, 1 kHz square wave. A watchdog time (WDT) is provided to protect against continual, non commanded firings. Finally the harmonized thruster controls require precise and variable firing periods over a large range of firing durations. Initially this requirement as expressed as a need for a 4 msec minor cycle that would allow the thruster firing to be extended or terminate every 4 msec. This would allow indefinite thruster firing with 4 msec resolution, albeit with an unacceptable overhead placed on the processor. Once the control problem was fully understood by all disciplines, the thruster driver was modified to allow variable firing times of 2 to 100 msec in 1 msec steps. Not only did this solution offer finer firing duration resolution, but the minor cycle was relaxed to 40 msec. This relaxedminor cycle allows the processor to spend more time in the sleep mode which in turn reduces the over all power consumption of the processor.

The thrusters require at least 20 volts for proper operation and the batteries require 29.4 volts at the beginning of their discharge cycle to meet the 20 volts requirement at the end of a four hour mission. Initially MOSIS technology was to be used to reduce the space taken by the twelve, high side thruster drivers, however the 29.4 volts battery requirements exceeds the MOSFET breakdown voltage available

using stardard MOSIS processing. For a time the thruster driver design reverted to a discrete component implementation. Later, it was realized that the thruster drivers could meet the 29.4 volt requirement with the standard MOSIS processing technology if the drivers were fabricated with MOSFETs arranged in

series. In addition, the MOSIS drivers are to be implemented with a NASA developed radiation tolerant design that will allow radiation tolerant devices to be fabricated with the standard MOSIS processing technology. To date the technology has been tested with 200 Mev Protons and the test chips have passed exposure of 19 krads and 51 krads. During the testing there have been no observed latch ups and no observed SEUs.

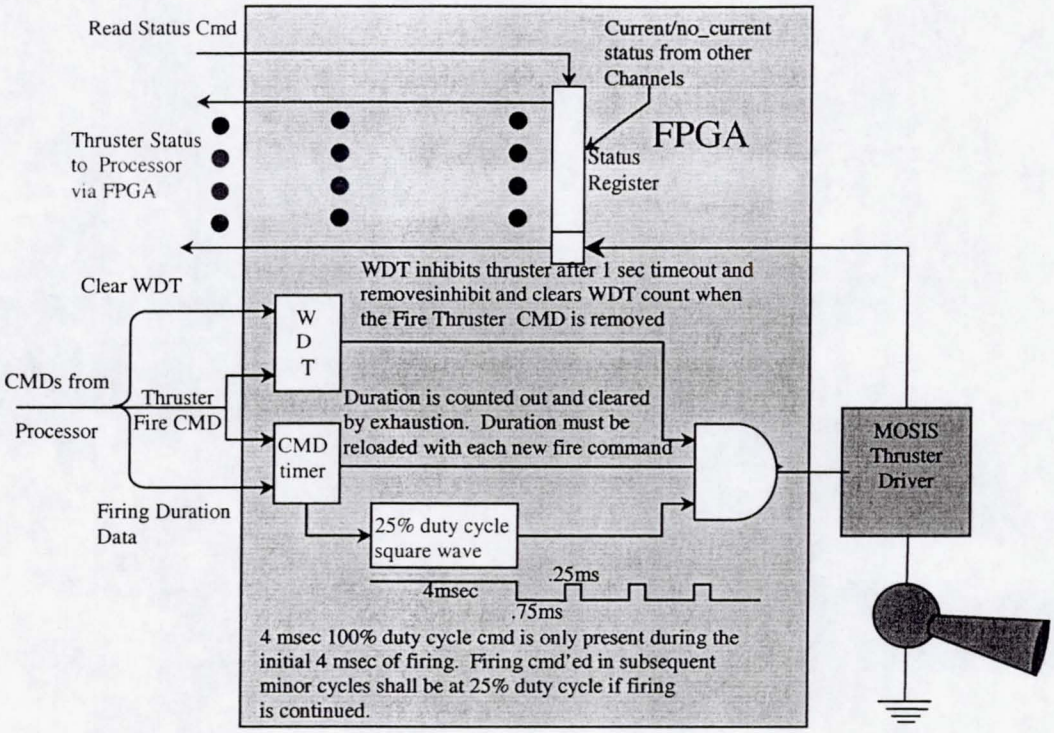

Figure 6: FPGA Thruster Driver Function

SUMMARY

Reference List

[1] Abbott, Larry W., Gary Cox, Hai Hguyen, Adapting PC/104 for Space, PC104 EmbeddedSolutions, Summer 2000, Volume 5 Number 2, Fountain Hills, Arizona, Open Systems Publishing, pages 33-40, www.pc104-embedded-solns.com.

[2] Abbott, Larry W., Gary Cox, Hai Hguyen, A Cost Effective System Design Approach for Critical Space Systems, 19th Digital Avionics System Conference, October 7-13, 2000, Philadelphia, Pa.