Electronics/Computers

Multiple Differential-Amplifier MMICs Embedded in Waveguides
Amplifiers are separated by no more than fractional-wavelength distances.

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Compact amplifier assemblies of a type now being developed for operation at frequencies of hundreds of gigahertz comprise multiple amplifier units in parallel arrangements to increase power and/or cascade arrangements to increase gains. Each amplifier unit is a monolithic microwave integrated circuit (MMIC) implementation of a pair of amplifiers in differential (in contradistinction to single-ended) configuration.

Heretofore, in cascading amplifiers to increase gain, it has been common practice to interconnect the amplifiers by use of wires and/or thin films on substrates. This practice has not yielded satisfactory results at frequencies >200 Hz, in each case, for either or both of two reasons:
• Wire bonds introduce large discontinuities.
• Because the interconnections are typically tens of wavelengths long, any impedance mismatches give rise to ripples in the gain-vs.-frequency response, which degrade the performance of the cascade.

Heretofore, it has been very difficult to achieve net increases in power by combining the outputs of amplifiers at frequencies >100 GHz. The only success-

ful approach that has been even marginally successful has involved the use of waveguide combiners designed and fabricated as components separate from the amplifiers. At these frequencies, even waveguides exhibit high losses that can easily dissipate any power gained by combining outputs.

In the present development, neither thin-film nor wire interconnections are used for cascading, and separate component waveguide combiners are not used for combining power. Instead, the amplifier units are designed integrally with the waveguides and designed to be embedded in the waveguides. The underlying concept of differential-amplifier MMICs designed integrally with and embedded in waveguides and the advantages of the differential over the single-ended configuration were reported in "Differential InP HEMT MMIC Amplifiers Embedded in Waveguides" (NPO-42857) *NASA Tech Briefs*, Vol. 33, No. 9 (September 2009), page 35. The novel aspect of the present development lies in combining the integration and embedment concepts with the cascading and parallel-combining concepts to obtain superior performance. In an amplifier assembly of the present type,

there is no need for interconnecting wires or thin-film conductors nor for separate waveguide power combiners because the waveguide in which the MMICs are embedded is the connecting medium. Because the distance between successive MMICs in a cascade is only a fraction of a wavelength, cascading can be highly efficient and ripple in gain versus frequency is reduced to a minimum. Moreover, power combining can be highly efficient because it is accomplished simply by placing MMICs side by side within the waveguide.

Rapid Corner Detection Using FPGAs
This algorithm can be used in automotive, navigation, and industrial factory applications.

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In order to perform precision landings for space missions, a control system must be accurate to within ten meters. Feature detection applied against images taken during descent and correlated against the provided base image is computationally expensive and requires tens of seconds of processing time to do just one image while the goal is to process multiple images per second.

To solve this problem, this algorithm takes that processing load from the central processing unit (CPU) and gives it to a reconfigurable field pro-

grammable gate array (FPGA), which is able to compute data in parallel at very high clock speeds. The workload of the processor then becomes simpler; to read an image from a camera, it is transferred into the FPGA, and the results are read back from the FPGA.

The Harris Corner Detector uses the determinant and trace to find a "corner score," with each step of the computation occurring on independent clock cycles. Essentially, the image is converted into an x and y derivative

map. Once three lines of pixel information have been queued up, valid pixel derivatives are clocked into the product and averaging phase of the pipeline. Each x and y derivative is squared against itself, as well as the product of the i_x and i_y derivative, and each value is stored in a W×N size buffer, where W represents the size of the integration window and N is the width of the image. In this particular case, a window size of 5 was chosen, and the image is 640×480.

Over a W×N size window, an equidis-