High-Performance CCSDS AOS Protocol Implementation in FPGA

Telemetry receivers can use this implementation to process telemetry at high rates.

NASA's Jet Propulsion Laboratory, Pasadena, California

The Consultative Committee for Space Data Systems (CCSDS) Advanced Orbiting Systems (AOS) space data link protocol provides a framing layer between channel coding such as LDPC (low-density parity-check) and higher-layer link multiplexing protocols such as CCSDS Encapsulation Service, which is described in the following article. Recent advancement in RF modem technology has allowed multi-megabit transmission over space links. With this increase in data rate, the CCSDS AOS protocol implementation needs to be optimized to both reduce energy consumption and operate at a high rate.

CCSDS AOS has been implemented as an intellectual property core so that the aforementioned problems are solved by way of operating the CCSDS AOS inside a field-programmable gate array (FPGA).

The CCSDS AOS in FPGA implementation consists of both framing and de-framing features.

Features of the AOS Framer include:

- Fully customizable with respect to insert zone, virtual channel ID, and trailer fields.
- 8-bit parallel CCITT CRC16 calculation.
- First header pointer field calculation based on the data provided from the packet layers such as CCSDS Encapsulation Service or CCSDS Space Packet.
- Optimized for the Packet Service primitives with M_PDU.
- Available in byte-based or packet-based egress interface options.
- Statistical counters at both byte and frame levels to facilitate data product accountability.

Features of the AOS De-Framer include:

- Ingress buffer implementation to provide ingress processing overflow.
- 8-bit parallel CCITT CRC16 calculation and frame discard if CRC16 fails.
- First header pointer field extraction and forwarding to the de-packetizing layers such as CCSDS Encapsulation Service or CCSDS Packet Service.
- Optimized for the Packet Service primitives with M_PDU.
- Statistical counters at both byte and frame levels to facilitate data product accountability.

The combination of energy and performance optimization that embodies this design makes the work novel.

This work was done by Loren P. Clare, Jordan L. Torgerson, and Jackson Pang of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov.

The software used in this innovation is available for commercial licensing. Please contact Daniel Broderick of the California Institute of Technology at danielb@caltech.edu. Refer to NPO-47166.

Advanced Flip Chips in Extreme Temperature Environments

This technology has application in avionics and electronics packaging.

NASA's Jet Propulsion Laboratory, Pasadena, California

The use of underfill materials is necessary with flip-chip interconnect technology to redistribute stresses due to mismatching coefficients of thermal expansion (CTEs) between dissimilar materials in the overall assembly. Underfills are formulated using organic polymers and possibly inorganic filler materials. There are a few ways to apply the underfills with flip-chip technology. Traditional capillary-flow underfill materials now possess high flow speed and reduced time to cure, but they still require additional processing steps beyond the typical surface-mount technology (SMT) assembly process.

Studies were conducted using underfills in a temperature range of -190 to 85 °C, which resulted in an increase of reliability by one to two orders of magnitude. Thermal shock of the flip-chip test articles was designed to induce failures at the interconnect sites (-40 to 100 °C). The study on the reliability of flip chips using underfills in the extreme temperature region is of significant value for space applications. This technology is considered as an enabling technology for future space missions.

Flip-chip interconnect technology is an advanced electrical interconnection approach where the silicon die or chip is electrically connected, face down, to the substrate by reflowing solder bumps on area-array metallized terminals on the die to matching footprints of solder-wettable pads on the chosen substrate. This advanced flip-chip interconnect technology will significantly improve the performance of high-speed systems, productivity enhancement over manual wire bonding, self-alignment during die joining, low lead inductances, and reduced need for attachment of precious metals.

The use of commercially developed no-flow fluxing underfills provides a means of reducing the processing steps employed in the traditional capillary flow methods to enhance SMT compatibility. Reliability of flip chips may be significantly increased by matching/tailoring the CTEs of the substrate material and the silicon die or chip, and also the underfill materials.

Advanced packaging interconnects technology such as flip-chip interconnect test boards have been subjected to various extreme temperature ranges that cover military specifications and extreme Mars and asteroid environments.

The eventual goal of each process step and the entire process is to produce components with 100 percent interconnect and satisfy the reliability requirements. Underfill materials, in general, may possibly meet demanding end use requirements such as low warpage, low stress, fine pitch, high reliability, and high adhesion.

This work was done by Rajeshuni Ramesham of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). ***NPO-41181***