Annual Conference of the Prognostics and Health Management Society, 2009

Effects of Lightning Injection on Power-MOSFETs

Jose Celaya[1], Sankalita Saha[2], Phil Wysocki[3], Jay Ely[4], Truong Nguyen[4], George Szatkowski[4], Sandra Koppen[4], John Mielnik[5], Roger Vaughan[5] and Kai Goebel[6]

[1]*SGT, Inc., NASA Ames Research Center, Moffett Field, CA, 94035, U.S.A.*
jose.r.celaya@nasa.gov

[2] *MCT, Inc., NASA Ames Research Center, Moffett Field CA, 94035, USA*
sankalita.saha-1@nasa.gov

[3] *ASRC Aerospace Corp., NASA Ames Research Center, Moffett Field CA, 94035, USA*
philip.f.wysocki@nasa.gov

[4] *NASA Langley Research Center, Hampton VA, 23681, USA*
jay.j.ely@nasa.gov
truong.x.nguyen@nasa.gov
george.n.szatkowski@nasa.gov
sandra.v.koppen@nasa.gov

[5] *Lockheed Martin Corporation, Hampton, Virginia, 23681, USA*
john.j.mielnik@nasa.gov
roger.k.vaughan@nasa.gov

[6] *NASA Ames Research Center, Moffett Field CA, 94035, USA*
kai.goebel@nasa.gov

ABSTRACT

Lightning induced damage is one of the major concerns in aircraft health monitoring. Such short-duration high voltages can cause significant damage to electronic devices. This paper presents a study on the effects of lightning injection on power metal-oxide semiconductor field effect transistors (MOSFETs). This approach consisted of pin-injecting lightning waveforms into the gate, drain and/or source of MOSFET devices while they were in the OFF-state. Analysis of the characteristic curves of the devices showed that for certain injection modes the devices can accumulate considerable damage rendering them inoperable. Early results demonstrate that a power MOSFET, even in its off-state, can incur considerable damage due to lightning pin injection, leading to significant deviation in its behavior and performance, and to possibly early device failures.*

1. INTRODUCTION

Power electronic devices such as power MOSFETs and Insulated Gate Bipolar Transistors (IGBTs) play an ever-increasing role in avionic systems where they are frequently used in high-power switching circuits. These switching circuits are present in a wide array of on-board electronic functions such as vehicle controls, communications, navigation, and radar systems. These electronic systems are frequently subject to off-nominal operating environments caused from exposure to events

such as lightning strikes or radiation, resulting in damage to component level devices such as power MOSFETs. Thus, understanding the effects of such events on these devices and the corresponding changes in behavior during normal operation is of significant importance for ensuring safety as well as reducing cost of maintenance and operations.

Commercial transport airplanes are typically struck by lightning once every 1000 to 20,000 flight hours (SAE 2005). Lightning caused by thunderstorms can produce currents as high as 500 kA and voltage potentials up to 30,000 kV, which are far beyond the normal operating range for these components. Significant shielding exists that is in place to prevent individual components from experiencing catastrophic failure or to be otherwise negatively affected. Nonetheless, it is possible for some surges to reach the components inductively or conductively. The interplay between lightning induced surges and device degradation is likely to reduce performance over the life of semiconductor components and result in failure before their expected lifetime.

This paper contributes to the understanding of deterioration effects on power electronic devices that are subjected to very high stress events. Going forward, this study will be extended to show how such events affect the accelerated aging of the devices as outlined in (Saha et al. 2009; Sonnenfeld et al. 2008). Such studies and analysis will provide a better understanding of aging behavior of these devices in adverse aerospace environments and in the prevention of unexpected catastrophic failures. Specifically, this paper presents preliminary results and analysis of lightning effects on power MOSFETs. These MOSFET devices were injected with different lightning waveforms under different pin configurations. The effects of these fault injections were studied by comparing key characteristic curves before and after injection as well as the output transient voltage waveforms. Significant deterioration in electrical characteristics was observed, indicating a reduced lifetime for such devices.

2. BACKGROUND

Prognostics and health management for electronic components is a relatively new research field as most of the past effort was concentrated on reliability-based studies. Until now, most of the focus has been on developing accelerated aging methodologies for these components by means of electrical, thermal or mechanical overstress (Lall et al. 2008; Saha et al. 2009; Sonnenfeld et al. 2008). However, understanding aging effects on electronic devices following single very-high stress events, such as lightning or electro-static discharge, is of significant importance as well. Though efforts have been made to observe effects of such fault injections, most of them have mainly been done from a reliability perspective.

The results presented in this work are part of an ongoing research effort geared towards health management of discrete power semiconductor devices at the component level. The overall hypothesis of this research effort is that a) there will be significant changes in the degradation process of devices exposed to lightning events, b) such devices will incur certain levels of damage due to the lightning event but not necessarily a catastrophic failure, c) such devices would still operate within specification limits but performance will be diminished, and d) the precursors to failure can be detected, therefore health management techniques can be applied.

Figure 1 shows the steps followed in this research effort. First, key electrical parameters are characterized for a set of pristine devices. Then, a subset of these devices is subjected to different levels and configurations of electrical waveforms representative of lightning events on avionics equipment. This is followed by a characterization of electrical parameters in order to assess the damage incurred by the devices due to the lightning injection. These devices along with a subset of pristine devices will then be aged in order to make an assessment of the effects of lightning events in the degradation process. The methodology outlined here will aid the development of damage progression models and finally, the development of prognostics algorithms that predict the remaining useful life of devices exposed to lightning events.

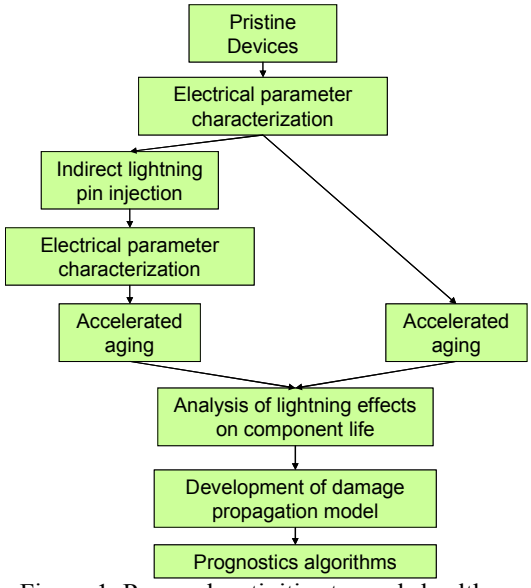

Figure 1. Research activities towards health management of power MOSFETs affected by lightning events.

2.1. Approach

The technical approach behind the study and analysis of lightning injection damage involves multiple steps and is outlined here and in the following sub-sections. First, the lightning injection effect was studied at component level using indirect pin-injection methodology. The devices were then put together in an unbiased set up for

different pin-injection configurations. This setup is further explained in section 3.2. Repeated tests or pretests were conducted to determine the appropriate lightning severity levels for the different pin configurations. The levels are designated as low, high and medium as described later. The different voltage waveforms that were explored in order to emulate real-life component pin-injection are explained in detail in section 3.1. These configurations were then tested using multiple samples of the device in order to investigate repeatability of the results. As explained in the experimental results section (section 4), it was observed that the configuration involving pin-injection at the gate-source (G-S) resulted in significant deviation in device behavior. Therefore, the G-S configuration damage was studied in more detail.

2.2. Related work

Prior studies and analysis of lightning effects on semiconductors, is devoted to the protection of equipment from lightning, including innovative surge protection circuitry for semiconductor devices e.g., (Satoh and Shimoda 1996). Various studies of both passive as well as active component behavior during and after passing of high voltage transients have been conducted. For example, in (Tasca 1976) and (Case and Miletta 1975), resistor and capacitor damage characteristics and failures have been analyzed. In (Wunsch and Bell 1968), (Tasca 1970) and (Jenkins and Durgin 1975), similar studies have been conducted for semiconductor components. In (Wunsch and Bell 1968), the focus is on the threshold failure levels for diodes and transistors, while in (Tasca 1970) submicroscopic pulse power failure modes for generic semiconductor devices both in biased and unbiased conditions are presented. In (Jenkins and Durgin 1975), the authors present test results for pulse power threshold levels for seven logic families of semiconductors. The work by (Jeong 2005) discusses failure mechanisms of high voltage bipolar junction transistors based line drivers for ADSL (Asymmetric Digital Subscriber Line) systems from lightning surges. Within this study, a transient temperature response analysis was carried out to determine the relationship between the temperature and the failure lightning surges applied. Lightning surges for two different configurations were applied and transient latch-up was observed as the main failure mechanism. A discussion on different methodologies of injecting lightning surges, system level tests and damage level tests is presented in (Plumer 2009). A transient temperature response analysis was performed in (Satoh 2007) in order to determine the relationship between temperature and failure under the application of a lightning surge to avalanche diodes, which are typically used in lightning surge protectors. Based on these findings one may conclude that there exists a distinct gap between the current state of the art and the required understanding of lightning effects on power semiconductors in order to apply health management techniques.

2.3. Effects of lightning events on semiconductor devices

Lightning can affect semiconductor components in several ways: In some cases, the device is damaged beyond repair (hard failure). In other cases, degradation gets introduced in the internal electrical junctions of the device such that they are still operable but fail to perform within specifications. Such cases are of grave concern since they may go unnoticed during regular maintenance leading to unexpected failures later. For example, a power MOSFET in a switching circuit may incur small damage due to a transient voltage from lightning which then changes the threshold voltage. This change alone does not affect the power switching capabilities of the device; however, when subjected to its operation environment or other adverse environmental conditions such as higher operating temperature or vibration, the aging of the device accelerates thereby reducing the threshold voltage significantly and ultimately resulting in a breakdown of the device.

Failure modes for power transistors include:

1. Junction damage: Semiconductor devices are prone to damage at the internal junctions due to heating and the subsequent temperature rise within the junction. Such temperature rise modifies the carrier concentrations as well as their mobility thereby altering their electrical behavior.
2. Metallization damage: High voltages can damage external elements of the device such as contact leads and conductor traces of devices embedded in integrated chips. Melting of these elements occur by virtue of the heat generated by the transient current. Although this type of damage does not affect the semiconductor die directly, it can cause damage which can significantly change the operating input/output signal levels.
3. Voltage punch-through: High transient voltages lead to high electric fields that can significantly alter gate behavior of MOSFET devices by causing punch-through in the oxide dielectric layer.

An interesting characteristic of semiconductors is the large variation in the amount of transient power required to be deposited in the device for damage, even for devices within the same manufacturing lot. Another feature of semiconductors is that cumulative effects can cause significant damage i.e., subsequent application of lower voltage levels can cause similar damage as a significantly high voltage level. Thus, if an initial voltage pulse of peak value V_{damage} renders a device beyond operation, cumulative application of pulses at 25% of V_{damage} can cause equivalent damage (Keefe and Perala 1999). These features were corroborated from observations in our experiments as mentioned in details in section 4.

3. LIGHTNING INJECTION EXPERIMENT

There are several elements in avionics equipment of modern and future aircraft that could potentially be affected by a lightning event (see Figure 2). As show, lightning strikes the fuselage of the aircraft and the energy propagates all the way to the electronics equipment, in particular components which in this case consist of power MOSFETS typically found in power modules and drivers for electro-mechanical actuators.

This propagation model is used in devising waveforms emulating real-life lightning effects for the purpose of study and analysis at laboratories. Details of these waveforms as outlined in the lightning waveform reference standard RTCA/DO-160E (RTCA/DO-160E 2004) and how they are customized for our studies are explained in the following section.

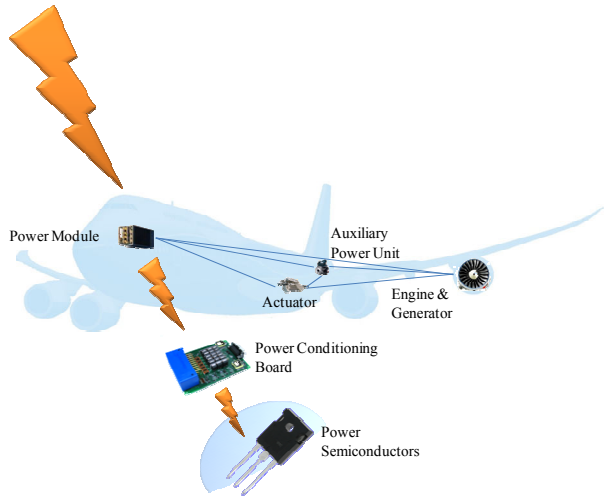

Figure 2. Propagation of lightning event through avionics.

3.1. Lightning injection methodology for electronic components

In order to determine lightning waveforms to be injected that are representative of real situations and the required intensity of the waveform pulses, the lightning waveform reference standard described in RTCA/DO-160E (RTCA/DO-160E 2004) was used. RTCA/DO-160E is intended for establishing flight worthiness tests of airborne equipment.

Since the waveforms described in this standard apply to assembled electronic systems rather than individual components, the test setup described in the standard was modified accordingly (Ely et al. 2009). Two of the waveforms selected for the test setup are shown in the following figures and consist of a "damped sinusoid" (Waveform 3 in Figure 3), "6.4µs-rise double exponential" (Waveform 4 in Figure 4) and a "40µs-rise double exponential" (Waveform 5). The figure for Waveform 5 is not presented given that it is similar to that of Waveform 4.

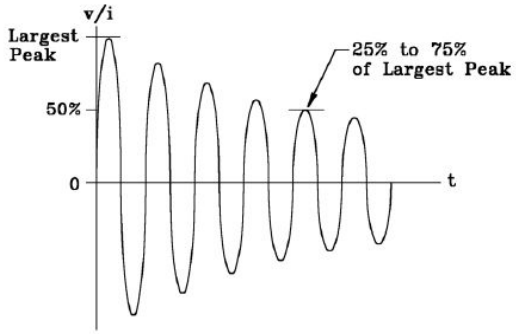

Figure 3. Voltage and current Waveform 3.

In general, Waveforms 3 and 4 simulate actual lightning waveforms encountered when airborne equipment is subjected to lightning-induced magnetic fields coupled to wiring. Waveform 5 simulates actual lightning waveforms encountered within airborne equipment subjected to direct conduction current paths when current flows through the airframe. Tests were conducted with the three different waveforms. Additional details on test setup, equipment used, and other testing considerations are presented in (Ely et al. 2009). Only results on test with Waveforms 3 and 4 are presented in this paper.

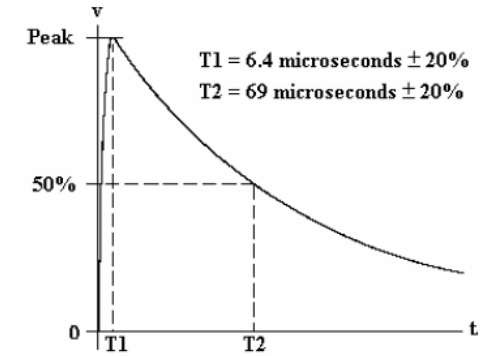

Figure 4. Voltage/Current Waveform 4.

Table 1 summarizes the voltage peak levels for the different waveforms for different environment conditions. For Waveform 3, V_{oc} and I_{sc} represent the largest amplitude on the waveform as presented in Figure 3. For Waveform 4 and Waveform 5, V_{oc} represents the peak voltage of the double exponential signal (see Figure 4 for Waveform 4) and I_{sc} represents the limit in the current sourced by such waveforms.

Table 1. DO-160E test levels for pin injection

Level	Representative Environment	Wave-form 3 (Voc/Isc)	Wave-form 4 (Voc/Isc)	Wave-form 5 (Voc/Isc)
1	Well Shielded	100/4	50/10	50/50
2	Partially Shielded	250/10	125/25	125/125
3	Partially Exposed	600/24	300/60	300/300
4	Severe	1500/60	750/150	750/750
5	More Severe	3200/ 128	1600/ 320	1600/ 1600

3.2. Lightning injection circuit setup

All testing was conducted in NASA's High Intensity Radiated Field (HIRF) Laboratory at NASA Langley Research Center. The HIRF Laboratory is equipped with generators for indirect lighting effects testing.

Lightning waveforms are injected directly to the terminals of the power MOSFET (Gate, Drain and Source). The gate serves as the switching control for the device. A biased gate will reduce the resistance from drain to source (R_{DS}) allowing current to flow from the drain to the source (ON-state). An unbiased gate will increase the resistance to a very large value (OFF-state). The experiments performed in this work consist only of lightning injections on the unbiased OFF-state. The lightning current will enter through one of terminals of the device and will exit to another of the terminals allowing for a total of six different pin-injection configurations.

The voltage pin injection setup is shown in Figure 5. The lightning generator equipment can produce waveforms of different intensity levels described earlier. It also provides a trigger signal used here to start the data acquisition by the oscilloscope. An attenuator consisting of a resistor network is used to achieve better resolution on the intensity of the injected waveform. High voltage probes are used to measure the injected voltage as well as a current sensor to monitor the current passing through the devices during the injection.

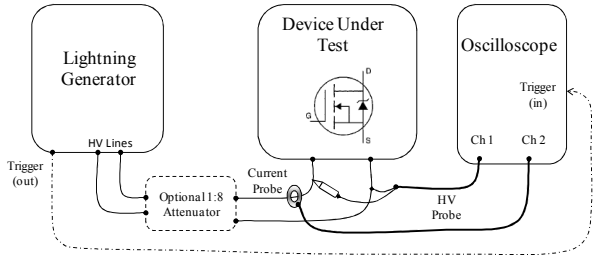

Figure 5. Pin injection test setup diagram.

3.3. Experimental details

First, a set of device characterization tests were carried out on several MOSFETs in order to determine the baseline parameters required for comparison against the characterization parameters of the lightning injected devices. All of these devices were tested in their unbiased OFF-state and under six different configurations to inject the voltage, as shown in Table 2.

Table 2. Pin connection nomenclature.

Pin Configuration	+Voltage Connected To:	-Voltage Connected To:
G-D	Gate	Drain
D-G	Drain	Gate
G-S	Gate	Source
S-G	Source	Gate
D-S	Drain	Source
S-D	Source	Drain

Three different voltage levels and two different waveforms were used. Table 3 summarizes these experiments.

Table 3. Lightning injection test matrix.

Waveform Type	Pin Config.	Levels	Number of Strokes	Test Samples
4	G-S	H, M, L	5, 10, 20	5
4	D-S	H, M, L	5, 10, 20	5
4	D-G	H, M, L	5, 10, 20	5
4	S-G	H, M, L	5, 10, 20	5
4	G-D	H, M, L	5, 10, 20	5
4	S-D	H, M, L	5, 10, 20	5
3	G-S	H, M, L	5, 10, 20	4

Injected voltage and current transient waveform data was collected. Additionally, post-injection component evaluation tests were performed in order to analyze the effects of the stress, as described in the following section.

3.4. Characterization of electrical parameters for MOSFETs

Electrical characteristics of the power MOSFETs were collected to verify whether the devices under test have incurred any damage. This test included a characterization of key electrical parameters to determine if damage had occurred and also to measure the extent of damage these devices experienced. In particular, three electrical parameters are used as health indicators for these devices; a) breakdown voltage, b) leakage current levels, and c) threshold voltage. Details of these parameters and their implications to the operation of the devices are given below.

3.4.1. Breakdown voltage ($V_{(BR)DSS}$)

The breakdown voltage ($V_{(BR)DSS}$) indicates the voltage level at which the drain-source path of the device starts conducting drain current (I_D) given that the gate is not biased (V_{GS}=0V). Under normal operation, the drain-source path should behave like an open circuit and very little current (in the μA range) should flow through the

device when the gate is not biased. As the voltage applied between the drain and source terminals (V_{DS}) increases, it reaches a point where the device starts conducting current. A source measurement unit (SMU) is required to assess the value of this parameter. This equipment is able to source large voltages while measuring the supplied current with high precision (usually at the pA levels). Figure 6 shows the configuration of the breakdown voltage tests.

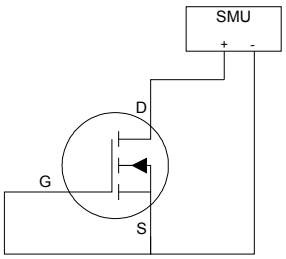

Figure 6. Leakage current and breakdown voltage tests for an n-type power MOSFET.

3.4.2. Leakage Current (I_{DSS})

The drain to source leakage current (I_{DSS}) is the current flowing from drain to source as the gate is shorted with the source (no gate bias, V_{GS}=0V). The gate and source are connected to the negative connector of the SMU which is grounded and the drain is connected to the positive terminal (see Figure 6).

3.4.3. Threshold Voltage ($V_{GS(th)}$)

The gate threshold voltage ($V_{GS(th)}$) refers to the minimum voltage required to bias the gate in order for the device to switch ON and allow drain current (I_D) to flow. This parameter is likely to change due to damage in the gate oxide of the device. The SMU equipment is used to measure these parameters by providing a voltage sweep at V_{GS} until reaching the point where I_D starts growing exponentially. Figure 7 shows the test configuration for threshold voltage measurement.

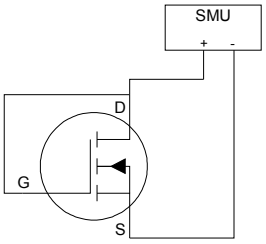

Figure 7. Threshold voltage test for an n-type power MOSFET.

4. EXPERIMENT RESULTS

This section presents the results from the experiments described in the previous section. First, a series of preliminary test were performed in order to establish the lightning intensity levels used for each of the experiment configurations described in Table 3. The electrical parameters are then measured for all the devices in the test matrix. A summary of the effects of lightning injection on the threshold voltage is presented for all the test configurations. In addition, the Gate-Source configuration results are presented in more detail.

4.1. Establishing maximum sustainable lightning intensity levels

A series of preliminary test were performed to identify the injection intensity levels for each of the waveforms described earlier. These tests first identified a peak voltage where the devices failed, as well as maximum peak voltage, where the devices could withstand 20 lightning injection strokes without failing. Table 4 lists the resulting intensity levels for Waveform 4. At the high voltage level the devices withstand 20 strokes without failure, the medium level is at 90% of the high level, and the low level is at 80% of the high level. For the Source-Drain configuration, the fail voltage was found to be higher than the lightning injection equipment capabilities.

In addition, Table 5 presents the intensity levels for Waveform 3. At the high voltage level the devices withstand 20 strokes without failure, the medium level is at 90% of the high level, and the low level is at 80% of the high level. Similar to the Waveform 4 case, the fail voltage for Source-Drain configuration exceeded the equipment capabilities. It should be noted that the power MOSFET has an internal diode which allows the flow of large currents from Source to Drain and the breakdown voltage of this diode is larger than the voltage capabilities of the lightning generator used in this study.

Table 4. Voltage intensity levels for Waveform 4.

Pin Config.	Fail (V)	High (V)	Medium (V)	Low (V)
G-D	90	75	68	60
G-S	80	76	68	61
D-S	280	266	239	213
D-G	200	170	153	136
S-G	70	55	50	44
S-D	>1700	-	-	-

Table 5. Voltage intensity levels for Waveform 3.

Pin Config.	Fail (V)	High (V)	Medium (V)	Low (V)
G-D	90	86	77	68
G-S	55	47	42	40
D-S	2200	2090	1881	1672
D-G	90	86	77	68
S-G	55	47	42	40
S-D	>2200			

The lightning injection levels presented in the two tables above were used to perform a series of experiments as outlined in section 3.3.

4.2. Results from component evaluation test

This section presents a summary of the results from the experiments listed in Table 3. The threshold voltage parameter is used to assess the health of the injected devices. The results from component evaluation test for Waveform 4 are shown in Table 6 through Table 9. These results show the median change in threshold voltage. The change in threshold voltage is computed by comparing the parameter measurement before and after the injection. The median of all the five samples for each experiment configuration (e.g. G-S configuration with high voltage intensity and 20 lightning injection strokes) is then taken. The median is used as an estimator of central tendency. It is used instead of a simple average due to its better performance under the presence of outliers and in situations where the number of samples is small.

Results for the Gate-Source configuration test are shown in Table 6. These results suggest that damage accumulates as a result of repeated injections. In addition, the damage magnitude increases as the intensity level of the injection increases. However, the same is not observed in the Source-Gate configuration as shown in Table 7.

Table 6. Median threshold voltage deviation for Gate-Source configuration (Volts).

Voltage Level	Strokes		
	5	**10**	**20**
High	0.0225	0.0518	0.2828
Medium	0	0.0033	0.0059
Low	0	0	0

Table 7. Median threshold voltage deviation for Source-Gate configuration (Volts).

Voltage Level	Strokes		
	5	**10**	**20**
High	0.0119	0.0115	0.0132
Medium	0.0074	0.0101	0.0091
Low	0.0094	0.0091	0.0084

The results for the Gate-Drain and Drain-Gate test configurations are presented in Table 8 and Table 9 respectively. It can be observed, that these results are not consistent with the damage accumulation hypothesis since there is no uniform decrease in the threshold voltage as more injections are applied or the injection intensity is increased.

No significant change in threshold voltage was observed for Drain Source and Source-Drain configurations.

Table 8. Median threshold voltage deviation for Gate-Drain configuration (Volts).

Voltage Level	Strokes		
	5	**10**	**20**
High	0.0383	0.0526	0.0721
Medium	0.0319	0.4064	0.4231
Low	0.3931	0.0204	0.0204

Table 9. Median threshold voltage deviation for Drain-Gate configuration (Volts).

Voltage Level	Strokes		
	5	**10**	**20**
High	0	0	0
Medium	0	0	0.3632
Low	0.2471	0.1281	0.0113

4.2.1. Discussion

Even though devices from the same manufacturer were used, the change in threshold voltage can vary considerably. Since most of devices have extremely small physical size – the die thickness is of the order of 0.1μm – even the slight variability in the manufacturing process affects the physical parameters such as thickness of oxide layer, or doping concentration significantly. Thus, devices with the same specifications from the manufacturer can behave differently from each other in terms of threshold voltage and hence fail in different manner as well.

4.3. Analysis of results of Gate-Source test configuration

The threshold voltage sweep curves were analyzed for all the cases from which it was concluded that the Gate-Source configuration showed significant deviation from normal behavior and hence was selected for further investigation.

For the MOSFET used in this work (IRF520Npbf), the drain-to-source leakage current (I_{DSS}) specifications are: a) max I_{DSS}=25μA for V_{DS}=100V and V_{GS}=0V at room temperature (25^{o}C); and b) max I_{DSS}=250μA for V_{DS}=88V, V_{GS}=0V, and T_J=150^{o}C.

Figure 8 shows the I-V characteristic curve on V_{DS} and I_D from measurements, which is used to identify breakdown voltage for a device. This device was injected in the Gate-Source configuration using a high-voltage setting (76V) and 20 consecutive strokes. As a result of the repeated injection, the breakdown voltage shifts to towards the left by ~1 V which is a significant deviation well beyond instrument error margin. It

should be noted that even after the injection, the breakdown voltage still complies with the ratings given in the specification datasheet. It is evident from these observations, that the injections cause some latent damage and should be further investigated to determine whether such damage affects the further operation and the remaining useful life of the device.

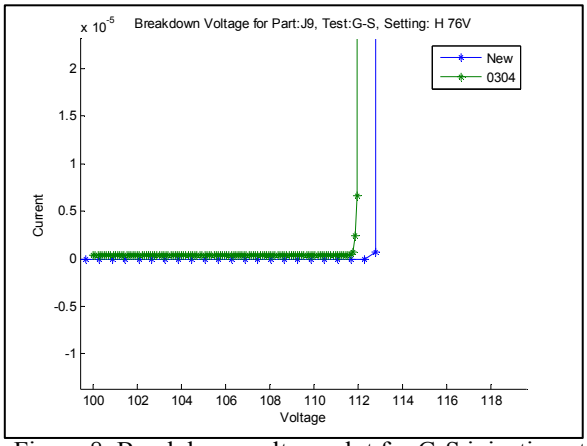

Figure 8. Breakdown voltage plot for G-S injection at high voltage setting (76V).

Figure 9 shows the results of the leakage current test performed on the same device. It was observed that the leakage current increases due the lightning injection. The observed leakage current while incurring significant change from normal behavior still conforms to the specification datasheet and it is evident that there is damage resulting from the repeated lightning strokes.

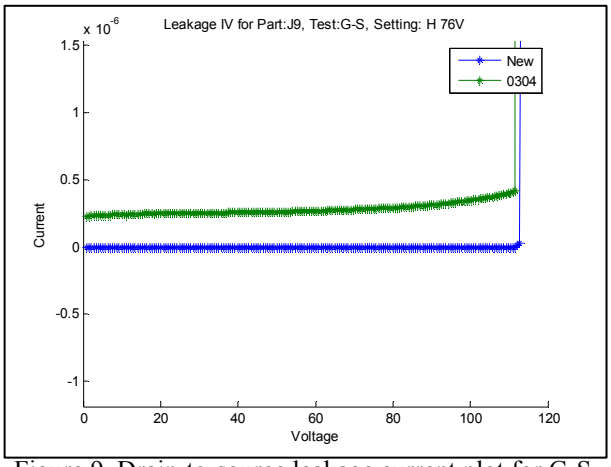

Figure 9. Drain-to-source leakage current plot for G-S injection at high voltage setting (76V).

The threshold voltage rating for the MOSFET under study indicates a minimum threshold voltage $V_{GS(th)}$= 2V and a maximum of $V_{GS(th)}$= 4V with V_{GS}= V_{DS} and I_D= 250uA. Figure 10 show changes in the threshold voltage which shows change beyond instrument error margins. The shift in the threshold voltage by a few hundred mV implies that the device requires a lower bias voltage to switch ON. This change is an indication of significant damage on the gate, even though the device still complies with the rating specified in the datasheet.

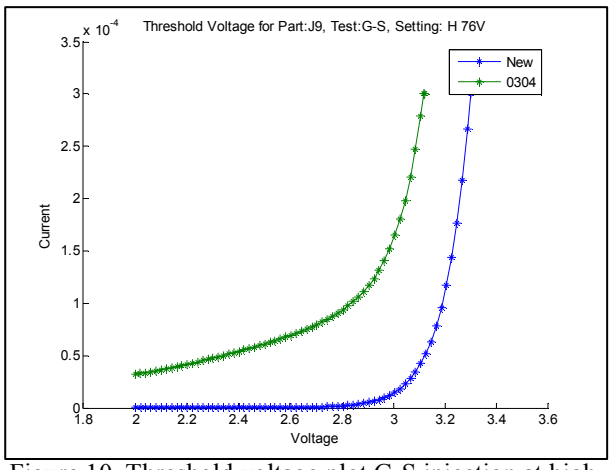

Figure 10. Threshold voltage plot G-S injection at high voltage setting (76V).

5. CONCLUSION

In this paper, the effect of lightning strikes on performance characteristics of power semiconductors is reported. Analysis of the characteristic curves of the devices showed that for certain injection modes the devices can accumulate noticeable damage. Significantly, this is the case even if the device is in its off-state. Thus, while the damage incurred is not severe enough to cause immediate failure, it may result in early failure and/or unexpected behavior in later operation and in operation under severe environmental conditions.

Work is under way to understand the possible damage these devices will incur while they are in the ON-state. This work will be further extended to understand how such stress affect the accelerated aging of the devices under electrical and thermal overstress (as outlined in (Saha et al. 2009; Sonnenfeld et al. 2008)) of the devices. The ultimate goal is to apply prognostic and health management algorithms using the features extracted during aging to allow calculation of expected remaining useful life. This will counteract some of the negative effects of damage incurred by lightning by providing information prior to the components failure such that safe operation of the system is maintained.

ACKNOWLEDGMENTS

The authors would like to express their gratitude to colleagues Abhinav Saxena, Bhaskar Saha and Mona

Fahimi at the Prognostic Center of Excellence (NASA Ames Research Center) for participating in research discussions. This work was funded by NASA Aviation Safety Program-IVHM Project.

REFERENCES

(Case and Miletta 1975) C. Case and J. Miletta. Capacitor Failure due to High Level Electrical Transients, *Harry Diamond Laboratories*, HDL-YM-75-25, 1975.

(Ely et al. 2009) J. J. Ely, T. X. Nguyen, G. N. Szatkowski, S. V. Koppen, J. J. Mielnik, R. K. Vaughan, P. F. Wysocki, J. R. Celaya and S. Saha. Lightning Pin Injection Testing on MOSFETS, *NASA*, TM-2009-215794, 2009.

(Jenkins and Durgin 1975) C. R. Jenkins and D. L. Durgin. EMP Susceptibility of Integrated Circuits, *in Proceedings of IEEE Conference on Nuclear and Space Radiation Effects*, 1975.

(Jeong 2005) J.-S. Jeong. Stress Mechanism about Field Lightning Surge of High Voltage BJT Based Line Driver for ADSL System, *Journal of Microelectronics Reliability,* vol. 45, pp. 1398-1401, 2005.

(Keefe and Perala 1999) R. L. Keefe and R. A. Perala. Lightning Protection for Modern Signal Systems, *in Proceedings of AREMA Annual Conference*, 1999.

(Lall et al. 2008) P. Lall, C. Bhat, M. Hande, V. More, R. Vaidya, J. Suhling, R. Pandher and K. Goebel. Latent Damage Assessent and Prognostication of Residual Life in Airborne Lead-Free Electronics Under Thermo-Mechanical Loads, *in Proceedings of International Conference on Prognostics and Health Management*, 2008.

(Plumer 2009) J. A. Plumer. System Functional Upset testing of Aircraft Electrical and Avionic Systems: How to Approach the Planning and Conduct of the Tests, *Lightning Technologies, Inc.*, http://www.lightningtech.com/pdfs/icolse.pdf, last access on September 2009.

(RTCA/DO-160E 2004) RTCA/DO-160E. Environmental Conditions and Test Procedures for Airborne Equipment, Section 22 "Lightning Induced Transient Susceptibility", *RTCA*, DO-160E, 2004.

(SAE 2005) SAE. Aircraft Lightning Environment and Related Test Waveforms, *SAE*, ARP5412, 2005.

(Saha et al. 2009) B. Saha, J. Celaya, K. Goebel and P. Wysocki. Towards Prognostics for Electronics Components, *in Proceedings of IEEE AEROSPACE*, 2009.

(Satoh 2007) H. Satoh. Transient temperature response of avalanche diodes against lightning surges, *Electronics and Communications in Japan (Part II: Electronics),* vol. 72:(10), pp. 33-39, 2007.

(Satoh and Shimoda 1996) H. Satoh and Y. Shimoda. Two-dimensional analysis of surge response in thyristor lightning surge protection devices, *in Proceedings of 8th International Symposium on Power Semiconductor Devices and ICs*, 1996.

(Sonnenfeld et al. 2008) G. Sonnenfeld, K. Goebel and J. R. Celaya. An agile accelerated aging, characterization and scenario simulation system for gate controlled power transistors, *in Proceedings of IEEE AUTOTESTCON*, 2008.

(Tasca 1970) D. M. Tasca. Pulse Power Failure Modes in Semiconductors, *IEEE Transactions on Nuclear Science,* vol. 17:(6), 1970.

(Tasca 1976) D. M. Tasca. Pulse Power Damage Characteristics of Electrical Resistors, *Air Force Weapons Laboratory*, 1976.

(Wunsch and Bell 1968) D. C. Wunsch and R. R. Bell. Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulse Voltages, *IEEE Transactions on Nuclear Science,* vol. 15:(6), pp. 244-259, 1968.

Jose Celaya is a staff scientist with Stinger Ghaffarian Technologies at the Prognostics Center of Excellence, NASA Ames Research Center. He received a Ph.D. degree in Decision Sciences and Engineering Systems in 2008, a M. E. degree in Operations Research and Statistics in 2008, a M. S. degree in Electrical Engineering in 2003, all from Rensselaer Polytechnic Institute, Troy New York; and a B.S. in Cybernetics Engineering in 2001 from CETYS University, Mexico.

Sankalita Saha is a research scientist with Mission Critical Technologies at the Prognostics Center of Excellence, NASA Ames Research Center. She received her M.S and PhD degrees in Electrical Engineering from University of Maryland, College Park in 2007. Prior to that she obtained her B.Tech degree in Electronics and Electrical Communications Engineering

from the Indian Institute of Technology, Kharagpur in 2002.

Phil Wysocki has extensive knowledge and background in test model based data acquisition, as well as programming and system design for diagnostics. He has developed and implemented test design for aging and characterizing IC's and environmental testing. This includes optimization of test hardware and software for prognostics. Phil earned a Bachelor of Science Degree in Computer Science along with over 25 years experience demonstrated at NASA Ames Research Center.

Jay Ely has been a research engineer for the HIRF laboratory at NASA Langley Research Center since 1996. He is interested in emerging radio technologies and how air vehicle operations, communication, navigation and surveillance are affected by the electromagnetic environment. From 1987 to 1996, Jay was a member of the Space Shuttle launch team at the Kennedy Space Center. He earned a BSEE degree from the University of South Florida in 1987, and a MSEE degree from the University of Central Florida in 1995.

John Mielnik is an Electronics engineering technician with Lockheed Martin working in the LaRC HIRF laboratory. He has 16+ years aircraft avionics and maintenance experience and an Associates Degree in Specialized Technology received in 1992 from the Pittsburgh Institute of Aeronautics, as well as FAA Airframe and Powerplant certificates, FAA Inspection Authorization, FCC General Radiotelephone Operators License with RADAR endorsement, and NASA Level B instructor NASA-STD-8739.3 Hand soldering, and NASA-STD-9739.4 Crimp, Cable, and Harness.

Kai Goebel received the degree of Diplom-Ingenieur from the Technische Universität München, Germany in 1990. He received the M.S. and Ph.D. from the University of California at Berkeley in 1993 and 1996, respectively. Dr. Goebel is a senior scientist at NASA Ames Research Center where he leads the Diagnostics & Prognostics groups in the Intelligent Systems division. In addition, he directs the Prognostics Center of Excellence and he is the Associate Principal Investigator for Prognostics of NASA's Integrated Vehicle Health Management Program. He worked at General Electric's Corporate Research Center in Niskayuna, NY from 1997 to 2006 as a senior research scientist. He has carried out applied research in the areas of artificial intelligence, soft computing, and information fusion. His research interest lies in advancing these techniques for real time monitoring, diagnostics, and prognostics. He holds eleven patents and has published more than 100 papers in the area of systems health management.