



Electronics/Computers

Reconfigurable Hardware for Compressing Hyperspectral Image Data

Multiple hardware cores can be combined to increase throughput.

NASA's Jet Propulsion Laboratory, Pasadena, California

High-speed, low-power, reconfigurable electronic hardware has been developed to implement ICER-3D, an algorithm for compressing hyperspectral-image data. The algorithm and parts thereof have been the topics of several *NASA Tech Briefs* articles, including "Context Modeler for Wavelet Compression of Hyperspectral Images" (NPO-43239) and "ICER-3D Hyperspectral Image Compression Software" (NPO-43238), which appear elsewhere in this issue of *NASA Tech Briefs*. As described in more detail in those articles, the algorithm includes three main subalgorithms: one for computing wavelet transforms, one for context modeling, and one for entropy encoding. For the purpose of designing the hardware, these subalgorithms are treated as modules to be implemented efficiently in field-programmable gate arrays (FPGAs).

The design takes advantage of industry-standard, commercially available FPGAs. The implementation targets the Xilinx Virtex II pro architecture, which has embedded PowerPC processor cores with flexible on-chip bus architecture. It incorporates an efficient parallel and pipelined architecture to compress the three-dimensional image data. The design provides for internal buffering to minimize intensive input/output operations while making efficient use of off-chip memory. The design is scalable in that the subalgorithms are implemented as independent hardware modules that can be combined in parallel to increase throughput. The on-chip processor manages the overall operation of the compression system, including execution of the top-level control functions as well as scheduling, initiating, and monitoring processes.

The design prototype has been demonstrated to be capable of compressing hyperspectral data at a rate of 4.5 megasamples per second at a conservative clock frequency of 50 MHz, with a potential for substantially greater throughput at a higher clock frequency. The power consumption of the prototype is less than 6.5 W.

The reconfigurability (by means of reprogramming) of the FPGAs makes it possible to effectively alter the design to some extent to satisfy different requirements without adding hardware. The implementation could be easily propagated to future FPGA generations and/or to custom application-specific integrated circuits.

This work was done by Nazeeh Aranki, Jeffrey Namkung, Carlos Villalpando, Aaron Kiely, Matthew Klimesh, and Hua Xie of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-42834

Spatio-Temporal Equalizer for a Receiving-Antenna Feed Array

Suppression of multipath effects and robust pointing would be achieved.

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A spatio-temporal equalizer has been conceived as an improved means of suppressing multipath effects in the reception of aeronautical telemetry signals, and may be adaptable to radar and aeronautical communication applications as well. This equalizer would be an integral part of a system that would also include a seven-element planar array of receiving feed horns centered at the focal point of a paraboloidal antenna that would be nominally aimed at or near the aircraft that would be the source of the signal that one seeks to receive (see Figure 1). This spatio-temporal equalizer would consist mostly of a bank of seven adaptive finite-impulse-response (FIR) filters — one

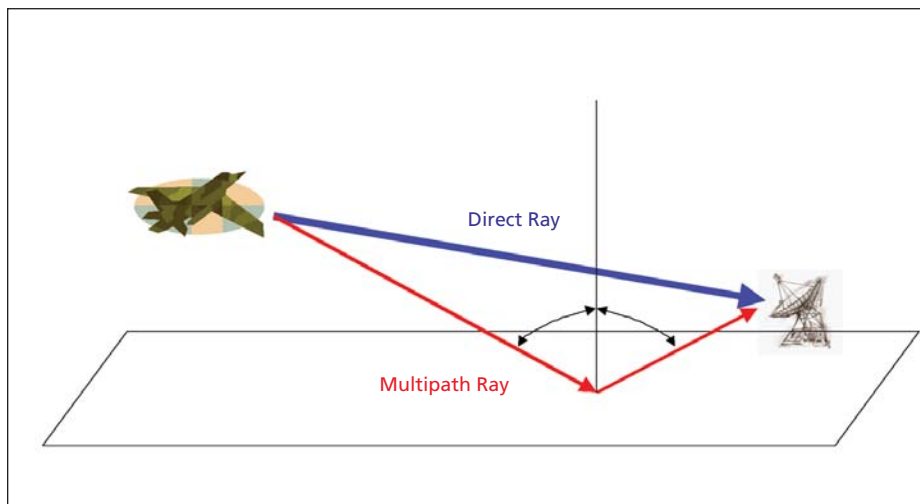


Figure 1. Signals Received by a Focal-Plane Array of feed horns would be processed by the spatio-temporal equalizer to suppress multipath effects and extract antenna-pointing information.