ROM through all phases of testing.

The controller has been designed as an integral subsystem of a system that includes not only the controller and the controlled EEPROM aboard a spacecraft but also computers in a ground control station, relatively simple onboard support circuitry, and an onboard communication subsystem that utilizes the MIL-STD-1553B protocol. (MIL-STD-1553B is a military standard that encompasses a method of communication and electrical-interface requirements for digital electronic subsystems connected to a data bus. MIL-STD-1553B is commonly used in defense and space applications.) The intent was to both maximize reliability while minimizing the size and complexity of onboard circuitry.

In operation, control of the EEPROM is effected via the ground computers, the MIL-STD-1553B communication subsystem, and the onboard support circuitry, all of which, in combination, provide the multiple layers of protection against inadvertent writes. There is no controller software, unlike in many prior EEPROM controllers; software can be a major contributor to unreliability, particularly in fault situations such as the loss of power or brownouts. Protection is also provided by a power-monitoring circuit.

This work was done by Richard Katz and Igor Kleyner of Goddard Space Flight Center. For further information, contact the Goddard Innovative Partnerships Office at (301) 286-5810. GSC-15492-1

Quad-Chip Double-Balanced Frequency Tripler

This technology has uses such as high-resolution radar and spectroscopic screening.

NASA's Jet Propulsion Laboratory, Pasadena, California

Solid-state frequency multipliers are used to produce tunable broadband sources at millimeter and submillimeter wavelengths. The maximum power produced by a single chip is limited by the electrical breakdown of the semiconductor and by the thermal management properties of the chip. The solution is to split the drive power to a frequency tripler using waveguides to divide the power among four chips, then recombine the output power from the four chips back into a single waveguide.

To achieve this, a waveguide branch-line quadrature hybrid coupler splits a 100-GHz input signal into two paths with a 90° relative phase shift. These two paths are split again by a pair of waveguide Y-junctions. The signals from the four outputs of the Y-junctions are tripled in frequency using balanced Schottky diode frequency triplers before being recombined with another pair of Y-junctions. A final waveguide branch-line quadrature hybrid coupler completes the combination.

Using four chips instead of one enables using four-times higher power input, and produces a nearly four-fold power output as compared to using a single chip. The phase shifts introduced by the quadrature hybrid couplers provide isolation for the input and output waveguides, effectively eliminating standing waves between it and surrounding components. This is accomplished without introducing the high losses and expense of ferrite isolators.

A practical use of this technology is to drive local oscillators as was demonstrated around 300 GHz for a heterodyne spectrometer operating in the 2–3-THz band. Heterodyne spectroscopy in this frequency band is especially valuable for astrophysics due to the presence of a very large number of molecular spectral lines. Besides high-resolution radar and spectrographic screening applications, this technology could also be useful for laboratory spectroscopy.

This work was done by Robert H. Lin, John S. Ward, Peter J. Bruneau, and Imran Mehdi of Caltech; Bertrand C. Thomas of Oak Ridge Associated Universities; and Alain Maestrini of the Observatoire de Paris for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-46567

Ka-Band Waveguide Two-Way Hybrid Combiner for MMIC Amplifiers

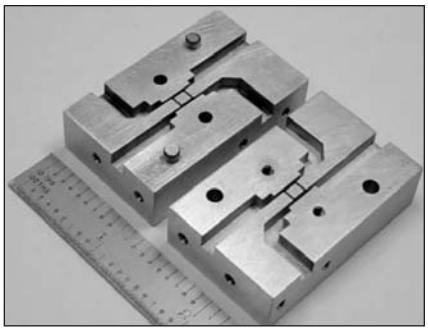
This technology is applicable as a power combiner for solid-state power amplifiers (SSPAs) with unequal and arbitrary power output ratios.

John H. Glenn Research Center, Cleveland, Ohio

The design, simulation, and characterization of a novel Ka-band (32.05±0.25 GHz) rectangular waveguide two-way branch-line hybrid unequal power combiner (with port impedances matched to that of a standard WR-28 waveguide) has been created to combine input signals, which are in phase and with an amplitude ratio of two. The measured return loss and isolation of the branch-line hybrid are better than 22 and 27 dB, respectively. The measured combining efficiency is 92.9 percent at the center frequency of 32.05 GHz. This circuit is efficacious in combining the unequal output power from two Ka-band GaAs pseudomorphic high electron mobility transistor (pHEMT) monolithic microwave integrated circuit (MMIC) power amplifiers (PAs) with high efficiency.

The component parts include the branch-line hybrid-based power combiner and the MMIC-based PAs. A two-waybranch-line hybrid is a four-port device with all ports matched; power entering port 1 is divided in phase, and into the ratio 2:1 between ports 3 and 4. No power is coupled to port 2.

MMICs are a type of integrated circuit fabricated on GaAs that operates at microwave frequencies, and performs the function of signal amplification. The power combiner is designed to operate over the frequency band of 31.8 to 32.3



The fabricated **Two-Way Ka-Band Branch-Line Hybrid Unequal Power Combiner** in E-plane split block arrangement. The dimensions of the assembled combiner are 1.8×1.2×1 in. (≈4.7×3.0×2.5 cm).

GHz, which is NASA's deep space frequency band. The power combiner would have an output return loss better than 20 dB. Isolation between the output port and the isolated port is greater than 25 dB. Isolation between the two input ports is greater than 25 dB. The combining efficiency would be greater than 90 percent when the ratio of the two input power levels is two. The power combiner is machined from aluminum with E-plane split-block arrangement, and has excellent reliability.

The flexibility of this design allows the combiner to be customized for combining the power from MMIC PAs with an arbitrary power output ratio. In addition, it allows combining a low-power GaAs MMIC with a high-power GaN MMIC. The arbitrary port impedance allows matching the output impedance of the MMIC PA directly to the waveguide impedance without transitioning first into a transmission line with characteristic impedance of 50 ohms. Thus, by eliminating the losses associated with a transition, the overall SSPA efficiency is enhanced.

For reducing the cost and weight when required in very large quantities, such as in the beam-forming networks of phased-array antenna systems, the combiner can be manufactured using metal-plated plastic. Two hybrid unequal power combiners can be cascaded to realize a non-binary combiner (for e.g., a three-way) and can be synergistically optimized for low VSWR (voltage standing wave ratio), low insertion loss, high isolation, and wide bandwidth using commercial off-the-shelf electromagnetic software design tools.

This work was done by Rainee N. Simons, Christine T. Chevalier, Edwin G. Wintucky, and Jon C. Freeman of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW 18473-1.

Radiation-Hardened Solid-State Drive

NASA's Jet Propulsion Laboratory, Pasadena, California

A method is provided for a radiation-hardened (rad-hard) solid-state drive for space mission memory applications by combining rad-hard and commercial off-the-shelf (COTS) non-volatile memories (NVMs) into a hybrid architecture. The architecture is controlled by a rad-hard ASIC (application specific integrated circuit) or a FPGA (field programmable gate array). Specific error handling and data management protocols are developed for use in a rad-hard environment. The rad-hard memories are smaller in overall memory density, but are used to control and manage radiation-induced errors in the main, and much larger density, non-rad-hard COTS memory devices.

Small amounts of rad-hard memory are used as error buffers and temporary caches for radiation-induced errors in the large COTS memories. The rad-hard ASIC/FPGA implements a variety of error-handling protocols to manage these radiation-induced errors. The large COTS memory is triplicated for protection, and CRC-based counters are calculated for sub-areas in each COTS NVM array. These counters are stored in the rad-hard non-volatile memory. Through monitoring, rewriting, regeneration, triplication, and long-term storage, radiation-induced errors in the large NV memory are managed. The rad-hard ASIC/FPGA also interfaces with the external computer buses.

This work was done by Douglas J. Sheldon of Caltech for NASA's Jet Propulsion Labora-Further information is contained in a TSP (see page 1). ***NPO-46925***