



The fabricated **Two-Way Ka-Band Branch-Line Hybrid Unequal Power Combiner** in E-plane split block arrangement. The dimensions of the assembled combiner are 1.8×1.2×1 in. (=4.7×3.0×2.5 cm).

GHz, which is NASA's deep space frequency band. The power combiner would have an output return loss better than 20 dB. Isolation between the output port and the isolated port is greater than 25 dB. Isolation between the two input

ports is greater than 25 dB. The combining efficiency would be greater than 90 percent when the ratio of the two input power levels is two. The power combiner is machined from aluminum with E-plane split-block arrangement, and has excellent reliability.

The flexibility of this design allows the combiner to be customized for combining the power from MMIC PAs with an arbitrary power output ratio. In addition, it allows combining a low-power GaAs MMIC with a high-power GaN MMIC. The arbitrary port impedance allows matching the output impedance of the MMIC PA directly to the waveguide impedance without transitioning first into a transmission line with characteristic impedance of 50 ohms. Thus, by eliminating the losses associated with a transition, the overall SSPA efficiency is enhanced.

For reducing the cost and weight when required in very large quantities,

such as in the beam-forming networks of phased-array antenna systems, the combiner can be manufactured using metal-plated plastic. Two hybrid unequal power combiners can be cascaded to realize a non-binary combiner (for e.g., a three-way) and can be synergistically optimized for low VSWR (voltage standing wave ratio), low insertion loss, high isolation, and wide bandwidth using commercial off-the-shelf electromagnetic software design tools.

This work was done by Rainee N. Simons, Christine T. Chevalier, Edwin G. Wintucky, and Jon C. Freeman of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW 18473-1.

Radiation-Hardened Solid-State Drive

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A method is provided for a radiation-hardened (rad-hard) solid-state drive for space mission memory applications by combining rad-hard and commercial off-the-shelf (COTS) non-volatile memories (NVMs) into a hybrid architecture. The architecture is controlled by a rad-hard ASIC (application specific integrated circuit) or a FPGA (field programmable gate array). Specific error handling and data management protocols are developed for use in a rad-hard environment. The rad-hard memories are smaller in

overall memory density, but are used to control and manage radiation-induced errors in the main, and much larger density, non-rad-hard COTS memory devices.

Small amounts of rad-hard memory are used as error buffers and temporary caches for radiation-induced errors in the large COTS memories. The rad-hard ASIC/FPGA implements a variety of error-handling protocols to manage these radiation-induced errors. The large COTS memory is triplicated for protection, and CRC-based counters are

calculated for sub-areas in each COTS NVM array. These counters are stored in the rad-hard non-volatile memory. Through monitoring, rewriting, regeneration, triplication, and long-term storage, radiation-induced errors in the large NV memory are managed. The rad-hard ASIC/FPGA also interfaces with the external computer buses.

This work was done by Douglas J. Sheldon of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-46925