



Technology Focus: Data Acquisition

Program Merges SAR Data on Terrain and Vegetation Heights

NASA's Jet Propulsion Laboratory, Pasadena, California

X/P Merge is a computer program that estimates ground-surface elevations and vegetation heights from multiple sets of data acquired by the GeoSAR instrument [a terrain-mapping synthetic-aperture radar (SAR) system that operates in the X and P bands]. X/P Merge software combines data from X- and P-band digital elevation models, SAR backscatter magnitudes, and interferometric correlation magnitudes into a simplified

set of output topographical maps of ground-surface elevation and tree height.

For computational efficiency, inversions are performed by use of lookup tables. The program performs calibrations to remove biases from output estimates, calibrates interferometric correlation magnitudes by accounting for geometric and radiometric errors, differentiates between surface and vegetated

areas, and, on a pixel-by-pixel basis, selects the lookup table corresponding to the best user-specified inversion approach.

This program was written by Paul Siqueira, Scott Hensley, Ernesto Rodriguez, and Marc Simard of Caltech for NASA's Jet Propulsion Laboratory.

This software is available for commercial licensing. Please contact Karina Edmonds of the California Institute of Technology at (626) 395-2322. Refer to NPO-40268.

Using G⁴FETs as a Data Router for In-Plane Crossing of Signal Paths

Cross-talk is low enough that integrity of signals could be preserved.

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Theoretical analysis and some experiments have demonstrated that silicon-on-insulator (SOI) 4-gate transistors of the type known as G⁴FETs could be efficiently used for in-plane crossing of signal paths. Much of the effort of designing very-large-scale integrated (VLSI) circuits is focused on area-efficient routing of signals. The main source of difficulty in VLSI signal routing is the requirement to prevent crossing, in the same plane, of wires that are meant to be kept electrically insulated from each other. Consequently, it often becomes necessary to design and build VLSI circuits in multiple layers with vias (connections between conductors in different layers at selected locations). Suitable devices that would prevent, or at least sufficiently suppress, undesired electrical coupling (cross-talk) between wires crossing in the same plane would enable compact, simpler implementation of complex interconnection networks with in-plane crossings that, heretofore, have not been possible in VLSI circuitry. The use of G⁴FETs as in-plane signal-crossing devices or routers, in combination with the use of G⁴FETs as universal programmable logic gates, would create opportunities for reducing complexity in VLSI design.

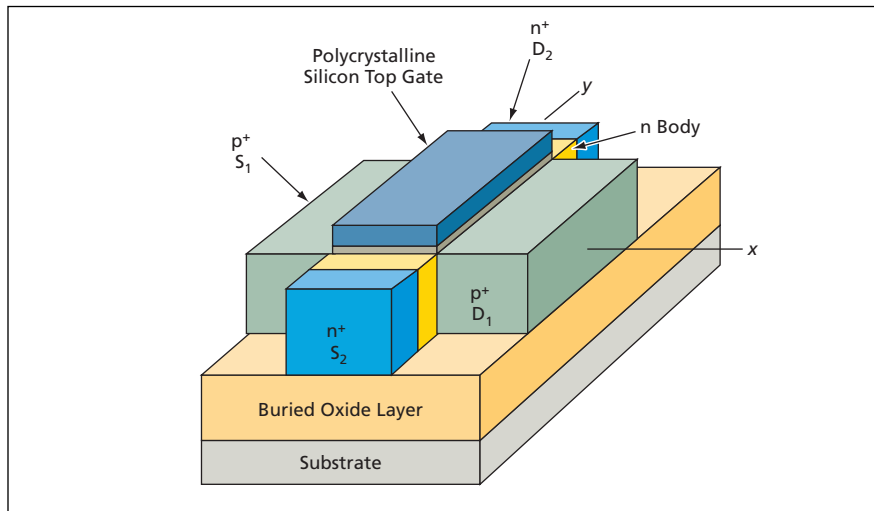


Figure 1. The G⁴FET consists of a p-channel inversion-mode MOSFET (including source S1 and drain D1) for current flowing in the x direction and an accumulation-mode n-channel MOSFET (including source S2 and drain D2) for current flowing in the y direction. The gate, body and substrate are common to both transistors.

A G⁴FET, depicted in simplified form in Figure 1, has the same basic structure as does a prior SOI cross-MOSFET (metal oxide/semiconductor field-effect transistor), though the cross-MOSFET is somewhat wider. The cross-MOSFET consists essentially of an inversion-mode and an accumulation-mode MOSFET that share gate and substrate terminals

and are oriented perpendicularly to each other. The prior use of the cross-MOSFET involved sequential operation of the inversion-mode and accumulation-mode MOSFETs. In contrast, the use of the G⁴FET as an in-plane router involves the simultaneous operation of the inversion-mode MOSFET in one in-plane direction and the accumulation-